

# A GaAs Distributed Amplifier with an Output Voltage of $8.5 V_{pp}$ for 40 Gb/s Modulators

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**Abstract**—In this paper, we report on a **Distributed Amplifier (DA)** with positive gain slope and  $8.5 V_{pp}$  output voltage swing at 20 GHz. This makes the amplifier suitable for driving LiNbO<sub>3</sub> modulators. The amplifier consists of six cascode cells and is fabricated in a commercially available 150 nm GaAs power pHEMT technology. Gain equals to 9.8 dB at low frequencies and rises up to 12.8 dB at 38 GHz. This amplifier is then cascaded with a preamplifier. Losses at high frequencies due to cascading are compensated by the positive gain slope of the amplifier described here. The cascaded amplifiers exhibit a gain of 19.5 dB and a bandwidth of 38 GHz with a flat frequency response of  $\pm 0.6$  dB up to 28 GHz.

## I. INTRODUCTION

The increase of data communication in recent years demands for increasing speed of the transmission systems. The transmission capacity is increased by **Wavelength Division Multiplexing (WDM)** together with increasing speed per channel. In fiber communication systems speed per channel went up from 2.5 Gb/s (OC-48) to 10 Gb/s (OC-192) and future 40 Gb/s (OC-768) are examined.

With very advanced SiGe HBT and InP HEMT based technologies, also bit-rates exceeding 40 Gb/s have been demonstrated [1], [2]. However, these technologies often do not offer the high breakdown voltage needed for driving 40 Gb/s LiNbO<sub>3</sub> Mach-Zehnder modulators. For bit-rates exceeding 10 Gb/s, due to introduced chirp, the laser source can no more be modulated directly. External modulators are realized either as **Electro Absorption (EA)** or **Mach-Zehnder (MZ)** modulators. State-of-the-art LiNbO<sub>3</sub> based MZ modulators typically require voltage swings of 5 to  $7 V_{pp}$  [3]. This makes it necessary to design the modulator driver with either InP double heterojunction bipolar transistors [3] or GaAs based technologies.

In this paper we describe the realization of an amplifier based on a relatively cost-effective GaAs HEMT technology to achieve the necessary drive voltage requirements for LiNbO<sub>3</sub> MZ modulators. Due to the relative low transistor speed of high power GaAs pHEMTs, a distributed amplifier topology, which is known for its excellent bandwidth performance [4], is utilized. The idea of a DA is to use several small active devices in parallel instead of one large one, and to separate parasitic capacitances by high impedance transmission lines. The resulting small signal structure at the input and output is designed to behave like a  $50 \Omega$  artificial lumped transmission line and therefore shows both small input and output reflection as well as flat gain over a large bandwidth. With this circuit topology, one can simultaneously have the high frequency characteristics of one unit-cell together with gain and output power performance of all unit-cells in parallel. This makes

the concept an attractive candidate for high speed modulator drivers.

## II. CIRCUIT DESIGN

The amplifier is realized in the commercially available PPH15 process of **United Monolithic Semiconductors (UMS)**. This is a high power 150 nm pseudomorphic HEMT GaAs process with an  $f_t$  of 75 GHz. The devices have an optimum transconductance of  $g_{m,max} = 550 \text{ mS/mm}$  at  $V_{GS} = -0.4 \text{ V}$ , a breakdown voltage of  $V_{bds} > 8 \text{ V}$ , and a power density of  $P_{1dB} = 0.6 \text{ W/mm}$ .

The basic topology of the amplifier is shown in Fig. 1.

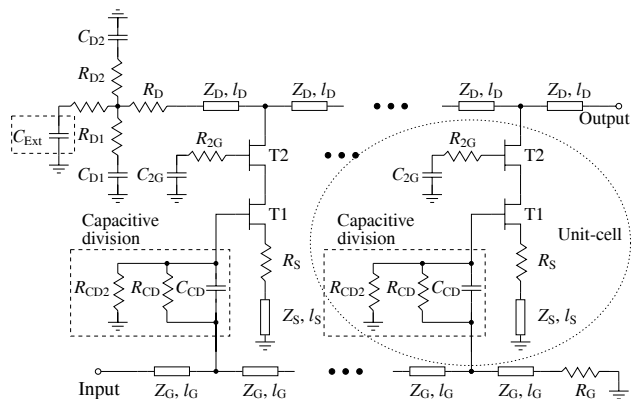


Fig. 1. Simplified circuit topology of the amplifier. The dashed box depicts the capacitive division principle at the input.

The on-chip termination on the artificial drain line provides a flat frequency response down to several GHz. To enable a good reverse drain termination down to frequencies in the kHz range, a pad is provided to attach an external 100 nF capacitor on top of the amplifier (see Fig. 7 on the right hand side). Alternatively, the pad can be used for bonding to an external high frequency laminate with the external SMD capacitor attached on it. For compensation of parasitics associated with the external capacitor, a small on-chip resistor is placed in series to the pad.

To achieve an output voltage swing close to the breakdown voltage of the transistors, six unit-cells are used. A large gate width of  $120 \mu\text{m}$  provides the wanted gain and power with a relatively small amount of unit-cells. Cascode cells are used to increase output impedance and decrease Miller-effect resulting in a smaller input capacitance at the gate terminal of the common source FET. A negative output resistance of the cascode at high frequencies allows for compensation of

losses on the artificial drain line [5]. However, the negative output resistance gives rise to instabilities and has to be partly compensated by the resistor  $R_{2G}$  and inductive source degeneration  $Z_S$  [5]. Other possibilities for stabilization of a DA are shown for example in [6], [7].

The micrograph of the circuit is shown in Fig. 2.

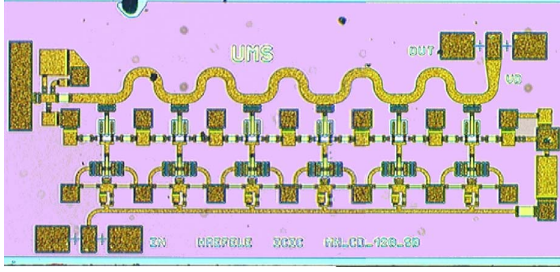


Fig. 2. Micrograph of the capacitive division DA (Chip size:  $2.50 \times 0.96$  mm<sup>2</sup>)

Because design rules request via holes to be separated by at least  $130\mu\text{m}$ , via holes are shared between two adjacent transistors to save expensive wafer-area.

Simultaneously achieving high bandwidth and output power is very challenging in microwave designs. By using a small gate width for the FET, a high bandwidth can be achieved but at the expense of reduced gain for a given number of unit-cells. In order to obtain high output power however, one would have to use many unit-cells which will increase gain ripple and instability [5]. In this paper we describe a DA with cascode cells and capacitive division. Using a capacitor in series to the transistors' input reduces the total input capacitance. This principle is therefore often used to achieve an ultra high bandwidth [8], [9], [10]. However, in this paper the circuit is optimized for high output power with good fabrication reproducibility. Thus, an increased gate width is used while still maintaining the same input capacitance as for a smaller FET without capacitive division. The increased gate width translates to more output current and thus power. Thereby the same output power can be realized with less unit cells reducing gain ripple and fabrication variations. For a typical FET, the input capacitance  $C_{gs}$  is larger than its output capacitance  $C_{ds}$ , which means that the cut-off frequency of a DA is limited by the artificial gate line. The serial capacitor  $C_{CD}$  between the input line and the gate of the common source FET reduces the effective input capacitance to:

$$C_{in,eff} \approx (C_{CD} \cdot C_{in,cas}) / (C_{CD} + C_{in,cas}) , \quad (1)$$

where for a cascode  $C_{in,cas}$  is approximately  $C_{gs}$  due to the unity voltage gain for the common source transistor:

$$C_{in,cas} = C_{gs} + C_{gd}(A_v + 1) \approx C_{gs} . \quad (2)$$

This way, bandwidth is increased at the expense of gain. However, high gain can be achieved with a preamplifier realized in a technology with higher cut-off frequencies, like for example a low noise GaAs technology [6] or a fast SiGe based technology, see for example [1], [11]. For biasing of the gate, a high ohmic resistor  $R_{CD}$  is put in parallel to  $C_{CD}$ . The outcome of the parallel combination of  $C_{CD}$  together

with  $R_{CD}$  is a high pass filter, which limits the low frequency performance. Thus, a second resistor  $R_{CD2}$  is placed in parallel to  $C_{gs}$ .

$$R_{CD2} = \frac{R_{CD} \cdot C_{in,cas}}{C_{CD}} . \quad (3)$$

The resistors  $R_{CD}$  and  $R_{CD2}$  have to be as large as possible to not introduce additional attenuation to the artificial gate line. However, a compromise has to be found between physical size and resistance. Therefore  $R_{CD}$  and  $R_{CD2}$  are chosen to  $2\text{k}\Omega$  and  $3\text{k}\Omega$ , respectively.

A positive gain slope is utilized by resistive source degeneration  $R_S$ . To additionally allow for self-biasing of the gate ( $V_{gs,opt} = -0.4\text{V}$ ), the value for  $R_S$  is chosen such that a compromise is achieved between gain slope and good self-biasing for improved overall gain. Furthermore, the source degeneration slightly improves the output voltage.

### III. MEASUREMENT RESULTS

For all measurements shown, a drain biasing of  $V_{DD} = 8.5\text{V}$  is applied, resulting in a power consumption of  $2.6\text{W}$ . Due to the resistive source degeneration, the gate line is left unbiased.

The measured small signal gain of the amplifier is shown in Fig. 3.

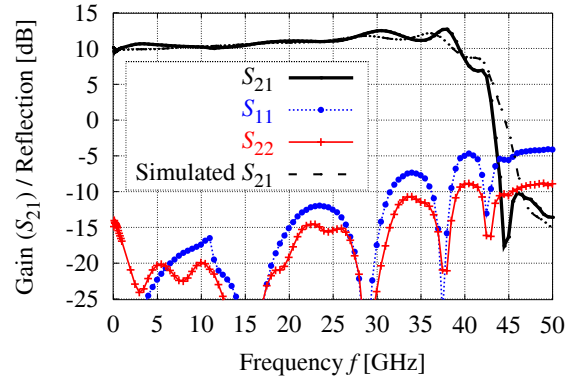


Fig. 3. On-wafer measured small signal performance of the amplifier. The gain equals to  $9.8\text{dB}$  near DC and rises to  $12.8\text{dB}$  at  $38\text{GHz}$ .

The midband gain of this amplifier is  $11.1\text{dB}$  with the gain rising from  $9.8\text{dB}$  near DC to  $12.8\text{dB}$  at  $38\text{GHz}$ . The positive gain slope of  $3\text{dB}$  was designed to equalize parasitic losses when mounted to a substrate. The measured data fits the simulation very well, except at the high frequency end where increased ripple shows up for the measurement. This ripple is due to higher gain peaking caused by slightly smaller stabilization resistances compared to simulations. Up to  $30\text{GHz}$ , input reflections are less than  $-11.5\text{dB}$ . Output matching is better than  $-14.5\text{dB}$  up to  $30\text{GHz}$  and less than  $-8.5\text{dB}$  within the  $50\text{GHz}$  measurement bandwidth.

The performance spread of 40 measured devices located at different positions on the wafer is very low, see Fig. 4. The gain variation at  $20\text{GHz}$  is within  $\pm 0.6\text{dB}$  over the whole wafer. The  $-3\text{dB}$  cut-off frequency exceeds  $36.5\text{GHz}$  for all measured devices. The low spread in gain and bandwidth also makes the amplifier suitable for production.

In case of optical systems the group delay is important in terms of low time jitter and thus good horizontal eye opening.

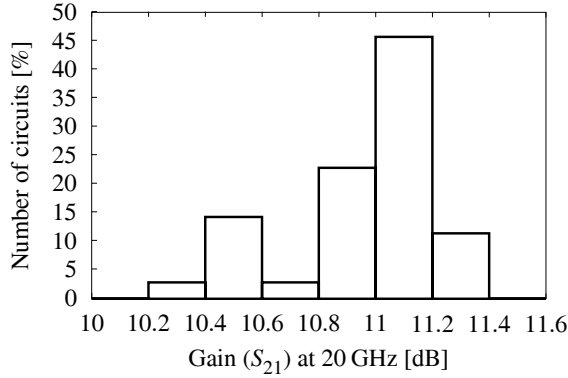


Fig. 4. Wafer spread of the gain at the midband frequency of 20 GHz. The gain variation is within  $\pm 0.6$  dB for all measured devices.

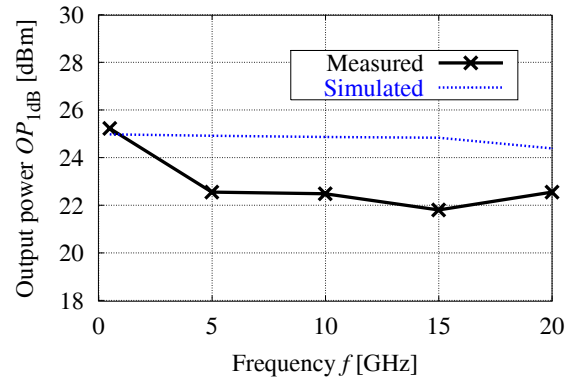


Fig. 6. Output power at 1 dB gain compression versus frequency. At 20 GHz the output power equals to 22.6 dBm.

A comparison between the measured and simulated group delay for this amplifier is shown in Fig. 5. The measured

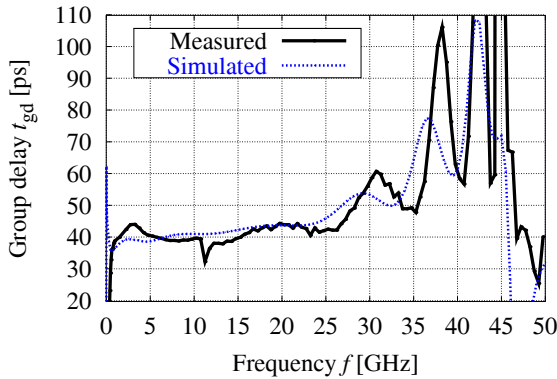


Fig. 5. Group delay of the amplifier. Measured group delay equals to  $\pm 15$  ps between 1 and 36 GHz.

group delay is less than  $\pm 15$  ps from 1 to 36 GHz. However, it degrades at higher frequencies due to the increased gain peaking.

The output power at -1 dB gain compression versus frequency is depicted in Fig. 6.

At low frequencies (0.5 GHz) the output power at 1 dB gain compression is 25.3 dBm or 11.6 V. The output power at 20 GHz equals to  $OP_{1dB} = 22.6$  dBm, which is equivalent to  $8.5 V_{pp}$  at  $50 \Omega$ , making the amplifier suitable for driving LiNbO<sub>3</sub> modulators.

The positive gain slope is now used to end up with a flat frequency response for the case that this amplifier is cascaded with a previously fabricated preamplifier [6]. The preamplifier exhibits a flat frequency response over the 50 GHz measurement bandwidth with a gain of  $11.3 \pm 1$  dB [6]. The output power of 13.2 dBm at 20 GHz is sufficient to drive the amplifier presented here into its limiting range. For cascading of the two amplifiers bias decoupling is needed. Therefore, the output of the preamplifier is connected to a transmission line on a Teflon<sup>®</sup> based substrate (Rogers Corporation RT/duroid<sup>®</sup> 5880) via two bond-wires. In the middle of the transmission line is the foot-print for a broadband capacitor. A

multilayer capacitor from Presidio Components Inc. is attached on top of it. Again, two bond-wires are used to connect the transmission line with the input of the amplifier described here. The substrate was chosen to give good high frequency performance. A substrate thickness of  $130 \mu\text{m}$  is taken to fit approximately the  $100 \mu\text{m}$  height of the fabricated amplifiers, allowing for short bond-wires. In Fig. 7, a micrograph of the cascaded amplifiers glued on a metal block is shown.

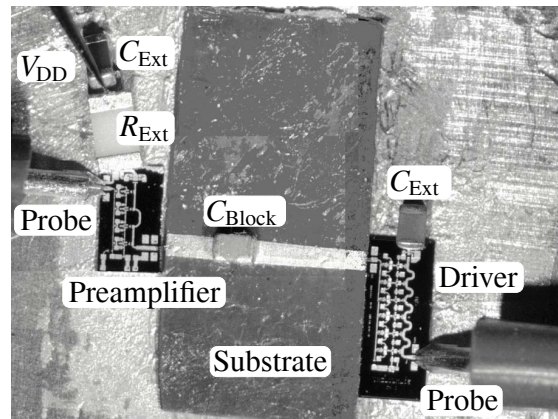


Fig. 7. Photograph of a preamplifier cascaded with the capacitive division DA probed by ground-signal-ground probes for small signal measurements.

Drain biasing for the preamplifier is applied by a needle connected to the off-chip capacitor used for grounding of low frequency signals. For the capacitive division DA the drain biasing is applied via the bias-Tee of the measurement setup. Due to the self-biasing of the power amplifier, no gate voltage has to be applied, strongly simplifying the assembly of the two amplifiers. The transistor technology of the preamplifier has its optimum transconductance at  $V_{gs,opt} = 0$  V and no gate biasing is needed either. For small signal measurements, on-wafer probe tips are connected to the input of the preamplifier and the output of the capacitive division DA. Small signal measurements for the cascaded amplifiers are shown in Fig. 8.

The gain equals to 19.5 dB with a cut-off frequency of 38 GHz. A flat gain of  $\pm 0.6$  dB up to 28 GHz is achieved by the positive gain slope which compensates for transmission line attenuation and losses due to the DC-blocking capacitor

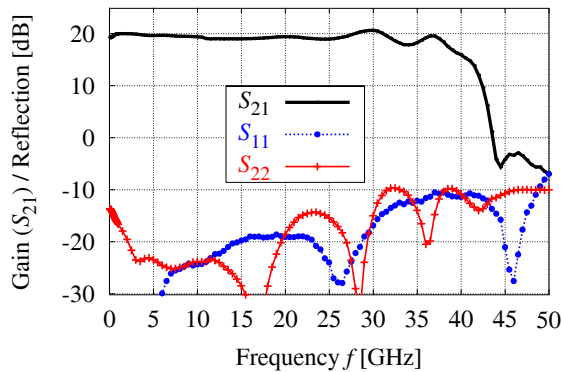


Fig. 8. On-wafer measured small signal performance of the cascaded amplifiers. The gain equals to 19.5 dB with a bandwidth of 38 GHz.

and bond-wires. Both, input and output matching are better than -9 dB up to 49 GHz.

#### IV. SUMMARY

In this paper we presented a distributed amplifier with six cascode unit-cells realized in a technology with a cut-off frequency of  $f_t=75$  GHz. Capacitive division is used at the input to allow for a larger gate width, reducing the number of unit-cells for the same output power. Resistive source degeneration is utilized for self-biasing and achieving a positive gain slope for gain equalization. The amplifier exhibits a gain of 9.8 dB at 50 MHz and rises by 3 dB up to 38 GHz. The high output power of 22.6 dBm at 20 GHz makes the amplifier suitable for applications requiring high voltage swings like for example LiNbO<sub>3</sub> based Mach-Zehnder modulators. The positive gain slope of this amplifier is used to compensate for losses when cascaded with a previously fabricated preamplifier. The cascaded amplifiers show an on-wafer measured gain of 19.5 dB with a flat frequency response of  $\pm 0.6$  dB up to 28 GHz and a -3 dB bandwidth of 38 GHz.

#### V. ACKNOWLEDGMENTS

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#### REFERENCES

- [1] O. Wohlgenuth, P. Paschke, and Y. Baeyens, "SiGe broadband amplifiers with up to 80 GHz bandwidth for optical applications at 43 Gbit/s and beyond," *Digest of European Microwave Conference*, pp. 1087–1090, October 2003.
- [2] S. Masuda, T. Takahashi, and K. Joshin, "An Over 110-GHz InP HEMT Flip-chip Distributed Baseband Amplifier with Inverted Microstrip Line Structure for Optical Transmission Systems," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 9, pp. 1479–1484, September 2003.
- [3] Y. Baeyens, N. Weimann, P. Roux, A. Leven, V. Houtsma, R. F. Kopf, Y. Yang, J. Frackowiak, A. Tate, J. S. Weiner, P. Paschke, and Y.-K. Chen, "High Gain-Bandwidth Differential Distributed InP D-HBT Driver Amplifiers With Large (11.3 V<sub>pp</sub>) Output Swing at 40 Gb/s," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1697–1705, October 2004.
- [4] K. Takahata, Y. Muramoto, H. Fukano, K. Kato, A. Kozen, S. Kimura, Y. Imai, Y. Miyamoto, O. Nakajima, and Y. Matsuoka, "Ultrafast Monolithic Receiver OEIC Composed of Multimode Waveguide p-i-n Photodiode and HEMT Distributed Amplifier," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 6, no. 1, pp. 31–37, February 2000.
- [5] H. Shigematsu, M. Sato, T. Hirose, and Y. Watanabe, "A 54-GHz Distributed Amplifier With 6-V<sub>pp</sub> Output for a 40 Gb/s LiNbO<sub>3</sub> Modulator Driver," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1100–1105, September 2002.
- [6] M. Häfele, K. Beilenhoff, and H. Schumacher, "A GaAs PHEMT Distributed Amplifier with Low Group Delay Time Variation for 40 Gbit/s Optical Systems," *Digest of European Microwave Conference*, pp. 1091–1094, October 2003.
- [7] J. M. Carroll, M. Coutant, M. S. Heins, C. F. Campbell, and E. Reese, "0.25  $\mu$ m pHEMT 40 Gb/s E/O Modulator Drivers," *IEEE MTT-S Digest*, pp. 489–492, 2002.
- [8] J. Pustl, B. Agarwal, R. Pullela, L. D. Nguyen, M. V. Le, M. J. W. Rodwell, L. Larson, J. F. Jensen, R. Y. Yu, and M. G. Case, "Capacitive-Division Traveling-Wave Amplifier with 340 GHz Gain-Bandwidth Product," *IEEE MTT-S International Microwave Symposium Digest (Orlando, Florida, 1995)*, pp. 175–178, 1995.
- [9] B. Agarwal, A. E. Schmitz, J. J. Brown, M. Matloubian, M. G. Case, M. Le, M. Lui, and M. J. W. Rodwell, "112-GHz, 157-GHz, and 180 GHz InP HEMT Traveling-Wave Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2553–2559, December 1998.
- [10] M. S. Heins, J. M. Carroll, M.-Y. Kao, C. F. Steinbeiser, T. R. Landon, and C. F. Campbell, "An ultra-wideband GaAs pHEMT driver amplifier for fiber optic communications at 40 Gb/s and beyond," *IEEE Optical Fiber Communication Digest*, pp. 273–274, March 2002.
- [11] G. Freeman, M. Meghelli, Y. Kwark, S. Zier, A. Rylyakov, M. A. Sorna, T. Tanji, O. M. Schreiber, K. Walter, J.-S. Rieh, B. Jagannathan, A. Joseph, and S. Subbanna, "40-Gb/s Circuits Built From a 120-GHz  $f_t$  SiGe Technology," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1106–1114, September 2002.