GaAs custom MMIC foundry service : a business view

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ABSTRACT

In the 80's, almost all the GaAs IC companies offered on a commercial basis to fabricate prototype MMIC's designed or not by the customer himself into the foundry proprietary processes.
Most of the leading GaAs IC companies have today discontinued their foundry service to focus on large volume production of standard parts like power amplifiers for mobilecom terminals.
However the traditional custom foundry business is well alive and kicking and will reach 250 MEuros in 2000 representing 20 % of the total GaAs MMIC market. It is no longer limited to prototyping but also includes small to medium volume production of customer specific ICs (CSICs).
The various GaAs custom foundry services are reviewed in detail including process guarantees, CAD support and the "known good die" issue. The economics of a GaAs foundry service is revisited and a business perspective for the coming years is given.

1) INTRODUCTION

In 1996 (1), 22 of the 46 GaAs IC fabrication lines in operation worldwide were offering some kind of foundry service . These foundries were located in the US and in Europe and only one in Japan. This picture had not changed significantly since the early 80's when the main goal was to build up a customer base and prove that GaAs ICs was the way to solve many of the shortcomings of hybrid solutions based on discrete FETs.
Fabless system houses which pioneered the use of GaAs IC foundries to prototype their µW functions (2) helped a lot in turning around research groups into industrial companies, especially by forcing the foundries to be clear on commitments (lead time, specified PCM parameters, traceability..) and keep to them. Unlike the silicon foundries, the GaAs IC foundry business is still very fragmented with foundry dependent processes like : single or double threshold PHEMT, GaInP/GaInAs or GaAlAs HBTs, self-aligned or recessed gate FETs, MOCVD or MBE heterostructures, etc...
In this paper, we only consider analogue custom ICs including high bit rate interface ICs with operating frequencies from a few 100 MHz up to 100 GHz. Custom ICs implies that the customer is actively involved in the development of the circuit by specifiying it, designing it and testing it with or without the support of the Foundry.
To assess the GaAs custom MMIC foundry business today, will first review the strengths and weaknesses in terms of key issues like : multiple projects, multiple customers, available and qualified processes, back-end processes, traceability and process change management, on-wafer tests, CAD tools and customer support, PCM specifications and statistical process control, unspecified parameters and parasitic effects, the known good die issue and the cost factor.
The paper is concluded with a short discussion of the threats and opportunities facing this business. This includes Si advances both in CMOS or BiCMOS, but also the future of custom designs against system solutions based on standard parts at ever higher frequency.

2) GaAs CUSTOM MMIC MARKET

The GaAs MMIC merchant market (3) is segmented into standard ICs which are the driving force today and custom ICs . In particular custom MMICs amounted to 180 MEuros in 1998. This comprises a significant prototyping part or NREs (non recurring expenses) of 60 MEuros and a production part of 120 MEuros. The custom MMIC business currently shows a 20 % CAGR, and is expected to reach 250 MEuros in 2000. It should be noted that this does not include the captive custom market that was originally established in defense related companies (figures 1, 2).
Custom MMICs are expected to be dominated by low noise or power amplifiers over the next five years much like standard parts, but they are specific to the customer proprietary system architecture. Preferred custom applications are :

- Defense and space telecommunications
- High bit rate fiber optic links
- Cellular base stations
- CATV modules
- Multi channel DBS distribution systems
- Instrumentation
- Automotive.

3) STRENGTHS AND WEAKNESSES OF THE GaAs CUSTOM MMIC FOUNDRY SERVICE

The GaAs foundry service has now grown into a mature industrial business, essentially dedicated to professional applications, with small to medium volume production (typically from 10 K to 1M ICs/year). After more than 10 years of customer feed-back through customer satisfaction survey, the procedures, design tools, guarantees, and also process limitations are usually considered satisfactory, even if improvements are still needed. We will analyse the present strengths and weaknesses in terms of key factors regularly regarded as sensitive by customers.

The custom foundry service flow, lead time guarantee and quality assurance

Most foundries today are at least ISO 9001 certified. Working with such a foundry (4) requires to accept a very strict flow of tasks fully documented and typically divided into : IC design, manufacturing and the testing. The key issue is the manufacturing lead time which is strongly affected by the starting time of the customer's wafer run.

In a foundry line typically loaded at 85 % capacity, prototype runs have to inserted in time slots that have to be planned long ahead and are not flexible. As a consequence the lead time of prototype runs is often experienced by the customer to vary from 5 to 10 weeks for a 10 mask level process, while the intrinsic fabrication time is only 3 weeks. The foundry commitment can only concern the maximum lead time.

Multiple projects, multiple customers

Some foundries offer shared prototype service also known as MCP (multichip project) or even PCO (prototype chip option). The time slot here is even more stricter, since up to 10 customers, each having 5 to 10 different designs, can be accommodated on the same wafer. This type of foundry service is primarily dedicated to Universities, Research institutes and SMEs.

One of the limitation is the allowed chipsize in the fixed pattern : for exemple : 1 x 1.5, 2 x 1.5, 2 x 3 or 2 x 1 mm^2. This has consequences on the number of pads, the In and Out active lines and finally the overall performance of the IC.

Available and qualified processes

Processes have to pass successive milestones before being released for production :

NPR : new process request
APD : approval for process development
AMI : approval for market introduction
APP : approval for preproduction
RFP : release for production

Basically after AMI, the process is open for collaborative projects with customers needing the most advanced processes. On the contrary, production can only be started after APP. At RFP, full statistical data is available and SPC control charts are in place.

Process roadmap

The GaAs process roadmap pursued by foundries worldwide has continuously kept ahead of its Si counterpart. The MESFET branch is now clearly being terminated to be replaced by the PHEMT / MHEMT processes on the one hand (figure 3) and the HBT processes on the other. A few additional statements can be made.

GaAs PHEMTs are steadily being scaled down below 0,1 µm especially for low noise applications.

GaAs MHEMTs (metamorphic HEMTs) are expected to supersede PHEMTS once the reliability issue is totally cleared. This will enable to reach InP HEMT performance on a GaAs.substrate.

Reliability of GaInP/GaInAs HBTs has now been clearly proven to be superior to that of GaAlAs/GaInAs HBTs at high current density (10^6 - 10^7 A/cm^2).

Finally Enhancement / Depletion MESFET and PHEMT processes are best suited for compact, efficient and low-cost circuitry (fig 3) especially for analogue / digital interface ICs.

Back-end processes

Back-end processes include all the actions from the release of PCM good wafers to shipment to the customer of the final product which can be a tested or untested packaged or unpackaged IC.

Back-end processes start with thinning, dicing, then after on-wafer test, assembly in a plastic or ceramic package followed by final test. Foundry back-end services now offer alternative solutions to the conventional through the substrate via holes like bumps (figure 4) for flip-chip mounting. Coplanar design is also used, but much controversial in terms of chip area reduction.

Back-end lead-time remains a bottleneck, since it is usually an option, specific to the customer. It should be noted that conventional RF plastic package (LQFP32, TQFP48, SS016, etc..) are now well modelled and available from the main foundries.

Traceability and process change management

This has been a significant improvement over the last 10 years. Some foundries do stick to a strict process change management, guaranteeing full transparency. This has to be based on adequate full traceability where any change, minor or major, is kept track of. This includes all the products supplied upfront to the foundry chemicals, gases, substrates, evaporation materials... Audit by the customer is a prerequisite to build up lasting partnership.

On-wafer tests

On-wafer testing of low-noise and power devices is now available up to at least 60 GHz from most foundries. One of the main issues concern L-band applications where testing of UNBALANCED functions can be troublesome due to unsatisfactory decoupling of active probes. Multifunction chip or high gain amplifiers do require a long development time and results in a high test price. DC testing is always a minimum test, which combined with high grade visual inspection and sampling RF testing on a board, can be an acceptable test strategy for many customers.

CAD tools and customer support

After many years of extensive research on device and process modelling, it is now recognized that GaAs processes are not as simply and satisfactorily modelled as silicon (due to not well defined surface states and to the existence of deep-traps in the substrates). Pragmatic approaches based on DOEs (design of experiments) associated with simple equivalent network have been shown to be most cost-effective.

Comprehensive and user friendly design manuals are available even in CDROM form (4). Smart libraries of the main active and passive devices including pre laid-out cells have significantly eased off the task of IC designers.

The main simulation tools today are PSPICE with the TOM model for low frequency analogue / digital RC design. More traditional Microwave environment are MDS from HP and series IV from Eesof / HP. Both have to be supported by the foundries. They will soon be merged into the ADS tool which will save a lot of energy and money .

PCM specifications, statistical process control and yield statistics

The foundries generally releases wafers based on specifications to be met by selected electrical parameters on at least 80 % of 5 to 12 process control monitors (PCMs) located at specific positions across the wafer. These parameters include sheet resistances of metal layers and GaAs active layers, the capacitance per unit area of MIM capacitances and the DC and RF key parameters of the active devices like saturated drain current (Idss), transconductance (Gm0), threshold voltage (Vt), breakdown voltages (Bvgs, Bvgd ,Vdss max), and unity current gain cut-off frequency (Ft).

Not all the foundries guarantee all these parameters, especially the RF ones which are derived from a simple equivalent network of the active device. In addition no standard definition of these parameters is used by the various foundries. As an example Ft is either defined as h21 (Ft) = 0, or Gm0 / (2 π Cgs) or finally Gmo / (2 π (Cgs + Cgd)). But even when h21(Ft) = 0 is used, different Fts are derived whether the test pad capacitance for the microwave probe is included or not (figure 5).

Comparing processes between foundries can only be done on a specific design, small signal parameters measured at the biasing points, for instance do not tell everything about the behaviour of the active devices (figure 6).

In the recent years, SPC (statistical process control) has been extensively used on-line for physical parameters like thicknesses, spacings, feature sizes and off-line for PCM's electrical parameters. The control cards and corrective action plans enable to guarantee that the distribution of the wafer parameters are stable in time. Historical data to calculate Cpk's should be based on at least one year production (figure 7). Continuous adjustment is totally unacceptable, and was unavoidable at a time when substrate purity was not reproducible (1).
Worst-case simulation based on the distributions given in the design manuals can always be used to centre the design and determine the sensitive design parameters like the threshold voltage Vt or input gate to source capacitiance Cgs or drain to source resistance Rds.
An experimental DOE (design of experiments) is then recommended to determine the worst case performance of the IC across the process variation range.

Unspecified parameters and parasitic effects (5)
For a long time, GaAs ICs have been plagued with parasitic effects like backgating, gate and drain lags and photosensitivity. These effects affect the operation of ICs in many ways by reducing the output voltage in digital ICs, the output power of power stages, or by increasing the 1/f noise of low noise amplifiers and phase noise of oscillators due to substrate oscillation.
All these effects have been minimized by adequate process changes. Deep P+ implant is used to reduce low frequency response of deep trap levels at the active layer substrate interface and proper gate recess and passivation allow to minimize low frequency modulation of access resistances by surface states.
It remains true that, before embarking on a design, a specific process characterization might be needed. Power amplifier design usually requires a complete load pull analysis of the frequency dispersion of the drain characteristics of FETs .

The known good die issue, the wafer size and the cost factors
To understand some parameters ruling the economics of this business, we consider a simple cost model for a known good die in a 0.2 µm process using e-beam writing. The main cost factors are : substrate price (SP), wafer area (WA), chip area (CA), material cost/wafer (MC), e-beam writing / unit time (EBW), Line yield (Y), on-wafer RF IC yield (RFY), RF IC test cost/ wafer (TC), processing fixed cost (FC), number of wafers processed per year (C).
PCM good wafer cost (WC) = (SP + MC + (EBW x writing time + FC) / C) / Y.
Known good die cost = (WC x WA / CA +TC) / RFY
The substrate price, material cost are primarily independent of the wafer count per year. The e-beam-writing cost is the dominant factor since it is time consuming and directly proportional to the number of dies per wafer.
In this case, increasing the wafer size has hardly any impact on the die cost, because of the e-beam writing cost. Using a stepper solves this issue as long as the equipment as any other in the line is used up to 85 % capacity. Moving from 4 to 6 inch is always the good move, but the transition period might be painful economically speaking since the goal is always to load up the fab. A 40 % loaded fab is disastrous.
Line yield of 75 % to 90 % for volume production are now readily achieved. However, to guarantee that 1 or 2 prototype wafers are delivered at the committed time, a 3 to 6 minimum wafer batch is used. The effective prototyping yield is then 33 % resulting in 2 to 3 times higher wafer cost.
Finally RF IC yield, is very much dependent on the design robustness of the IC. To be able to offer a known good die service, a DOE is needed to determine the RF IC yield without having to process hundreds of wafers.

4) TREATS AND OPPORTUNITIES OF THE GaAs CUSTOM MMIC FOUNDRY SERVICE

Over the last ten years, not one technology has emerged that offers global trade-offs between contradictory parameters like output power, linearity, low noise, low supply voltage operation, mmW cut-off frequencies, etc... that could be used for any applications.
Much to the dismay of silicon experts, all the RF technologies are developing alongside each other for the foreseeable future. The real opportunities of the GaAs custom MMIC foundry service do reside in the increasing need from the major telecommunication companies for higher performance infrastructure networks using fiberoptic, cable or wireless links at very high bit rate (10, 40, 80 Gb/s) and high frequencies (20, 30, 45 GHz..). The market dynamics is faster than silicon advances, leaving enough room for GaAs ICs.

In addition custom ICs continue to be a prerequisite for leading telecommunication system houses which are needed to keeping ahead of their competitors by innovative system architecture based on the most advanced processes. The customer-foundry partnership is in this case the key success factor.

5) CONCLUSIONS

In the last ten years, GaAs custom MMIC foundries have matured by adopting and putting into practice all the industrial methodology of the silicon industry. The customer base is now well trained and do trust the technology. IC custom needs are not diminishing despite the tremendous growth of the GaAs standard IC market. The real challenge is to keep ahead of Si RF solutions as has been the case for 20 years now. GaInP/GaInAs HBTs and MHEMTs are two solid examples of recent breakthroughs that will enable this industry to move forward.

Acknowlegments
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Figures

Figure 1 GaAs custom MMIC market (source : Strategy Analytics)
Figure 2 GaAs NRE market (source : Strategy Analytics)
Figure 3 PHEMT and MHEMT roadmap
Figure 4 Bumps for flip chip mounting
Figure 5 ED PHEMT Ft versus gate length (Lg) (Ft defined as h21 (Ft) = 0 with RF probing pad Capacitance (1) or without (2)
Figure 6 Gain versus frequency of a 3 stage amplifier fabricated in 0.5µm D-mode processes from 5 different foundries. Processes #1 and #2 have identical Ft at operating biasing point (ref : 2 of this paper)
Figure 7 Distribution of Gmo over time in a SPC'ed process.

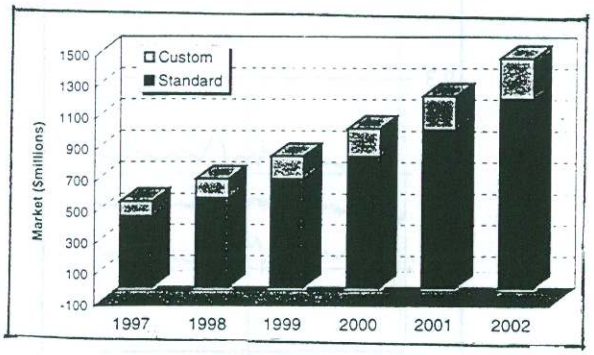

Figure 1

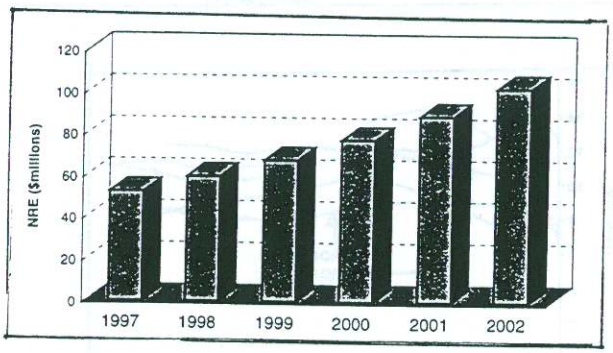

Figure 2

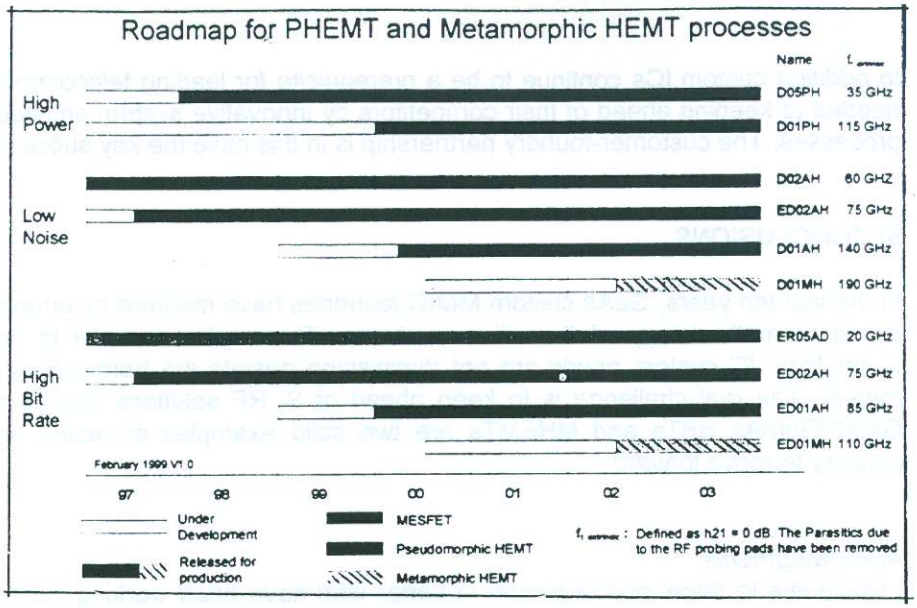

Figure 3

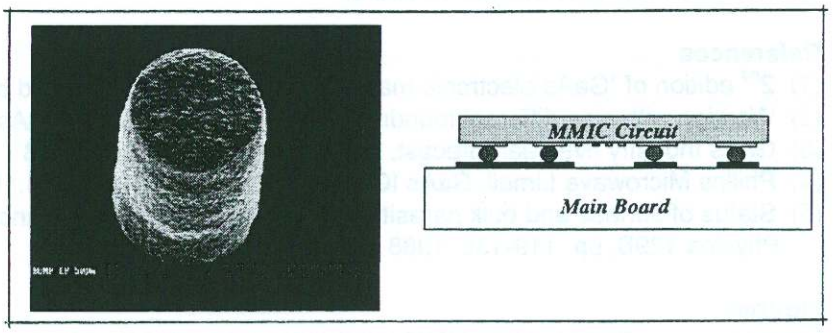

Figure 4

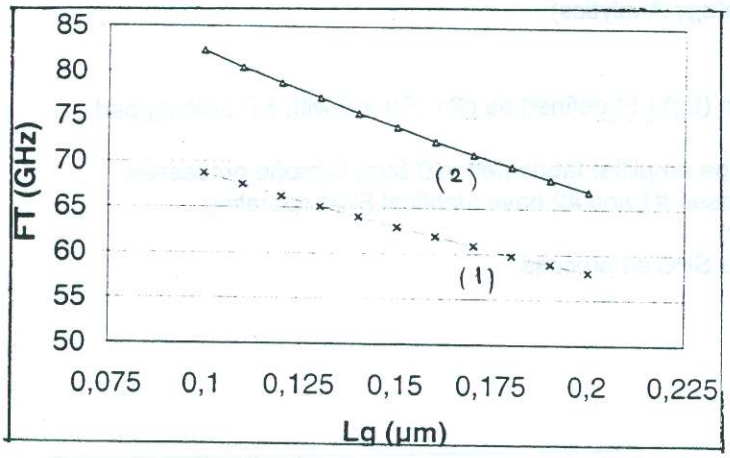

Figure 5

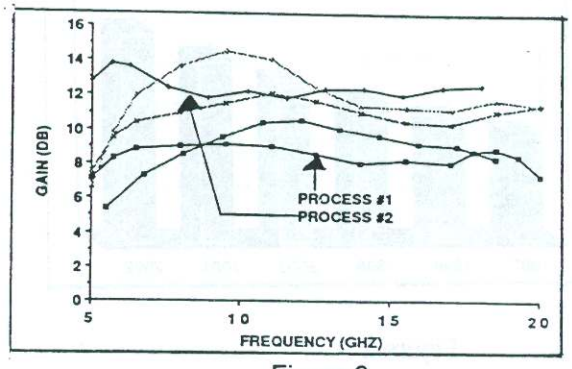

Figure 6

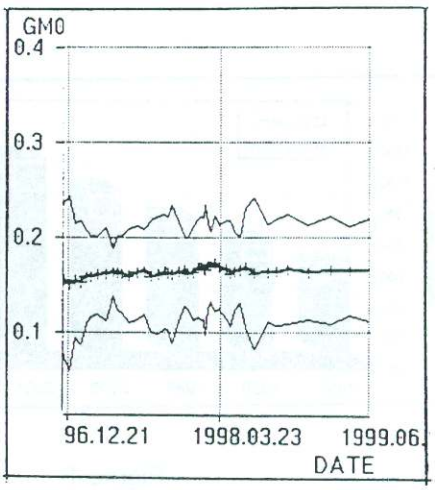

Figure 7