FET physics-based, MMIC yield analysis CAD tools and capabilities demonstrated within the EDGE project.

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BACKGROUND

EDGE is a programme of co-operation between small European enterprises involved with computer-aided design for high-speed circuits mainly in the compound semiconductor GaAs and its derivatives, but also in Si. The small enterprises involved are Barnard Microsystems (England), Jansen Microwave (Germany), GaAs Code (England), Talbot Technologies (Eire), with the University of Rome "Tor Vergata" fulfilling a special role as an associated partner. The initiative was set-up in 1995 and, from March 1996 to May 1998, was supported by the European Commission with participation of Dassault Electronique (France), GEC-Marconi Materials Technology (England) and Philips Microwave Limeil (France) as guides and evaluators.

One of the objectives of the formally funded phase was to evaluate a method of predicting the yield of self-biased microwave integrated circuits using a process-based FET simulator linked to a commercial circuit simulator - referred to as "Process-Linked Simulation and Yield Analysis". At its simplest, the idea is to forecast the yield of a complete circuit in terms of known variations in the technology of the active devices from which it is built, thereby to seek assurance that the circuit will be manufacturable.

THE METHOD AND ITS USE

The Basic Idea

The method hinges on a FET simulator, developed over many years prior to EDGE, called FETWin™. When linked to a linear circuit simulator programmed with a network description of an MMIC following the broad scheme of Figure 1, FETWin™ permits the response of the overall circuit to be simulated directly in terms of the particular FET process technology used to fabricate the MMIC, including production variations. Starting from a knowledge of process technology, the simulator calculates the dc characteristics of sub-micron gate length GaAs FETs together with the bias-dependence of the equivalent circuit elements, the scattering parameters, and the noise parameters.

Spreads in the FET's dc and microwave characteristics (as in the example of Figure 2) resulting from spreads in process technology are calculated and, when passed to the circuit simulator, allow the yield of MMICs manufactured using a real, toleranced, technology to be predicted.

Self-Biased Circuits

FETWin™ contains self-bias solvers for some commonly used single-FET and two-FET bias configurations, thereby extending the capability of commercial linear circuit simulators to self-biased circuits. Normally, linear circuit simulators are restricted to analysing circuits where the FET's microwave parameters (which are a function of bias point) are already known, as follows from assuming the FET operates at a known, fixed, bias point.

The FET simulator offers fast dc solvers for some common self-bias configurations, as for example in Figure 3. The self-bias solvers calculate the dc current and voltages at which each FET will

settle, and the simulator then evaluates all the FETs' microwave parameters at that bias point for passing to the circuit simulator. Further spreads in the FETs' microwave properties resulting from variations in supply voltage and bias network resistances are calculated in addition to those arising from technology spreads. The yield of a MMIC due to bias circuit variations, as well as technology, can be thus forecast.

Linking to Circuit Simulators

Prior to EDGE, FETWin™ had been linked only to MMICAD™, which is a linear circuit simulator from Optotek of Canada. During EDGE, the FET simulator was linked to Libra™ from HP-EEsof, WaveMaker™, from Barnard Microsystems, and LINMIC+/N™, from Jansen Microwave of Germany. Figure 4 gives an example of a yield calculation for a complete monolithic microwave integrated circuit (MMIC).

Obtaining the Technological Data

Process information can be made available in three ways:

(i) All readily measurable technological parameters (for instance, the doping profile, the gate length and recess depth) are determined, with spreads, by the foundry by direct measurement. Inaccessible parameters (such as the surface charge in the gate recess) are determined by seeking consistency between the electrical properties of FETs measured from the practical process and the electrical predictions of FETWin™ running the measured technological parameters. Subject to validation, the technological data is released by the foundry in encrypted form as part of the foundry library.

(ii) Indirect determination of the FETs' technological make-up may be made by analysing FET electrical data. Multi-bias *S*-parameters and noise parameters measured for several tens of FETs can be analysed to "reverse out" the process using a specially configured FET simulator.

(iii) Approximate process parameters can be derived using general knowledge of the process (for instance, that it is 0.5µm, ion-implanted), and by analysing a set of multi-bias *S*-parameters (and noise parameters if available) from a typical FET using the methods of (ii). Guessed spreads representative of the maturity of the process can be imposed on the nominal parameters thus deduced. Despite its apparent lack of rigour, this method has proved surprisingly useful.

Data for the F20 process of GEC-Marconi Materials Technology, which was the process used to manufacture the test circuit studied during EDGE, were compiled through the procedure of method (i) prior to EDGE, and the limits of validity of the FETWin™ simulator systematically established.

Applications

Applications of the method include

* generating more comprehensive FET data than a foundry provides for circuit design;
* designing microwave integrated circuits which use self-biased FETs;
* checking the design response of a circuit when the FETs it contains are "nominal FETs" i.e. FETs fabricated with the nominal parameters of the technology or process;
* predicting the yield of MMICs when manufactured by a process with known tolerances;

* improving the yield of MMICs by selecting a different bias point, a different bias method, a different size of FET, a different microwave circuit configuration, different circuit element values, or by systematically altering the spread in technological parameters.

Relationship to Other Methods of Yield Prediction

Circuit yields calculated by FETWin™ linked to a circuit simulator are predictions made directly from the uncontrolled variations in technology which are responsible for some circuits failing to meet specification. The method automatically generates and keeps all the essential correlations which arise between the electrical parameters of the active devices in the circuit - correlations which are lost in some yield forecasting schemes. Secondly, with commercial software from the major vendors, the yield of self-biased circuits has to be calculated using a non-linear simulator because linear simulators make no provision for bias-dependent device models. Most non-linear models do not reproduce small-signal *S*-parameters well, however, so the yield forecast may have in-built errors. Table 1 summarises the merits of the various methods for the main types of circuit.

Take-Up of the Method

Despite the potential of the yield prediction scheme to save waste and reduce costs, to date the take-up has been negligible. The method *has* been used by fabrication houses to modify existing processes in pursuit of higher yield or performance, but its application nevertheless has been narrow compared with that originally foreseen. It is seen by circuit designers, the largest group at which it is aimed, as a tool for foundry operators, not designers of circuits. Among the reasons given are a perceived lack of access to technological data; a shyness of anything vaguely related to physics; the promotion of circuit-based methods of yield analysis by major vendors of CAD software; an unceasing pressure to work on short-term objectives, which leaves no time to investigate anything new; a move to PHEMT technology, for which it is much more complicated (and time consuming) to develop a simulator to run at the necessary speed, and a need for a record of proved cases to convince people, which takes years to build. Finally, with today's large production runs, the relative overhead cost of finding answers by practical trial is small and therefore acceptable, although this could well change with more modern and contemporary circuits, especially for wireless application, where finding a manufacturable design may be impossible without sophisticated design tools.

WORK DONE DURING THE EDGE PROJECT

Dassault Electronique was the primary evaluator of the technique within the EDGE consortium. A four-stage low-noise amplifier (LNA), fabricated on GEC-Marconi Material Technology's F20 process, was chosen by Dassault as the circuit by which to evaluate the method. All four stages consist of self-biased FETs. The first and second stages are biased at approximately $I_{DSS}/5$, each using a 110Ω resistor in the source as a self-bias resistor. The third and fourth stages are biased at approximately $I_{DSS}/2$, each using a 32Ω resistor in the source as a self-bias resistor. A circuit using a cascade of self-biased stages was viewed as a critical test of the accuracy of the FET simulator and its in-built self-bias solvers, particularly given two stages biased at low current where previous work had already suggested the simulator's accuracy might need to be improved.

Although a general bias solver is available to solve for the bias condition of a circuit of arbitrary configuration, a higher speed of execution as needed for yield analysis can be achieved by developing bias solvers specific to a given circuit configuration. Accordingly, a new bias solver for the four-stage self-biased circuit was developed and implemented in FETWin™.

The first simulations were undertaken by Dassault with the F20 technological data as far was known from programmes prior to EDGE, none of which had tested the data and simulator as

stringently as the Dassault circuit. Extremely disappointing results were obtained: whereas the gain of practical MMICs had been 27dB to 30dB, the linked simulators predicted 18dB to 21dB.

The fault was traced to two main factors: first, the ***slope*** of the intrinsic transconductance with respect to the gate-source voltage, dg_{m0}/dV_{GS}, was found to be too low relative to practice by about 15% (it can be shown that the transconductance at a given drain current bias is proportional to dg_{m0}/dV_{GS}). Secondly, the drain-source resistance R_{ds} was too small by about 20%. Between them, these two factors were wholly responsible for the error in the predicted gain of the overall circuit, serving to illustrate graphically the *extraordinarily high accuracy necessary in a device simulator's results at all bias points if anything like acceptable representation of a real circuit's behaviour is to be achieved.* Bear in mind that we are here talking about the ***slope*** of the intrinsic transconductance with respect to the gate-source voltage in the low-current region where the current is flowing in the tail of the doping profile.

A complete cure of the deficiencies in the FET simulator as revealed by Dassault's first work on the four-stage circuit was effected through two changes:

(i) the ion-implantation profile was altered to remove the flowing tail of the measured profile which was originally taken to be a result of ion channelling but is now understood to be an artefact of the profile measuring method;

(ii) the dc current-voltage characteristics of the FET are calculated as a transform of the large-signal RF $I(V)$ characteristics the FET simulator primarily calculates, rather than calculating the dc characteristics from an approximate boundary condition. (Even after the twenty-five years the GaAs FET has been with us in some volume, there is still not a widespread appreciation of just how complicated is the set of processes which give rise to the dc characteristics.)

Results for all these cases will be given during the spoken presentation.

CONCLUSION

Although the deficiencies in FETWin™ as it stood prior to EDGE were known, their seriousness for certain types of commonplace, almost classical, microwave circuit was not apparent. Dassault's choice of circuit has led not only to useful and unexpected improvements in the FET simulator but also to a more detailed understanding of how various features of the doping profile affect the bias dependence of the microwave parameter functions the simulator predicts.

Task	Linear Circuit Simulator	Non-Linear Circuit Simulator	Physics-based FET Simulator and Circuit Simulator
Yield prediction of linear, truly VOLTAGE-biased, circuits	✓ (must use "data-base" sampling)	✓ (must use "Truth" model)	✓ avoids need for voluminous S2P measurements
Design of SELF-BIASED linear circuits	×	Poor accuracy in bias-dependent reactive parts & may be in current parts	✓ (needs improving in g_{m0} at low V_{DS} and low I_D)
Yield prediction of SELF-BIASED linear circuits	×	×	✓
Yield improvement of SELF-BIASED linear circuits	×	×	✓

Table 1. *Comparison of methods of yield prediction*

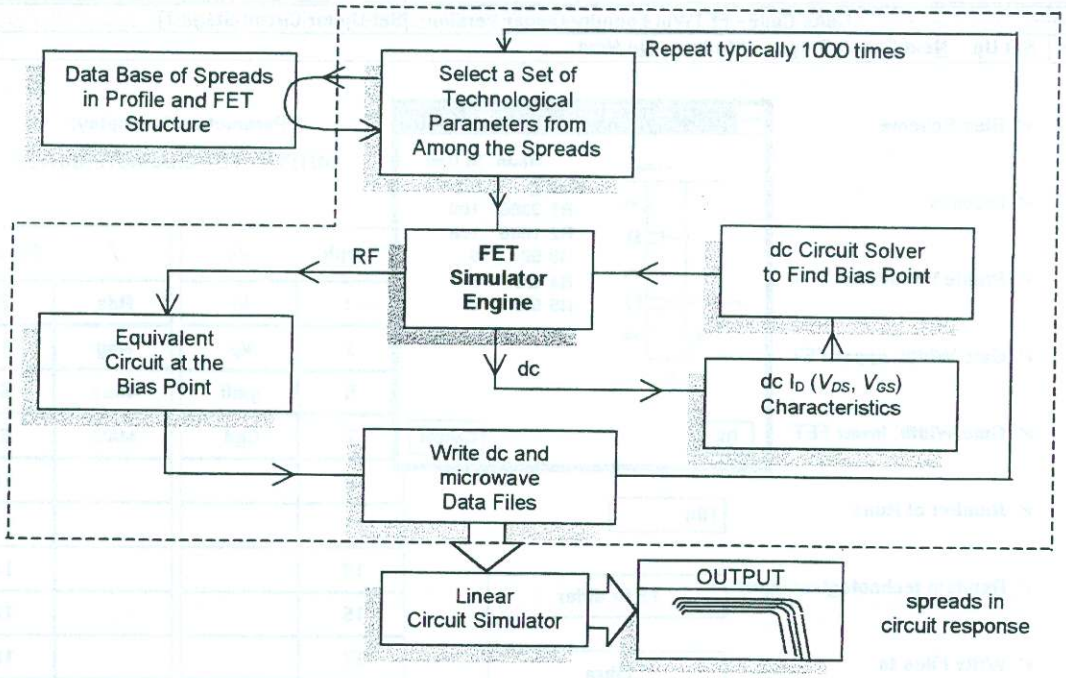

Fig. 1: The functioning of FETWin™ linked to a linear circuit simulator

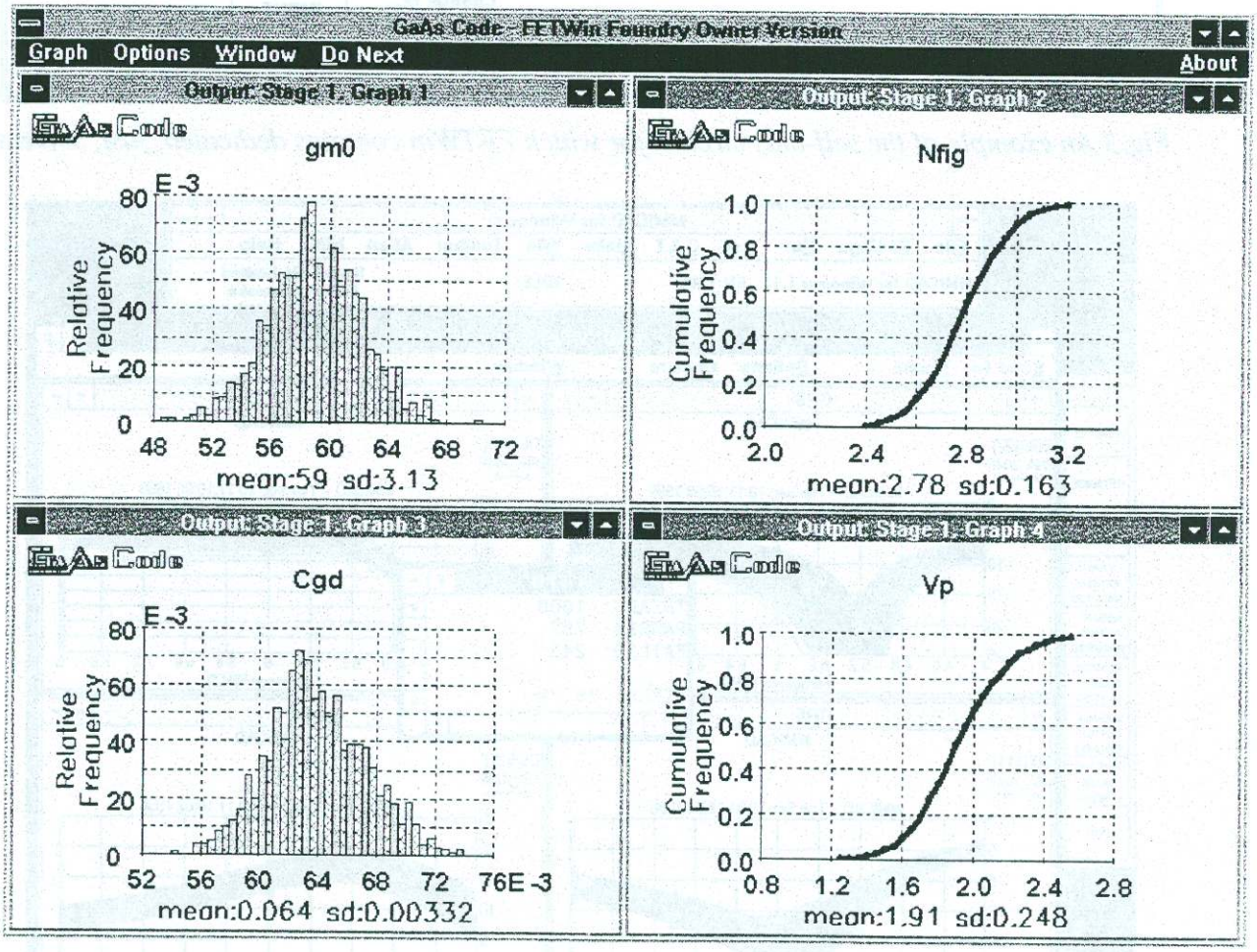

Fig. 2: FETWin-calculated histograms of transconductance and gate-drain capacitance, and cumulative distributions of noise figure and pinch-off voltage, resulting from variations in manufacturing technology for a 0.5μm FET biased at $0.5I_{DSS}$.

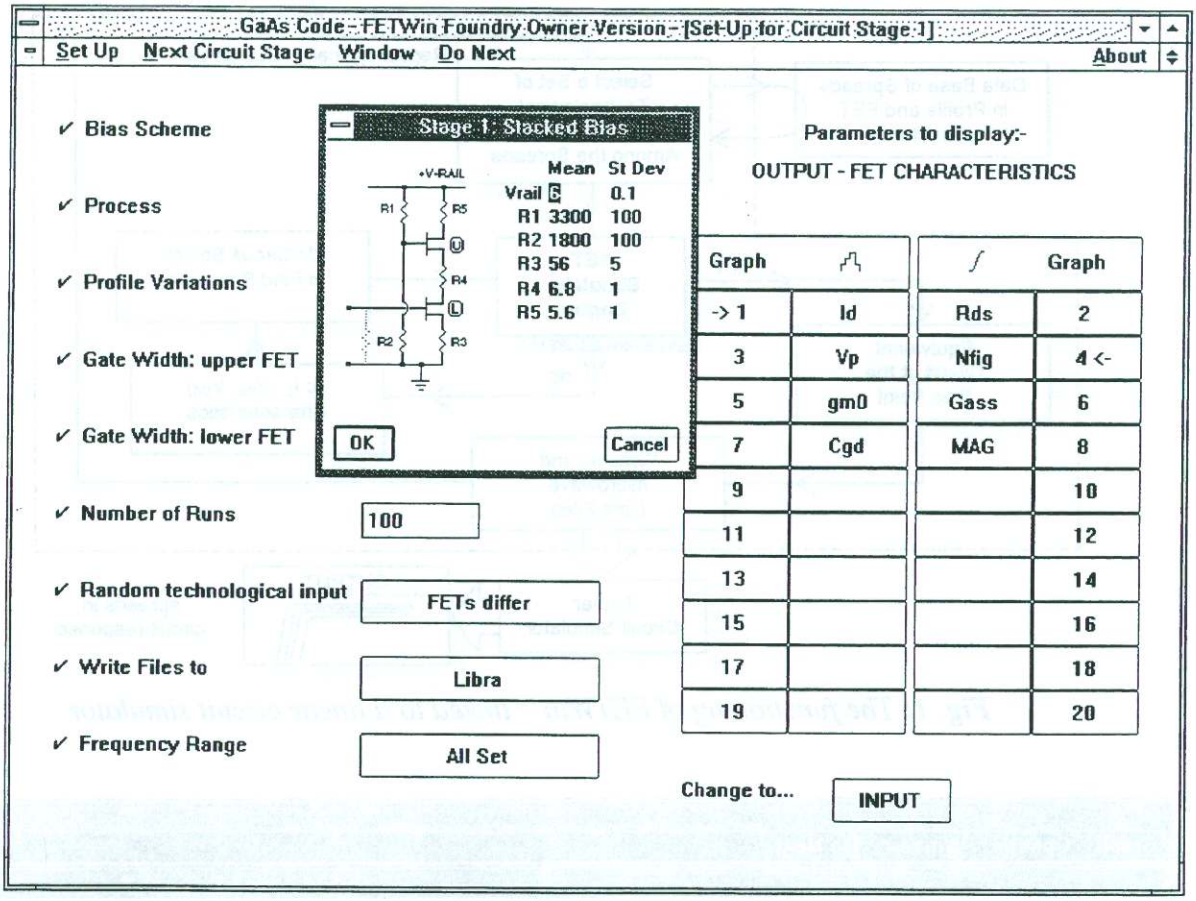

Fig.3 An example of the self-bias circuits for which FETWin contains dedicated, fast, solvers.

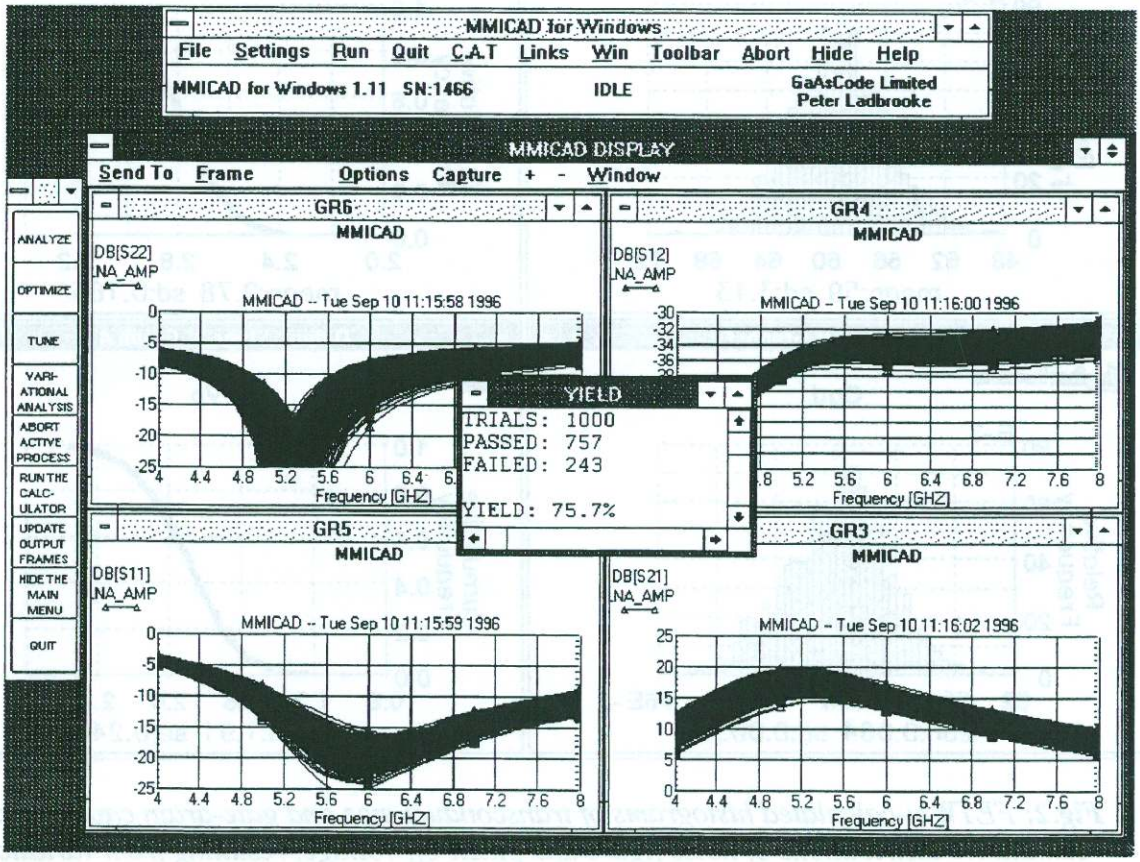

Fig.4 Yield of a 0.5μm FET-based MMIC as calculated by FETWin and MMICAD.