Optimised Thermal and Microwave Packaging for Wide-Band Gap transistors : Diamond & flip chip

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***Abstract* — Wide-band gap (WBG) transistors give a real breakthrough for power devices compared to Silicon (Si) and Gallium Arsenide (GaAs) components. However, for space applications, the high power density of WBG transistors makes the thermal management critical and requires thermal investigations. Some packaging solutions dedicated to those power transistors are presented in this paper. The focus is made on diamond-based packaging with two topologies. In the first one, the die is soldered on a diamond carrier. In the second one, it is flip chip bonded on a diamond circuit. Thermal simulations, thermal cycling and electrical measurement results are given for both configurations.**

I. Introduction

As wide band gap Thales transistors begin to appear in space power applications, packaging must be thought differently. For Gallium Nitride/Silicon Carbide (GaN/SiC) HEMT 0.9mm transistors, power density goes up to 4W/mm which means that one transistor dissipates from 10 to 30W. The use of such power dice is simply impossible without the right packaging. Usual solutions do not have enough thermal conductivity. Other materials or packaging must therefore be identified.

There are some active thermal management possibilities such as heat-pipes and some passive thermal management ideas with very dissipative substrates such as diamond. This leads to very challenging packaging solutions as they are not so easy to implement.

We will focus on a passive solution based on diamond, with two packaging configurations. In the first one, components are soldered on a diamond carrier. Microwave connections are performed through wire bonding. In the second case, dice are flip chip bonded on a diamond circuit. Both solutions will be presented with associated thermal simulation, thermal cycling and electrical measurement results.

We will finally see how those high power component maximum frequency is limited by their source connection to ground. With a flip chip assembly, via hole implementation in diamond could help increase this maximum operating frequency.

II. Thermal Dissipation

Thermal management can be either passive or active.

Active one can be based on micro-fluidic components or micro-machined heat-pipes [2][3]. This is a valuable alternative or complement to passive solutions.

Passive thermal management is the easiest to implement as it is based on material or package intrinsic thermal characteristics. A compromise must be found between thermal conductivity and mechanical properties such as the Coefficient of Thermal Expansion (CTE). On Fig.1, the grey zone stands for the main semiconductor material CTE domain, that is 4-7ppm/°C. Composite materials are very attractive as some of them have good thermal conductivity and matched CTE.

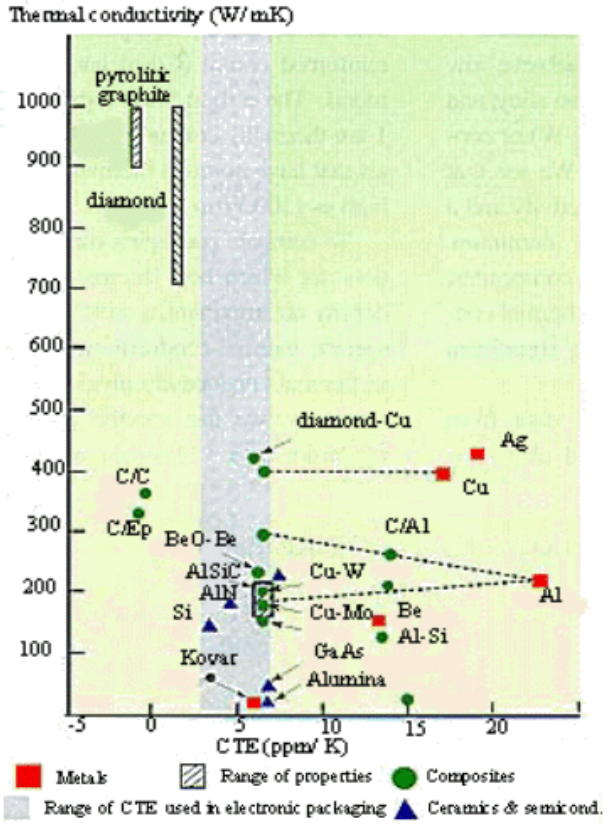

Fig. 1. Materials thermal conductivity vs. CTE [1]

Diamond and pyrolitic graphite are highly interesting for their very good thermal conductivity (only in plane for pyrolitic graphite). But their CTE is low, which will make assembly delicate. Finally, non composite or more standard materials such as Copper Tungsten (CuW), Silicon or Aluminum Nitride (AlN) will have to be completed by an active thermal system to reach equivalent thermal performances.

We decided to focus on passive management first and we chose diamond for it is a very promising material.

A. Two possible topologies with diamond

Diamond is of great interest as it can be used either as a carrier or as a RF circuit. The TRT GaN/SiC components we used have RF and thermal bumps. Therefore they can be active face-up mounted as it is usually made with soldering and wire bonding steps. Diamond is then a simple thermal carrier. Or they can be flip chip mounted and then, diamond is an RF circuit.

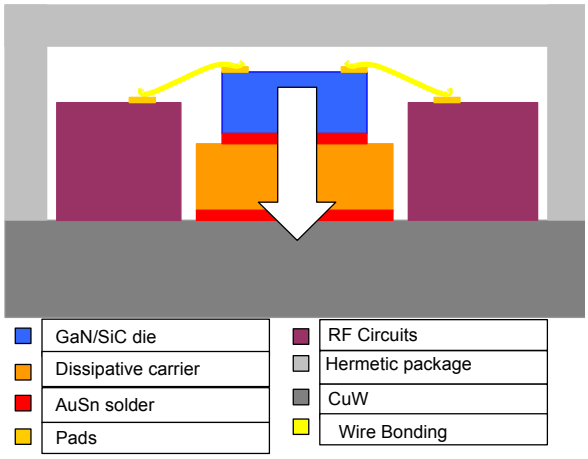

Fig. 2. Active face-up mounting (wire bonding) topology

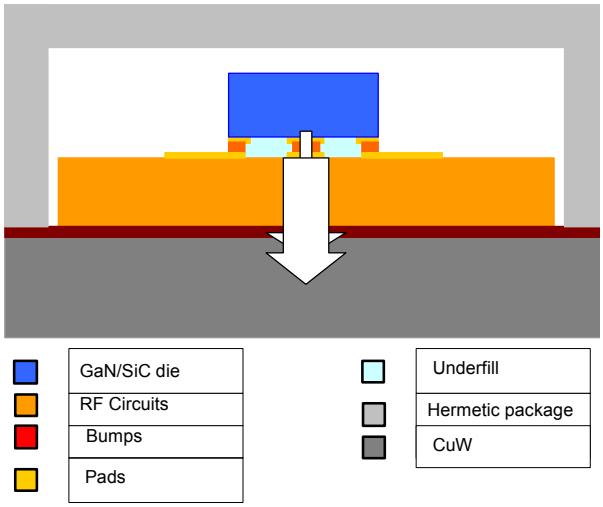

Fig. 3. Flip Chip assembly topology

Several assemblies were realised for both topologies with diamond. This paper mainly focuses on the flip chip one.

B. Flip chip first reliability piece of information

A few transistors were flip chip mounted on a diamond circuit with usual thermo-compression parameters.

Fig. 4. Flip Chip assembly of a GaN transistor on diamond substrate

Visual or Scanning Acoustic Microscopy (SAM) inspection and electrical measurements were done after assembly and after 500 thermal cycles [-55;+125°C]. No default has been noticed. Measurement results are given on Fig. 5. Although CTE is around 4.5ppm/°C for SiC and only 1.5ppm/°C for diamond, there was no failure. This is certainly due to the die small dimensions (1.5 x 2mm²).

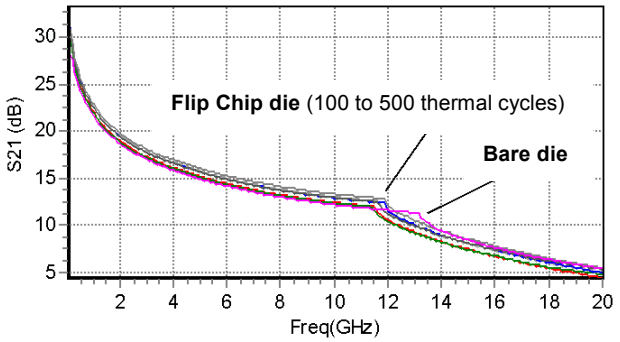

Fig. 5. GaN transistor measurement before and after flip chip (and thermal cycles)

C. Thermal Simulations

Concerning thermal point of view, first simulation results are presented in Table 1 for TRT GaN/SiC transistors. They show that a face-up assembly on a diamond carrier is more thermally effective than a flip chip assembly. And the larger the carrier the lower the junction temperature. Flip Chip assembly on AlN substrate was simulated as this material is commonly used in microelectronics. Thin-film technology with metallized holes is mature on AlN. This is not the case of diamond. But as said before, AlN does not have high enough thermal conductivity for such high power components.

	Conf 1	Conf 2	Conf 3	Conf 4
Assembly	Soldering	Soldering	Flip Chip	Flip Chip
Carrier	Diamond	Diamond	No carrier	Diamond
Carrier Thickness	300µm	300 µm	-	500 µm
Carrier dimensions	1.2 x 9 mm	9.0 x 18 mm	-	9.0 x 18 mm
Micro package (thickness)	CuW (1mm)	CuW (1mm)	AlN (1.5mm)	CuW (1mm)
Junction T°	**165 °C**	**155 °C**	**235 °C**	**190 °C**

TABLE I
SUMMARY OF THERMAL SIMULATION RESULTS
CONTINUOUS WAVE CONDITIONS WITH 70°C BASE PLATE T°

So active face-up mounting seems more interesting than flip chip assembly for thermal considerations. This is mainly due to the role of the SiC substrate in the die. Its thermal conductivity is quite high (400–500W/mK). So it plays a big role in a conventional configuration while it is not used in a flip chip assembly as heat does not go much through it.

Further simulations must be done in order to find the optimised configuration for flip chip assembly (via position and distance from transistor source…). Recent results show that diamond thickness influence on junction temperature is quite negligible (with 200µm thick diamond instead of 300µm). But a thinner substrate is highly interesting on the electrical point of view.

Then if we pay attention to electrical performances, flip chip could be more interesting than face-up mounting as it allows higher frequency response and bandwidth.

III. REACHING HIGHER FREQUENCIES

A. Electrical Simulations

ADS simulations given on Fig. 6 show that those component frequency bandwidth is limited by the source connection to ground. The more inductive this connection the lower the maximum operating frequency.

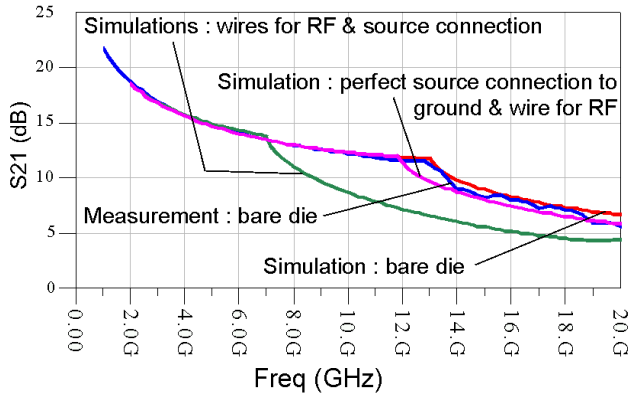

Fig. 6. GaN transistor simulation depending on source connection to ground

Those GaN/SiC components could operate up to 12GHz. But they do not have via holes. So when face-up mounted on a diamond carrier with microstrip accesses made on alumina circuits, the transistor source must be connected to micro-package ground with a lot of wires. Because of those wire high inductive effect, this upper frequency limit drops to 8GHz.

Flip chip assembly on diamond circuit could solve the problem if there are metallized holes in the diamond. Otherwise there would be many wires between the source and the ground also, and the inductive effect would remain the same.

HFSS 3D electromagnetic simulations were performed on the half-structures shown on Fig. 7. We made a comparison between two flip chip topology. The reference one has no hole in diamond. Source is then connected to the ground with several wires. On the other hand, studied solutions have one, two…holes in diamond for ground connection.

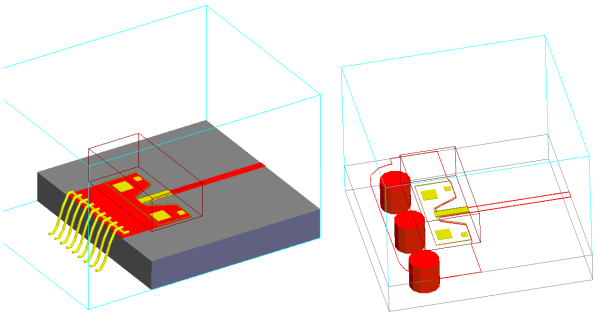

Fig. 7. ½ structure HFSS simulation for the inductive effect optimisation

Two or three metallized holes made in the diamond circuit on each side of the transistor would provide a 40% reduction of the inductance between source and ground. Misaligned holes could even give a 50% inductance reduction. And of course, the thinner the diamond the better for inductance reduction.

Considering those promising simulation results, a few diamond circuits with metallized holes had to be fabricated.

B. Diamond circuit fabrication

Metallized holes associated to thin film technology is not an easy task with substrates such as diamond. Several attempts have been made without success but some recent ones were encouraging, as shown on Fig. 8. It depicts a good-quality hole without residue and with an homogenous shape. Furthermore, thin film has been performed on diamond with success.

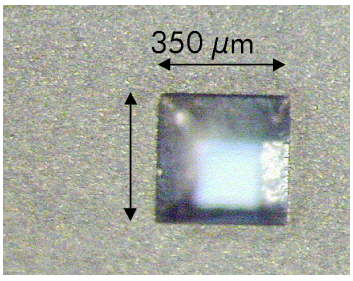

Fig. 8. Via hole in diamond substrate

So complete thin film technology with metallized holes was almost ready. The whole process has been recently performed with excellent results on a 300µm thick diamond substrate. Fig. 9 shows some photos of one diamond circuit made for GaN flip-chip assembly. Those holes were laser drilled without any problem. Their diameter is 350µm diameter on diamond top face and 220µm on back face. Their sides are very regular, clean and smooth. And there was no difficulty performing thin film metallization on diamond and in those holes.

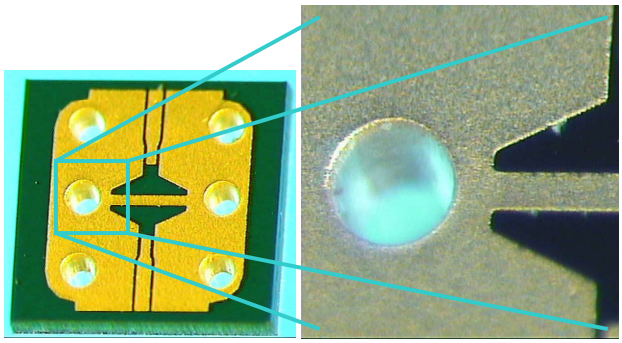

Fig. 9. Via hole in diamond substrate

C. Measurements

Hole position and quantity have been optimised with HFSS. The sample shown on Fig. 9 and 10 is one of the simulated configuration. A few GaN transistors have been flip-chip mounted on these circuits.

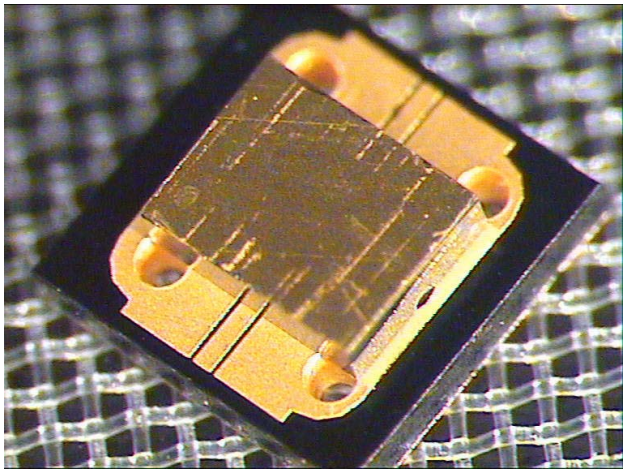

Fig.10. GaN transistor flip chip mounted on diamond circuit with metallized holes

Measurement results are given on Fig. 11. This graph shows one stand-alone transistor performances, one wire-bonded version and the recent flip chip version. All modules were glued on a CuW heat sink. As expected with ADS and HFSS simulations, the frequency limit is pushed forward thanks to flip chip and holes in diamond circuit. It does not reach the transistor performances but it is better than the wire-bonded configuration with a 2.5 to 3 GHz frequency step.

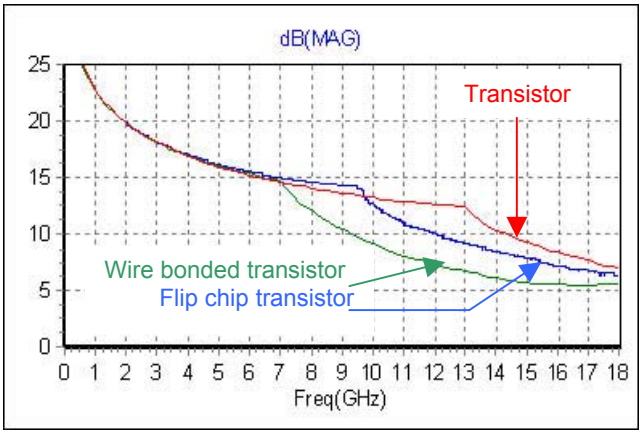

Fig. 11. GaN/SiC transistor gain measurement

IV. Conclusion

Wide-band gap is a challenging technology as dissipated power is much higher than it is with GaAs transistors. Packaging must be different and even audacious, otherwise the transistors can not give their best. Diamond has such a high thermal conductivity that we decided to replace the CuW carrier with it, even if it makes assembly a bit more delicate to perform because of its mechanical properties. Active face-up assembly of SiC/GaN dice on a diamond carrier is more thermally efficient than flip chip assembly on a diamond circuit. But on the other hand, frequency bandwidth is today strongly reduced with a face-up mounting because of the lack of via holes at die level. Flip chip and metallized holes in diamond can push this frequency limit higher. One must then make a choice between higher temperature dissipation and higher operating frequency.

Finally, another advantage for flip chip technique is that the SiC substrate does not matter. It could be Sapphire or Silicon instead of SiC and the thermal result would not be much different. Then flip chip can play an even bigger role for easier or cheaper GaN processes.

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