Development and Verification of a Non-Linear Look-Up Table Model for RF Silicon BJTs

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This work presents, for the first time, a large-signal look-up table based model for the forward-active region of RF Si BJTs. The state functions are obtained by integrating the device's bias-dependent intrinsic elements, extracted from de-embedded multi-bias S-parameter measurements. The model accuracy is evaluated using vectorial large-signal measurements.

INTRODUCTION

The large-signal state-space model concept, introduced in Root *et al.* (1), has been successfully applied to the non-linear analysis of various types of FET transistors, e.g., MOSFET by Vandamme *et al.* (2) or HEMT in (1) and Schreurs *et al*. (3). Compared to compact models, this model type has many advantages, among which the measurement-based, straightforward parameter extraction using only one device geometry can be highlighted. Despite these advantages, the elaboration of this modelling concept, according to our knowledge, has not been reported yet for RF bipolar transistors. In this work, for the first time, a non-linear look-up table based model for Si BJTs has been developed and verified.
The next section outlines the small-signal equivalent circuit extraction procedure, needed for non-linear model generation. Then, a proper large-signal look-up table based model for Si BJTs is introduced in the consecutive section. Finally in the last section, the model is verified using the recently available vectorial large-signal measurements.

SMALL-SIGNAL EXTRACTION

The large-signal model identification method, proposed here, starts from extracting the small-signal parameters of the hybrid-Π equivalent circuit, depicted in Fig. 1, from multi-bias S-parameter measurements. The equivalent circuit is composed of bias independent extrinsic elements laying outside, and bias dependent intrinsic ones laying inside the dotted line rectangular.

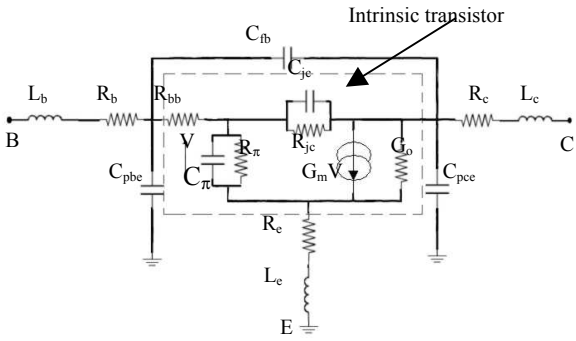


Figure 1: Hybrid–Π small-signal equivalent circuit of BJT.

The framework of the small-signal extraction procedure is based on the full analytical method introduced by Belquin *et al*. (4) and consists of the following steps:

1. S-parameters measurements of the transistor in various bias conditions,
2. De-embedding of the contact pads and the access metal interconnections,
3. Extraction of series and then parallel extrinsic elements,
4. Identification of intrinsic transistor elements.

The measurement control, data acquisition and the small-signal extraction were implemented in Agilent-IC-CAP. Basing on S-parameter measurements of the open and short dummy structures, available on the same silicon wafer, the de-embedding method was applied prior to the direct extraction procedures. These procedures involved S-parameter measurements of the transistor in specific bias conditions.

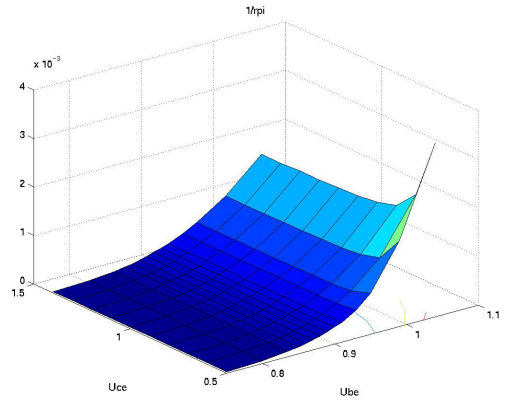


Figure 2: Extracted intrinsic transistor $1/R_\pi$ [S], parameter values in the forward-active bias region.

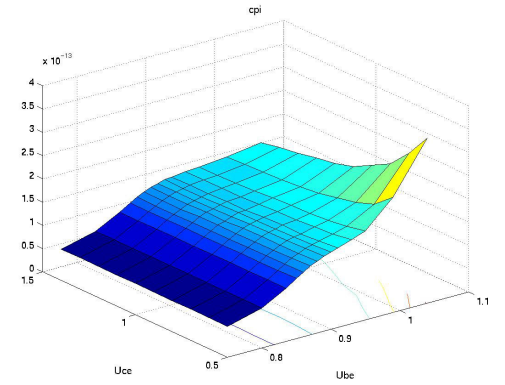


Figure 3: Extracted intrinsic transistor C_π [F] parameter values in the forward-active bias region.

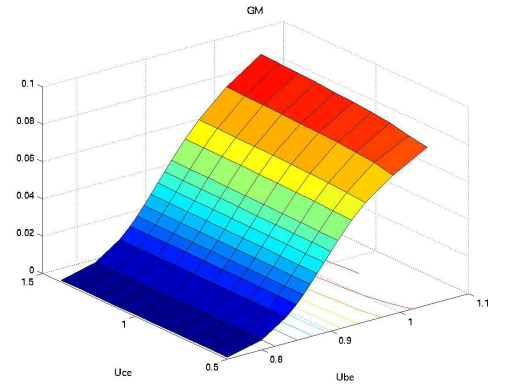


Figure 4: Extracted intrinsic transistor G_m [S] parameter values in the forward-active bias region.

A logarithmic frequency scale has been used to provide more measurement points in the lower frequency range, where most elements are being extracted. The extraction resulted in values for the extrinsic elements and in a set of values for the bias dependent intrinsic elements.
For an NPN 0.8x20 μm BJT, fabricated by IMEC, we determined typical values of series and parallel extrinsic elements as follows: R_b=3.39 Ω, R_c=2.59 Ω, R_e=9.13 Ω, C_{fb}=16.26 fF, C_{pce}=33.33 fF. It should be noted that the values of C_{pbe}, L_b and L_c revealed to be very small or even negative over a significant frequency range and this may result from subtracting their influence during the de-embedding step. As an example of the bias dependent parameters, $1/R_\pi$, C_π, and g_m are presented in Figs. 2, 3 and 4, respectively. The shown surfaces are limited to the BJT's forward-active mode, being the operation conditions mostly utilised in RF circuit applications.

LARGE-SIGNAL MODEL

We assume the large-signal model topology of the intrinsic transistor as shown in Fig. 5. Voltage-controlled current and charge sources represent the non-linear dynamic properties of the modelled transistor and are referred to as the device's state functions.

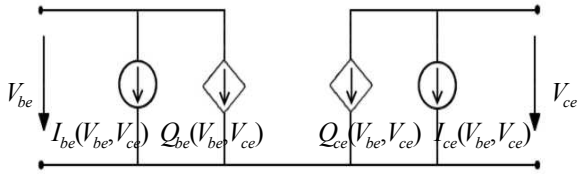


Figure 5: Intrinsic large-signal state-space model.

The state functions depend on the instantaneous values of the intrinsic V_{be} and V_{ce} voltages and can be determined from the bias dependency of the extracted intrinsic elements. For this purpose, the current $I(V_{be},V_{ce})$ and charge $Q(V_{be},V_{ce})$ state functions are calculated as the path-independent contour integrals:

$$I_{be}(V_{be},V_{ce}) = I_{be}(V_{be0},V_{ce0}) + \int_{V_{be0}}^{V_{be}} \mathrm{Re}\{Y_{11}(V,V_{ce0})\}dV + \int_{V_{ce0}}^{V_{ce}} \mathrm{Re}\{Y_{12}(V_{be},V)\}dV \quad (1)$$

$$Q_{be}(V_{be},V_{ce}) = \int_{V_{be0}}^{V_{be}} \frac{\mathrm{Im}\{Y_{11}(V,V_{ce0})\}dV}{2\pi f} + \int_{V_{ce0}}^{V_{ce}} \frac{\mathrm{Im}\{Y_{12}(V_{be},V)\}dV}{2\pi f} \quad (2)$$

$$I_{ce}(V_{be},V_{ce}) = I_{ce}(V_{be0},V_{ce0}) + \int_{V_{be0}}^{V_{be}} \mathrm{Re}\{Y_{21}(V,V_{ce0})\}dV + \int_{V_{ce0}}^{V_{ce}} \mathrm{Re}\{Y_{22}(V_{be},V)\}dV \quad (3)$$

$$Q_{ce}(V_{be},V_{ce}) = \int_{V_{be0}}^{V_{be}} \frac{\mathrm{Im}\{Y_{21}(V,V_{ce0})\}dV}{2\pi f} + \int_{V_{ce0}}^{V_{ce}} \frac{\mathrm{Im}\{Y_{22}(V_{be},V)\}dV}{2\pi f} \quad (4)$$

where Y_{xx} and Y_{xy} represent the intrinsic transistor's admittance matrix parameters given by:

$$Y_{\mathrm{int}} = \begin{bmatrix} G_\pi + G_{jc} + j\omega(C_\pi + C_{jc}) & -G_{jc} - j\omega C_{jc} \\ g_m e^{-j\omega\tau} - G_{jc} - j\omega C_{jc} & G_o + G_{jc} + j\omega C_{jc} \end{bmatrix} \quad (5)$$

V_{be0} and V_{ce0} used in equations 1-4 indicate transistor's DC condition and determine the starting point of integration.

Consequently, the state functions $I(V_{be},V_{ce})$ and $Q(V_{be},V_{ce})$ are obtained in the form of look-up tables with values referred to all V_{be} and V_{ce} voltages within the considered working range (see Fig. 6 for Q_{ce} and Fig. 7 for I_{ce}).

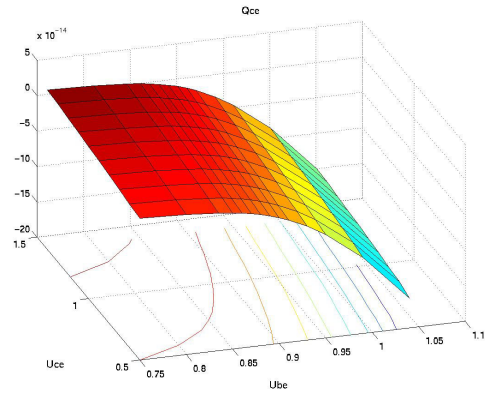


Figure 6: Calculated state function Q_{ce} [C].

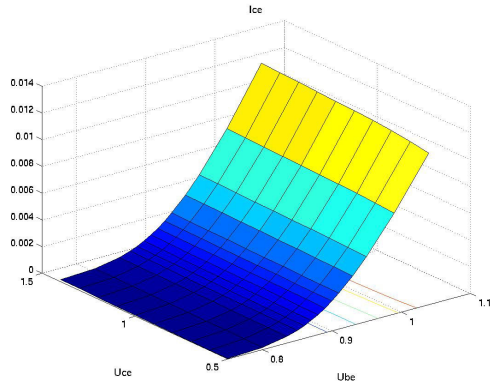


Figure 7: Calculated state function I_{ce} [A].

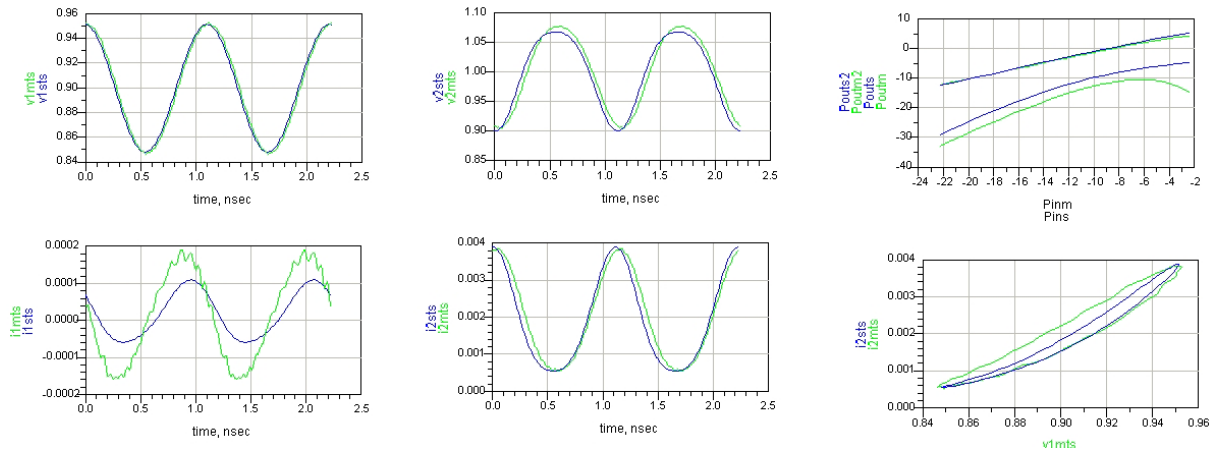
The complete large-signal model of the transistor is then obtained by embedding the intrinsic non-linear equivalent circuit from Fig. 5 into the extrinsic element network shown in Fig. 1 to account for the influence of the transistor's contact pad structure. For numerical simulations, such a model was implemented in ADS2001 of Agilent as a Symbolically Defined Device.

VERIFICATION

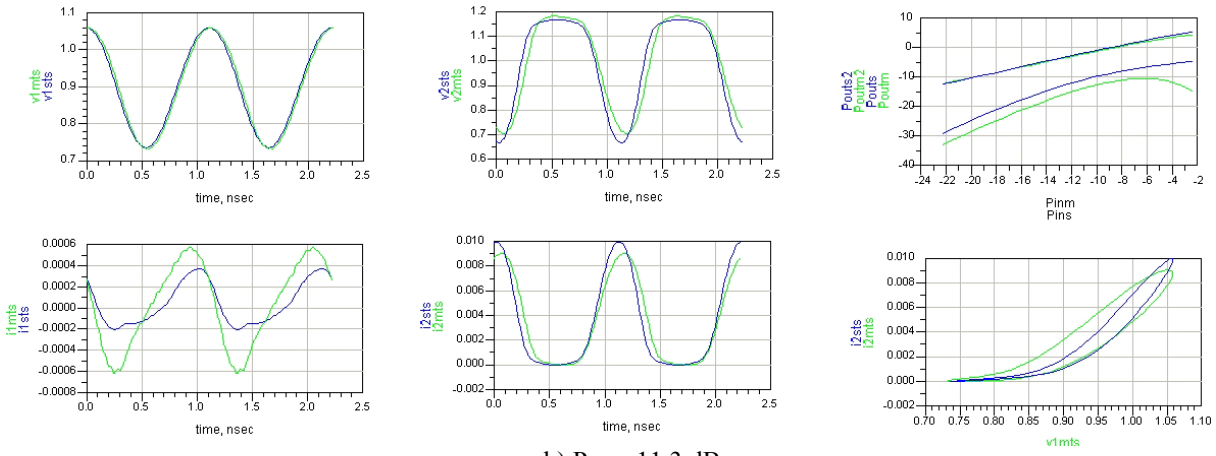
In order to verify the model, a large-signal power-swept measurement at 0.9 GHz was performed using a unique measurement set-up (Verspecht *et al.* (5)). The bias point was selected in the middle of the forward-active region. Fig. 8 shows results of harmonic balance simulations and experimental measurements for two input power levels. As one may notice, agreement of the traces is better for the dominant non-linearity in I_{ce} than for the smaller one in I_{be}. Moreover, good agreement is achieved as long as the measured instantaneous values of V_{be} and V_{ce} are within the considered operating region that was used in the calculations in the previous section. This is due to limited extrapolation capability of the model, a well-known drawback of look-up table models.

CONCLUSIONS

In this work, we presented for the first time the procedure for the identification of a large-signal look-up table based model for RF Si BJTs. This approach has been validated in the forward-active bias region of the transistor using large-signal measurements.



a) P_{in}= –21.3 dBm.



b) P_{in}= –11.3 dBm.

Figure 8: Experimental data (light color) and simulation results (dark color) for input (left) and output (center) voltage (top) and current (bottom) time series, respectively. Fundamental and second harmonic levels vs. input power (top right). Collector current vs. V_{be} voltage (bottom right). The DC bias condition is: V_{be}= 0.9 V, V_{ce}= 1 V and the fundamental frequency is 900 MHz.

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