A 0.18-µm 2.4~6GHz CMOS Broadband Differential LNA For WLAN and UWB Receiver

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Abstract — **A 2.4-6 GHz broadband CMOS differential LNA for WLAN and UWB receiver is presented. The LNA is fabricated with the 0.18 µm 1P6M standard CMOS process. Measurement of the chip is performed on a FR-4 PCB test fixture. In the UWB low-band (3 to 5.15GHz), the broadband LNA exhibit a gain of 17.5-18.2 dB, noise figure of 3.4-5dB, input/output return loss better than 10 dB, and input P_{1dB} of –17 dBm, respectively. In the band from 2.4 to 3GHz (covering a 802.11b/g band), the LNA exhibit a gain of 17.5-18dB and noise figure less than 3.5dB. From 5.2 to 6GHz, the noise figure of the LNA becomes higher than 5 dB. The gain also decrease to about 15 dB. The DC supply is 1.8V.**

I. INTRODUCTION

Ultra Wideband (UWB) radio [1][2] is originally the technology of transmitting and receiving short, information-encoded, electromagnetic impulses. The large occupied bandwidth (3-5.15 GHz or 3-10.1 GHz) enables UWB networks with exceptionally large capacities in higher bandwidth communications. UWB is a power limited technology because the emissions are targeted to be below the emission levels currently allowed for unintentional emitters. Consequently, UWB will coexist with and overlay existing narrow band radio services while causing nearly imperceptible changes in the noise floor of those receivers. UWB thus opens a new spectrum and new combinations of capabilities for solving the demands of an increasingly wireless world. More over, UWB transmissions can be designed to coexist fully with deployed wireless systems like IEEE 802.11a/b/g, GSM and PCS. Fig. 1. shows the spectrum allocation of the current UWB system for multiband OFDM (MBOA) group A (with 802.11/a/b/g) and direct sequence (DS) CDMA UWB. The MBOA group A covering from 3 to 5 GHz has three bands and each with a bandwidth of 500MHz. The DS-UWB system has a low band from 3.1 to 5.15GHz and a high band 6 to 10.1GHz.

Several UWB single-ended low noise amplifiers have been reported by SiGe or CMOS technology [3][4]. It is known that the differential circuit topology can mitigate the effects of common mode noise and clock feed-through. The UWB LNA with a differential circuit topology is not reported yet. This paper presents a 2.4-6 GHz CMOS broadband differential LNA which can be used for UWB low-band (3~5.15GHz) and 2.4-GHz 802.11b/g WLAN receiver application. The LNA is fabricated in a TSMC 0.18-µm standard CMOS process.

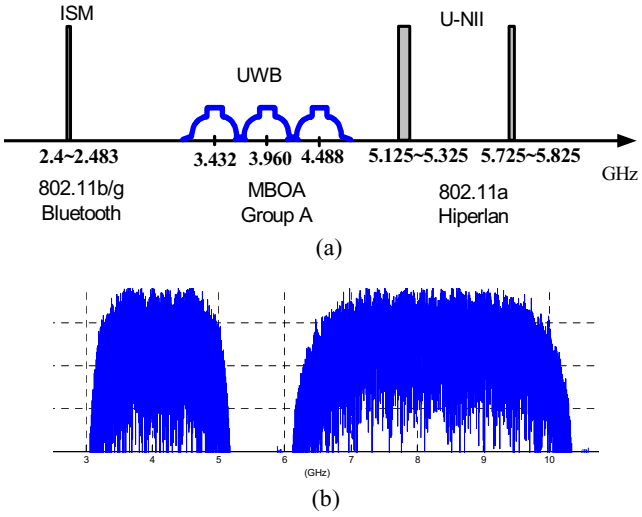

Fig. 1. Spectrum allocataion for UWB communication: (a) MBOA group A (with IEEE 802.11/a/b/g), (b) DS-CDMA.

II. CIRCUIT DESIGN

Fig. 2. shows the circuit schematic of a three-stage broadband CMOS differential LNA. From [5][6] we can know the sources of noise and how to determine the gate width of the first stage transistor. Under power consumption limit, the chosen gate width of the first stage transistor is 150µm (60 x 2.5 x 0.18µm). The design of the 2nd and 3rd stage amplifier mainly consider the linearlity. Hence, the chosen gate width of the 2nd stage transistor is 70 µm (28x2.5x0.18 µm) and that of the 3rd stage transistor is 50µm (25x2.5x0.18 µm). For the broadband design, instead of using the inductance and capacitance, the inter-stage matching should utilize the direct coupling. The 1st and 2nd stage use the inductive load to achieve the broad bandwidth and high gain. The 3rd stage use the resistive load to achieve a good output return loss. A good input return loss for wideband frequency range is achieved by using the negative feedback from the 2nd to 1st stage. The transistor Q_f provides a DC bias to 1st stage. The feedback resistance R_f is mainly to shunt the input impedance of M_1 to perform a wideband input matching. The diode connected the NMOS transistor M_f is for frequency response extension and to supply the gate bias of transistor M_1 [7]. Also, the virtual ground of V_{dd} is to perform the gain flatness.

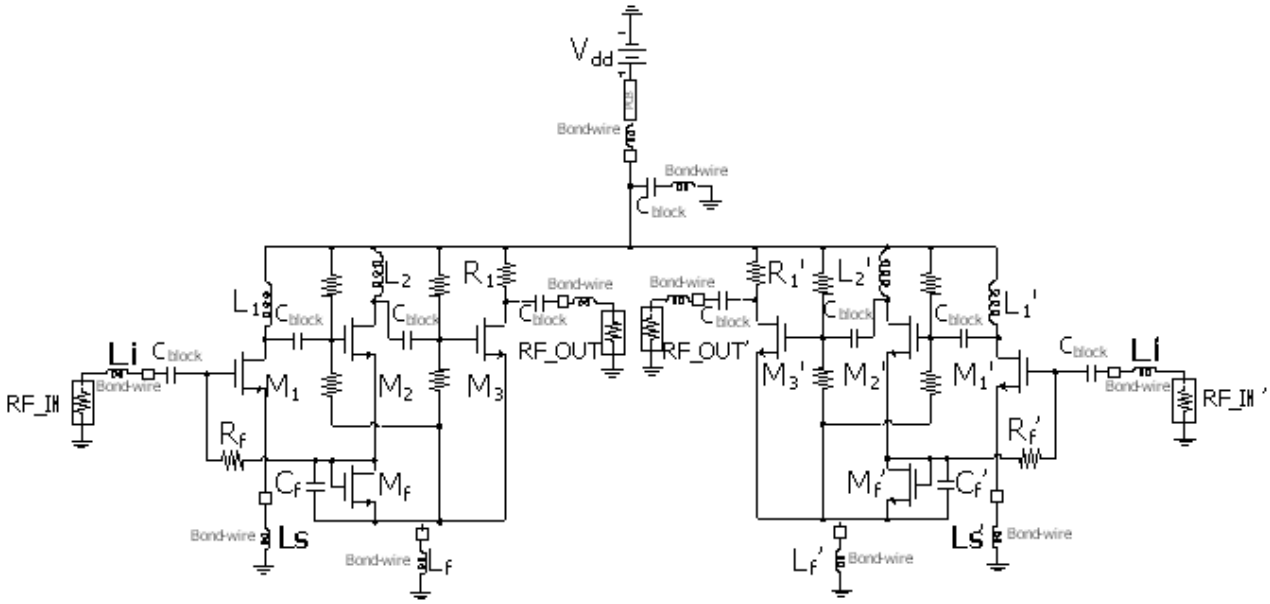

Fig. 2. Circuit schematic of a three-stage broadband CMOS differential LNA

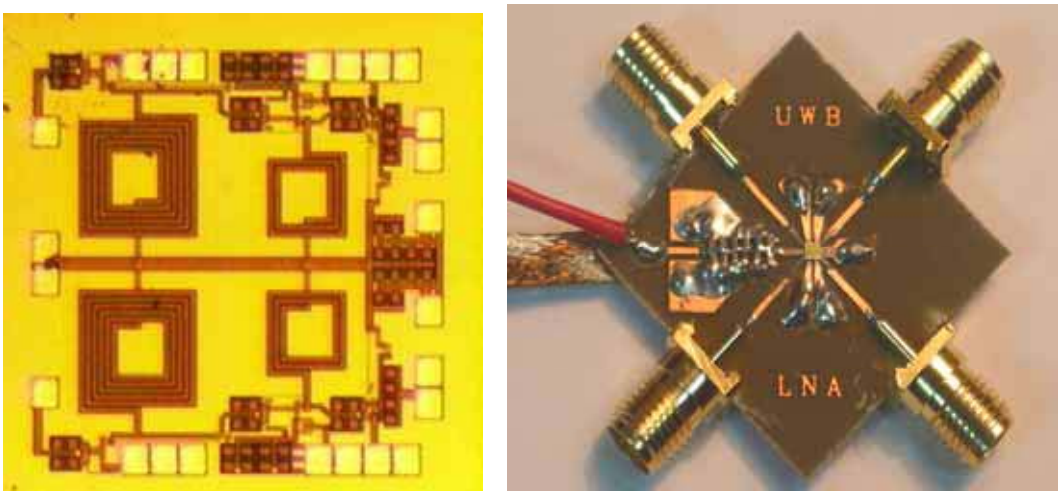

Fig. 3. LNA chip micrograph and photograph of the FR-4 PCB test board

As shown in Fig. 1 this LNA, which did not use a high impedance at the source terminal, is a pseudo-differential circuit structure. The reason not to use a true differential amplifier circuit is that, for low-voltage RFIC design (for example 1.8V) a high impedance at the source terminal will compress the voltage headroom and output voltage swing which will reduce the amplifier gain. Also this pseudo-differentia LNA circuit still can reject the common mode noise from V_{dd}.

III. CIRCUIT PERFORMANCE

Fig. 3 shows the LNA chip micrograph with a die size of 1.0872 x 1.0352 mm^2 and the photograph of the FR-4 PCB test board for measurements. The LNA chip is connected to the test board with aluminum bond-wires. The bond-wire length is carefully controlled and the bond-wire inductance is about 0.8 nH per mm. The effects of the bond-wire inductance and the FR-4 test board are all taken into account in the simulations The S-parameters are measured by a 4-port vector network analyzer. For the noise figure measurement, as shown in Fig. 4, two microstrip 180° hybrid ring couplers connected to the differential input and output ports of the LNA. This is to generate and combine a differential signal for the noise figure measurement.

Several microstrip ring couplers for different frequency bands covering 2.4 to 6 GHz have been fabricated. The return loss of each ring coupler is higher than 15 dB and the insertion loss of that is about 1 dB. The effect of the coupler has been taken into account in both simulation and measurement de-embedding.

Table I summarizes the simulated and measured performance. Measurement results of the differential LNA are discussed as follows.

(a) In the ISM band from 2.4 to 3GHz (covering a 802.11b/g band), the broadband LNA exhibit a gainof 17.5-18dB, noise figure less than 3.5dB, input/output return loss **better** than 6 dB, and input P_{1dB} of –17 dBm, respectively. The DC supply is 1.8V.

(b) In the UWB low-band (3.1 to 5.2GHz), the broadband LNA exhibit a gain of 17.5-18.2 dB, noise figure of 3.4-5 dB, input/output return loss **better** than 10 dB, and input P_{1dB} of −17 dBm, respectively.
(c) From 5.2 to 6GHz, the noise figure of the LNA becomes higher than 5 dB. The gain also decrease to about 15 dB.

Compared with previously published UWB LNAs[3][4], although the current consumption of our CMOS LNA seems much higher than that of [4] (also CMOS LNA), it should be noted that the current consumption of our LNA includes the buffer stage for 50-Ω measurement and each buffer consumes about 6mA. Hence a half-circuit of this differential LNA (without the buffer stage) consumes about 11mA (=34/2-6 mA). Although it is about a double of that (5 mA) of the CMOS LNA in [4], it is noted that the gain of our LNA is almost 9dB higher at 3~5 GHz. As for the SiGe LNA in [3], it consumes 10mA under 3V DC voltage which is equivalent to 30mW power consumption. Although it is about 25% lower than that of our LNA (22mA x 1.8V = 39.6mW), the SiGe bipolar device, which has an inherently lower noise and higher power gain than pure CMOS device, will have a higher process cost.

IV. CONCLUSION

This paper presents a 2.4-6 GHz broadband CMOS differential LNA fabricated with the 0.18 μm 1P6M standard CMOS process. Measurement of the chip is performed on a FR-4 PCB test fixture. Several microstrip 180° ring couplers for different frequency bands covering 2.4 to 6 GHz have been fabricated as baluns to generate and combine a differential signal for the noise figure measurement. The effect of the ring coupler has been taken into account in both simulation and measurement de-embedding. In the UWB low-band (3.1 to 6GHz), the broadband LNA exhibit a gain of 15.5-18.2 dB, noise figure of 3.4-5.9dB, input/output return loss **better** than 10 dB, and input P_{1dB} of −17 dBm, respectively. In the band from 2.4 to 3GHz (covering a 802.11b/g band), the LNA exhibit a gain of 17.5-18dB, noise figure less than 3.5dB, and input P_{1dB} of −17 dBm, respectively. The DC supply is 1.8V with a current consumption of 22mA without the buffer stage (or 11mA for a half-circuit).

ACKNOWLEDGEMENT

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TABLE I
SUMMARY OF THE SIMULATION AND MEASURED PERFORMANCE OF A BROADBAND CMOS DIFFERENTIAL LNA

2.4~6 GHz Broadband CMOS Differential Low-Noise Amplifier		
Technology	0.18μm CMOS	
Frequency Range	3.1 ~ 5.2GHz (UWB Low-Band)/ 2.4 ~ 3.1GHz (WLAN b/g)	
	Simulation	Measurement
DC	1.8V/22mA (without buffer) (11mA for half circuit)	1.8V/22mA (without buffer) (11mA for half circuit)
Input Return Loss	>14dB/>11dB	>10dB/>6dB
Output Return Loss	>13dB/>13dB	>11dB/>10dB
Gain	>20dB/>20dB	>17.5dB/>17.5dB
Flatness	<1dB/<1dB	<0.7dB/<0.5dB
Input P_{1dB}	-23dBm	-17dBm
IIP3	-11dBm	-13.2dBm
Noise Figure	<3dB/<2.5dB	<5dB/<3.5dB
3dB Gain BW	2~7GHz	2~6GHz
Die size	1.0872 x 1.0352 mm^2	