A Novel Wideband MMIC Voltage Controlled Attenuator with a Bandpass Filter Topology

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Abstract **– The design and analysis of a novel wideband, monolithic, bandpass, π-network, voltage controlled attenuator (VCA) is presented. A 24 to 32 GHz VCA was developed using 0.15μm GaAs pHEMT technology. This is the first reported VCA to use a bandpass filter topology to achieve the required operating frequency band and eliminate the effects of parasitic capacitances of the pHEMTs. The bandpass filter absorbs the parasitic capacitances and thereby eliminates their detrimental effects.**

The measured attenuation dynamic range is 12dB ± 0.5dB with minimum insertion loss of 2-3dB. The input power handling capability is up to 0dBm. The VCA is well matched and may be placed in a 50Ω system [1].

I. Introduction

Attenuators are found in a variety of applications in communication systems. The main applications are feedback networks, transceivers, and temperature compensation networks. Some specific applications include automatic level (or gain) control systems, switches, broadband microwave leveling loops, and amplitude stabilization in oscillators [2 - 10].

The common resistive network topologies utilized in attenuators are the T-network, the π-network, and the bridge-T network [2].

Traditionally, variable attenuators are realized using PIN diodes and a pair of couplers in a balanced configuration. Recently, over the past two decades, MESFETs and HEMTs are being used increasingly in the design of variable attenuators [2, 3, 11].

Most reported variable attenuators using FETs address the issues of eliminating parasitic capacitances, increasing attenuation dynamic range, and improving linearity [5, 7, 12 - 15]. Others tackle the issue of increasing power handling capability [4, 16]. Yet some address the issue of phase flatness with respect to attenuation settings [17].

The methods reported to eliminate the parasitic capacitances and improve linearity and dynamic range vary. [5] uses feedback to control input and output return losses as attenuation is changed and achieves 12dB dynamic range from 2 to 8 GHz. [7] uses a parallel combination of FETs in both the series and shunt arms of the T-network attenuator achieving 12dB dynamic range over 1 to 6 GHz. In [12], the author uses a T-network in which the shunt arm FET is distributed into four smaller cells interconnected by high impedance transmission lines, and a 50Ω resistor is placed in parallel with each series FET. The result of this is a dynamic range of 30dB from DC to 50GHz. In [13], the author utilizes a bridged-T network in which the series and shunt FETs are each a parallel combination of several FETs with a resistive gate voltage divider. The result is improved linearity with a dynamic range of 12dB from DC to 8GHz. [14] shows a π-attenuator in which the series arm consists of two cascaded FETs achieving 40dB dynamic range for CDMA applications (900MHz). [15] employs a gate pinch-off tracker for both the series and shunt FETs in the T-attenuator resulting in 20dB linear dynamic range at 900MHz.

In the following sections, a new method of eliminating parasitic capacitances and achieving linear attenuation with good dynamic range will be presented. The new method involves implementation of a bandpass filter design approach for the variable π-attenuator. In this design approach the parasitic capacitances are absorbed by the bandpass filter structure. Thus, the new design method not only serves the formerly stated purpose, but also achieves the desired wide operating frequency range.

II. Design of the Voltage Controlled Attenuator

The voltage controlled attenuator (VCA) uses FETs to achieve variable attenuation in a π-network topology. The VCA is implemented with a 0.15μm pHEMT process on a 75μm thick wafer.

A. FET Attenuator Design

In FETs, the drain-to-source resistance, r_{ds}, is proportional to the applied gate voltage when the drain-to-source voltage and current are zero. Also, when the FET is unbiased, the transconductance is zero, thereby simplifying the FET's model into a combination of resistors and capacitors, represented as a parallel RC circuit with an effective resistance and an effective capacitance. The FET attenuator relies primarily on the variation of r_{ds} by varying the applied gate voltage; however, parasitic capacitances and resistances do exist. These parasitic capacitances have a significant influence on the VCA performance at high frequencies [2, 3, 4, 7, 11, 12].

Not only does the value of r_{ds} (hence the effective resistance) depend on the gate potential, but also it depends on the gate width of the FET. Increasing the gate width, or increasing the number of fingers, decreases r_{ds},

but the parasitic capacitances increase in value. These larger capacitances limit the dynamic range of attenuation, especially at higher frequencies, where the FET is predominantly capacitive; whereas at lower frequencies, the FET is predominantly resistive. [2 - 5, 7, 10 – 12]

In addition to gate potential and gate width, the effective resistance (and parasitic capacitances) is dependent on frequency as well [1].

With all of this said, careful analysis must be carried out to select the optimum topology and FET sizes in order to obtain linear attenuation (analyzing the output admittance of several FET sizes with respect to voltage and frequency) [1]. Hence, the π-network topology was selected with a 300µm FET in the series arm and a 200µm FET in each of the shunt arms as shown in Fig. 1.

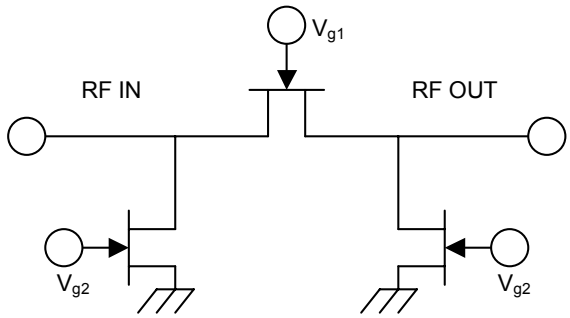


Fig. 1. π-network FET attenuator.

The FET selections also involve careful analysis of the optimum voltage control settings that would give maximum, linear dynamic range of attenuation with minimal insertion loss at the low setting. The VCA uses two voltage controls, one for the series arm FET (V_{g1}) and one for both of the shunt arm FETs (V_{g2}). Eleven pairs of control voltage settings were selected for optimum performance [1].

B. Bandpass Filter Design

In [18] it is shown that a bandpass filter can be formed by using T-sections and π-sections as shown in Fig. 2 where Z_{image}=50Ω.

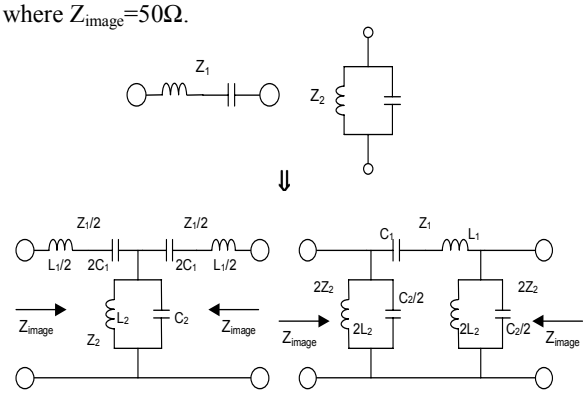


Fig. 2. T-section and π-section bandpass filters

From Fig. 2, either two cascaded T-sections or one π-section are necessary to form a π-network. The π-section has fewer components than the two cascaded T-sections; hence, it was chosen for the design.

Therefore, using C_1=C_{out} of the 300µm FET in the series arm and using $C_2/2$=C_{out} of the 200µm FET in the shunt arms, the band pass π-attenuator can be implemented as shown in Fig. 3, where L_1 and L_2 are external elements. The bandpass filter structure (Fig. 3) absorbs the parasitic capacitances of the FETs.

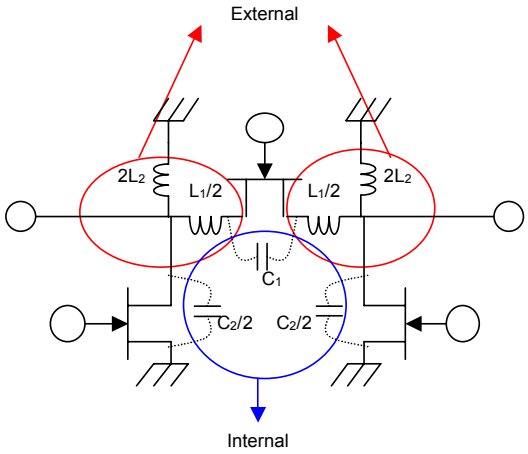


Fig. 3. π-attenuator bandpass topology.

The design equations for an ideal bandpass filter obtained from [19] are:

$$L_1 = R_0 / \pi(f_2 - f_1) \quad (1)$$

$$C_1 = (f_2 - f_1) / 4\pi R_0 f_1 f_2 \quad (2)$$

$$L_2 = R_0(f_2 - f_1) / 4\pi f_1 f_2 \quad (3)$$

$$C_2 = 1 / \pi R_0(f_2 - f_1) \quad (4)$$

$$R_0 = \sqrt{(L_1/C_2)} = \sqrt{(L_2/C_1)} \quad (5)$$

$$f_0 = \sqrt{(f_1 f_2)}. \quad (6)$$

Here f_0 is the center frequency of the band, f_1 and f_2 are the lower and upper cutoff frequencies respectively, R_0 is the image impedance (Z_{image}) at f_0, and L_1, C_1, L_2, C_2 are shown in Fig. 3. From equations (1) through (6), the following can be inferred:

1) For a certain f_0, $f_1 f_2$ (the product) is fixed by (6), and
2) For a given R_0 and C_2 (i.e. C_{out} of FET), f_2–f_1 (the difference) is fixed by (4).

C. Bandpass π-Attenuator Design

In the final design of the VCA, the design constraints for equations (1) through (6) are slightly modified. Both C_2 and C_1 are held constant as a design constraint instead of just keeping C_2 fixed. Hence, $C_2/2$=C_{out} of the 200µm FET and C_1=C_{out} of the 300µm at the appropriate gate voltages. Using equations (2) and (4), the product and the difference of the lower and upper cutoff frequencies are calculated with R_0=50Ω. Then the values of L_1 and L_2 are calculated using (1) and (3). This approach helped center the pass-band more effectively than following the standard design constraints.

The resulting circuit was then implemented in microstrip form using a 0.15µm pHEMT process on a 75µm thick wafer. The layout is shown in Fig. 4.

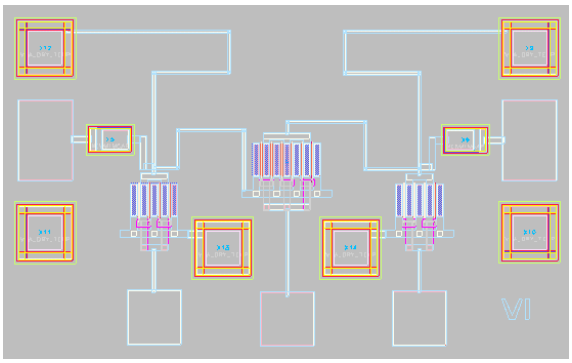


Fig. 4. Final layout of the band pass π-attenuator.

III. Measured Results

The VCA was fabricated at Fujitsu Quantum Devices in Japan and tested at Fujitsu Compound Semiconductor, Inc. (now known as Eudyna). The size of the VCA is approximately 800µm x 500µm and is shown in Fig. 5.

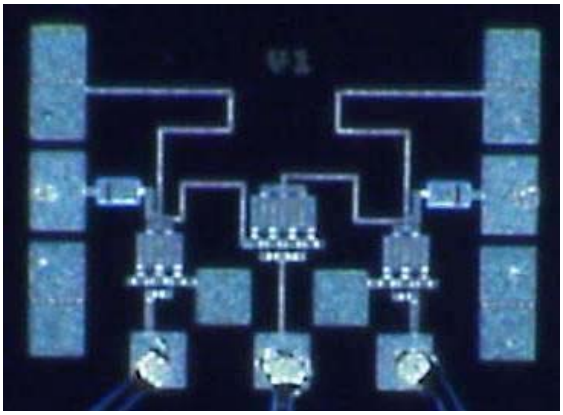
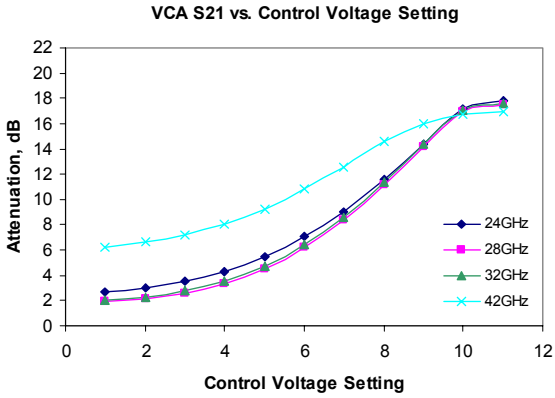


Fig. 5. Photograph of the fabricated VCA chip.

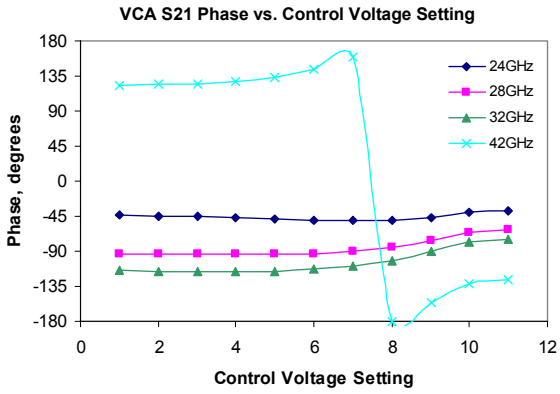
The measurements of the VCA consisted of S-parameters and power measurements over the frequency range 24 to 42 GHz at each of the eleven pairs of control voltage settings (bias points) of V_{g1} and V_{g2}.

From the S-parameter data, plots of attenuation, phase, and return losses versus control voltage settings were obtained. Fig. 6 shows these plots. The data shows that the attenuator is fairly linear with a dynamic range of about 12dB ± 0.5dB from 24 to 32 GHz; the phase flatness varies from 2° to 5° from 24 to 28 GHz; and the return losses are greater than 10dB for the first eight attenuation settings from 24 to 32 GHz. The minimum insertion loss is 2 to 3 dB.

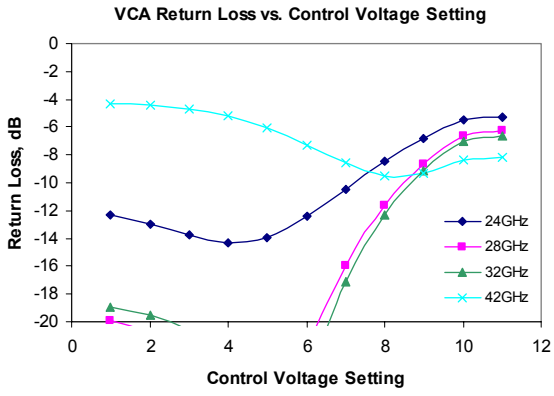
Power measurements were obtained from 24 to 32 GHz at 1GHz steps at each of the eleven pairs of control voltage settings where P_{in} was varied from -15dBm to +15dBm. A plot of P_{out} vs. P_{in} over the frequency range at the fifth control voltage setting is shown in Fig. 7. The input power handling capability deduced from the data is about 0dBm.



(a)



(b)



(c)

Fig. 6. Measured parameters: (a) Attenuation, S_{21} (b) Phase of S_{21} (c) Return Losses, S_{11} and S_{22}.

IV. Conclusions

The design method and analysis of a novel wideband, monolithic, bandpass, π-network, voltage controlled attenuator has been presented. The 24 to 32 GHz voltage controlled attenuator presented in this paper has a linear attenuation dynamic range of about 12dB ± 0.5dB with minimum insertion loss of 2 to 3 dB. The input power

handling capability is about 0dBm. The VCA is well matched and can be placed in a 50Ω system.

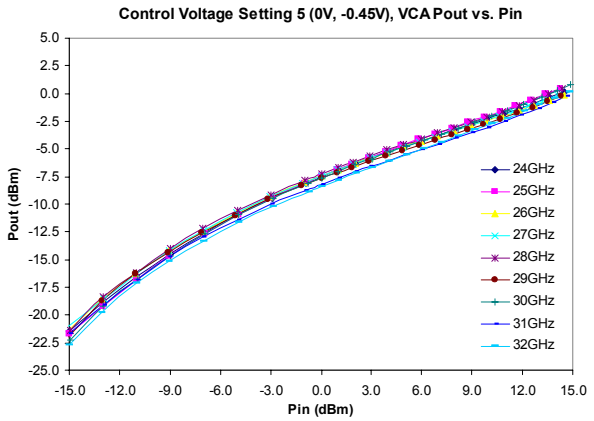


Fig. 7. Measured P_{out} vs. P_{in} over frequency at the fifth control voltage setting.

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REFERENCES

[1] S. M. Halabi (Scarlet M. Daoud), "Active Bias, Power Detector, and Voltage Controlled Attenuator MMICs," MSEE Thesis, Department of Electrical and Computer Engineering, Bradley University, Peoria, IL, USA, 2004.

[2] J. M. Golio, *Microwave MESFETs & HEMTs*, Boston, MA: Artech House, 1991.

[3] R. E. Collin, *Foundations for Microwave Engineering*, 2nd Edition, IEEE Press, 2001.

[4] Y. Tajima, T. Tsukii, R. Mozzi, E. Tong, L. Hanes, and B. Wrona, "GaAs Monolithic Wideband (2-18 GHz) Variable Attenuators," *IEEE MTT-S Digest*, pp. 479-481, 1982.

[5] G. S. Barta, K. E. Jones, G. C. Herrick, E. W. Strid, "A 2 to 8 GHz Leveling Loop Using A GaAs MMIC Active Splitter and Attenuator," IEEE Microwave and mm-wave Monolithic Circuits Symposium Digest, pp.75-78, 1986.

[6] S. Dindo, R. Meierer, and R. North, "Computer-Aided Design of MMIC Variable Attenuators," Microwave Journal, pp. 134-140, November 1997.

[7] G. Lizama, T. Andrade, R. Benton, "1 – 6 GHz GaAs MMIC Linear Attenuator with Integral Drivers," IEEE Microwave and mm-wave Monolithic Circuits Symposium Digest, pp. 105 – 107, 1987.

[8] P. S. Bachert, "FET Attenuator, 0-1 GHz," Applied Microwave & Wireless, pp. 57-64, Spring 1996.

[9] L. M. Devlin, B. J. Buck, J. C. Clifton, A. W. Dearn, A. P. Long, "A 2.4GHz Single Chip Transceiver," IEEE Microwave and mm-wave Monolithic Circuits Symposium, pp. 23-26, 1993.

[10] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*, Reading, MA: Addison-Wesley Publishing Company, 1971 (second printing 1978).

[11] J. P. Mondal, A. G. Milnes, and J. G. Oakes, "Theoretical analysis for microwave T- and π-type attenuator circuits using MESFETs," International Journal of Electronics, Vol. 58, No. 2, pp. 231-247, 1985.

[12] H. Kondoh, "DC–50GHz MMIC Variable Attenuator with a 30dB Dynamic Range," IEE MTT-S Digest, pp. 499-502, 1988.

[13] B. Maoz, "A Novel, Linear Voltage Variable MMIC Attenuator," IEEE Transactions on Microwave Theory and Techniques, Vol. 38, No. 11, pp. 1675-1683, November 1990.

[14] M. Inamori, K. Motoyoshi, T. Kitazawa, K. Tara, and M. Hagio, " A New GaAs Variable Gain Amplifier MMIC with a Wide-Dynamic-Range and Low-Voltage-Operation Linear Attenuation Circuit," RFIC Symposium, pp. 39 – 42, 1999.

[15] L. Boglione and R. Pavio, "Temperature and Process Insensitive Circuit Design of a Voltage Variable Attenuator IC for Cellular Band Applications," IEEE Microwave and Guided Wave Letters, Vol. 10, No. 7, pp. 279 – 281, July 2000.

[16] M. Shifrin, P. Katzin, Y. Ayasli, "High Power Control Components Using a New Monolithic FET Structrure," IEEE Microwave and mm-wave Monolithic Circuits Symposium, pp. 51-56, 1989.

[17] L. Sjogren, D. Ingram, M Biedenbender, R. Lai, B. Allen, and K. Hubbard, "A Low Phase-Error 44-GHz HEMT Attenuator," IEEE Microwave and Guided Wave Letters, Vol. 8, No. 5, pp.195-195, May 1998.

[18] After O.J. Zobel, "Wave (Zobel) Filters, Part I," Lecture notes from Dr. Prasad N. Shastry.

[19] S. N. Prasad (Prasad N.Shastry), J.B. Beyer, "Band-Pass Distributed Amplifiers," *Microwave and Optical Technology Letters*, Vol. 2. No. 10, pp. 349 – 354, October 1989.