A New Empirical Non-linear Model for SOI MOSFET

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Abstract – An empirical non-linear model for SOI MOSFET useful for large-signal simulations of high frequency circuit design is presented. An original close form expression is proposed for the drain current and charge conservation is taken into account, as capacitances are derived from a single charge model. The model's parameters are first extracted, prior the model implementation in a circuit simulator. Then some comparisons with experimental data are proposed to validate the model. Note that the model is well suited for the Fully Depleted either the Partially Depleted devices.

INTRODUCTION

SOI MOSFET devices present more and more interesting high frequency performances along with the continuous decrease of the gate length. For this reason, it seems realistic to use such devices in centimetrique and probably millimetrique wave ranges [1] [3].

Several empirical non-linear models for MESFET's and HEMT's have been developed for high frequency applications, but not so much for MOSFET on SOI substrate. The existing ones are generally physics oriented and they require technological data for their parameter extraction [2].

The aim of this paper is to present an empirical non-linear model for SOI MOSFET, easy to extract, scalable on gate width, for applications like amplifiers, mixers and oscillators down to the millimetrique range. This model which was studied for Fully Depleted (F.D.) and Partially Depleted (P.D.) SOI MOSFET's realised by the CEA LETI [3], describes accurately their electrical (DC-AC) characteristics. It includes a non-linear drain current expression that is continuous and infinitely derivable, leading the transconductance and the drain conductance to be continuous. The capacitances are derived directly from a gate charge expression that ensures the charge conservation principle.

THE NON LINEAR DRAIN CURRENT

The drain current equation is originally based on the Angelov's [4] model developed for III-V devices, but it has been modified in order to be suitable for SOI devices:

$$I_{dsi}(V_{gsi},V_{dsi}) = Kf(V_{gsi})\, f(V_{gsi},V_{dsi}) \qquad (1)$$

In (1), the first function depends on the control voltage V_{gsi} while the second one is dependent on both V_{gsi} and V_{dsi}. More specifically the drain current is given by the following expression:

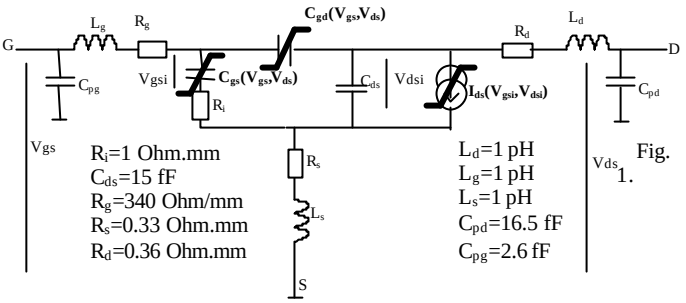


Fig. 1. Equivalent-circuit model for the MOS SOI with the non-linear elements. Intrinsic and extrinsic element values for an F.D. SOI MOS with Lg=0.25 µm and W=8x12.5µm.

$$I_{ds}(V_{gsi},V_{dsi}) = I_{pk} W_f n_f \left[1+P(V_{gsi})\tanh(\Psi(V_{gsi}))\right]\times$$
$$\times\left[P(V_{gdi})\tanh\left(V_{dsi}\left(K_7 V_{gsi}+a\right)\right)\right]\times\left[0.5\left(1+\tanh\left((V_{gsi}-\frac{V_{th}}{2})10^6\right)\right)\right] \qquad (2)$$
$$\Psi(V_{gsi}) = P_1\left(V_{gsi}-V_{pk}\right)+P_2\left(V_{gsi}-V_{pk}\right)^2+P_3\left(V_{gsi}-V_{pk}\right)^3$$
$$P(V_{gsi}) = K_0+K_1 V_{gsi}+K_2 V_{gsi}^{\ 2}+K_3 V_{gsi}^{\ 3}$$
$$P(V_{gdi}) = 1+K_4 V_{gdi}+K_5 V_{gdi}^{\ 2}+K_6 V_{gdi}^{\ 3}$$

In (2) Y is the same term as those used in Angelov model [4]. Polynomial expressions were added to better describe the experimental variations of the transconductance g_m and conductance g_d in the saturation regime. The term $tanh(V_{dsi}(K_7 V_{gsi}+a))$ describes the region between the linear and the saturation regime of the transistors. The last term ensures a current to be equal to zero in subthreshold region and for negative gate biases. All the terms P_i, K_i, a, V_{pk} and I_{pk} are the current model's parameters, W_f is the transistor's width per finger and n_f the number of fingers. V_{th} is the measured threshold voltage. They don't have any real physical meaning (except of V_{th}) even if some of them have physical dimensions.

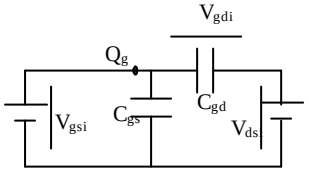
The transconductance's and conductance's equations are given by:

$$g_{mi}(V_{gsi},V_{dsi}) = \frac{dI_{ds}}{dV_{gsi}|_{V_{dsi}=cte}}$$
$$g_{di}(V_{gsi},V_{dsi}) = \frac{dI_{ds}}{dV_{dsi}|_{V_{gsi}=cte}} \quad (3)$$

This model describes the static current versus the intrinsic voltages V_{gsi} and V_{dsi} taking into account the potential drop across R_s and R_d.

THE NON LINEAR CAPACITANCE

The best way to model capacitance and to keep charge conservation is to consider the total charge at a given physical point of a device [5]. The charge on the gate electrode depends on the gate bias and the drain bias : $Q_g(V_{gsi},V_{dsi})$. The capacitance C_{gs} and C_{gd} will be [5]:



$$C_{gs} + C_{gd} = \frac{dQ_g}{dV_{gsi}|_{V_{dsi}=cte}}$$
$$C_{gd} = -\frac{dQ_g}{dV_{dsi}|_{V_{gsi}=cte}} \quad (4)$$

The capacitances C_{gs} and C_{gd} are derived from the same charge expression and are interdependent. They have to verify this mathematical relation (4), otherwise the model is not charge conservative. Using a charge model from which the expressions for C_{gs} and C_{gd} are calculated by (4), we can model the gate capacitances without having to take into account of a transcapacitance C_m element [5], [6].

Following this principles the gate charge for the MOS SOI transistors was modelled by the equation inspired by [7]:

$$Q_g = K\left(f_1(V_{gsi},V_{dsi}) + f_2(V_{gsi},V_{dsi})\right)$$
$$K = C_0 n_f W_f \left(L_g - 2L_d\right)$$
$$f_1 = \left(C_{gg1}V_{gsi} + C_{gg2}V_{gsi}^{\ 2} + C_{gg3}V_{gsi}^{\ 3}\right)\left[C_{gg0} + \tanh\left(\frac{V_{dsi}^{\ 2}}{gV_{gsi}^{\ 2}}\right)\right] \quad (5)$$
$$f_2 = \left(C_{gd1}V_{gdi} + C_{gd2}V_{gdi}^{\ 2}\right)\left[C_{gd0} + \tanh\left(-\frac{V_{dsi}}{V_t}\right)\right]$$

In (5), L_g is the gate length, W_f the gate width per finger and n_f the number of fingers. C_0, L_d, C_{ggi}, C_{gdi}, g and V_t are the model parameters. (4) and (5) give the explicit functions for C_{gs} and C_{gd}.

SIMULATION, RESULTS

We present here the results obtained for a FD SOI MOSFET with *W=8x12.5 µm, Lg=0.25 µm* and with salicide gate. The model parameters extracted for this transistor are summarized in table I.

TABLE I

Current parameters

V_{pk}	I_{pk}	a	P_1	P_2	P_3	V_{th}	
403.7 mV	34.89 mA/mm	0.808 V^{-1}	2.434 V^{-1}	-0.791 V^{-2}	1.016 V^{-3}	0.34 V	
K_0	K_1	K_2	K_3	K_4	K_5	K_6	K_7
1.202 —	2.118 V^{-1}	4.613 V^{-2}	-0.799 V^{-3}	0.049 V^{-1}	0.049 V^{-2}	0.061 V^{-3}	2.962 V

Charge parameters

C_0	L_d	C_{gg0}	C_{gg1}	C_{gg2}	C_{gg3}
1.768 fF/mm^2	4.441 fm	-4.905 —	-24.78 —	-29.63 V^{-1}	6.066 V^{-2}

C_{gd0}	C_{gd1}	C_{gd2}	?	V_t
1.671 —	51.68 —	-17.36 V^{-1}	0.584 —	1.552 V

The parameters were extracted using an optimisation procedure in the ICCAP environment (Agilent Technologies EEsof), by adjusting the model equations on the measured DC and AC data. The intrinsic and extrinsic elements were deduced from bias depending S-parameter measurements [8]. The model was implemented in the ADS (Agilent Technologies EEsof) circuit simulator. Small signal and large signal simulations were carried out in order to perform some comparisons with experimental data and validate the model.

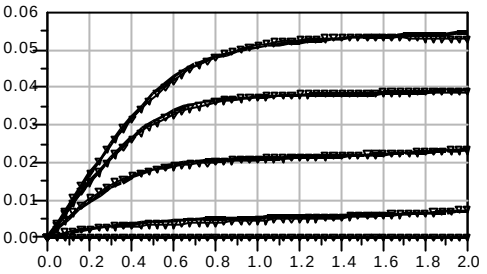


Fig. 2.a Static drain current versus drain bias for 5 different values of gate bias. Measurements (symbols) and model (solid line).

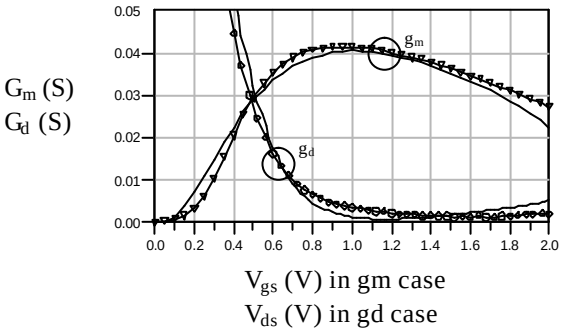


Fig. 2.b Static transconductance gm versus gate bias Vgs for Vds=1V. Measurements (triangles) and model (solid line). Static conductance gd versus drain bias Vds for Vgs=1V. Measurements (circles) and model (solid line).

We observe an excellent agreement in Fig.2a-b upon the static simulation for the drain current versus V_{ds} for different values of V_{gs}, but also for the output conductance g_d and the transconductance g_m. In Fig.3 is shown the capacitance C_{gs} measured and modelled by the expressions (4) and (5). There is a slight disagreement due to the fact

that, a priori, we don't know the exact expression of the gate charge, nevertheless the model is charge conservative.

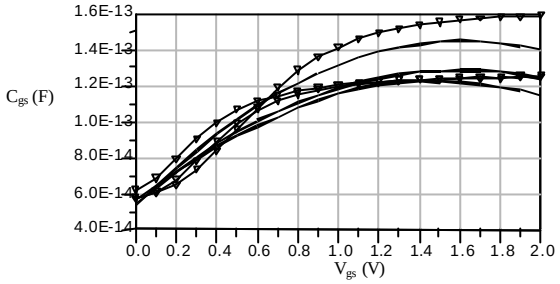


Fig. 3. Capacitance Cgs versus gate bias Vgs for Vds=0, 1 and 2 V. Measurements (symbols) and model (solid line).

Next, in Fig.4 a-b, the small-signal simulations are compared to the measured ones. The four S-parameters are plotted for frequencies varying from *0.25 GHz* to *50 GHz* and the agreement is quite good.

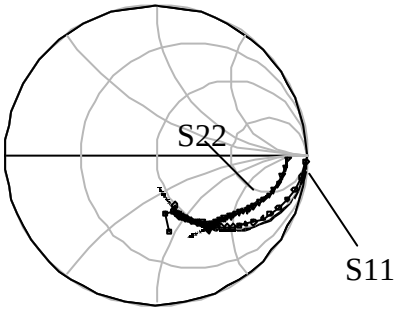


Fig. 4.a S11 and S22 parameters versus frequency varying from 0.25 GHz to 50 GHz for Vgs=0.6 V and Vds=1 V. Measurements (symbols) and model (solid line).

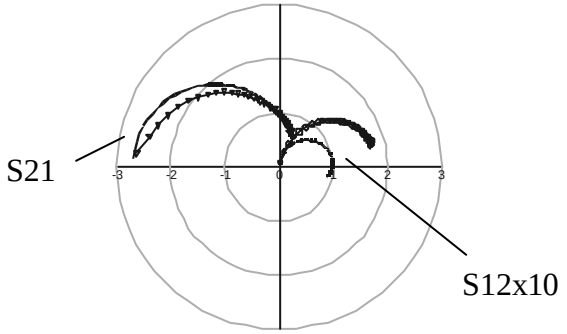


Fig. 4.b S21 and S12(x10) parameters versus frequency varying from 0.25 GHz to 50 GHz for Vgs=0.6 V and Vds=1 V. Measurements (symbols) and model (solid line).

Finally, in order to validate the model, some large signal measurements have been carried out. For this purpose, we have applied at the input of the device a microwave power P_{in} using a 50 Ω generator and measured the output power P_{out} absorbed by the 50 Ω load (Fig.5) [9]. The results are shown in Fig.6.a and a good agreement has been observed with the large signal simulation made using ADS.

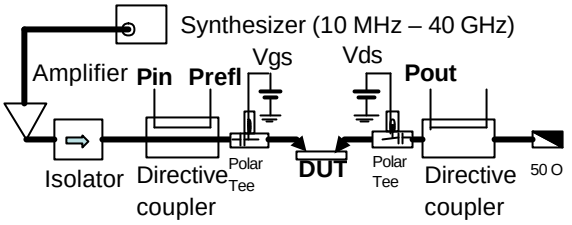


Fig. 5 Schematic measurement setup used for determination of the one tone power response of the device.

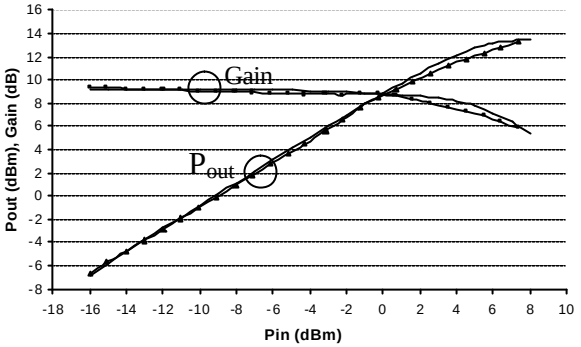


Fig. 6.a Output power Pout and gain versus input power on the transistor with W=8x12.5 µm. f=4 GHz, Vgs=1.5 V, Vds=2 V. Measurements (symbols) and model (solid line).

The scalability of the model in large signal condition versus gate width *W* has been checked as well on Fig.6.b, where we present the P_{out} versus P_{in} of the transistor with *W=8x12.5 µm* scaled at *W=8x6.25 µm*, and we compare it to the measured data of a transistor with *W=8x6.25 µm* (same frequency and biases).

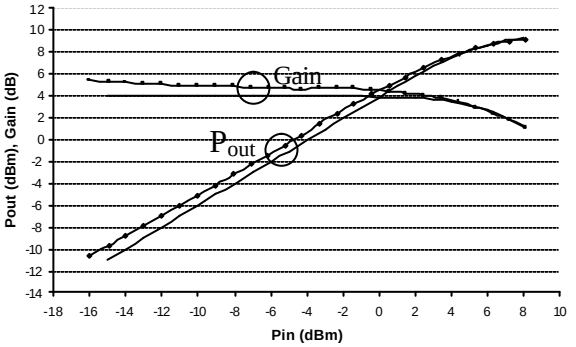


Fig. 6.b Output power Pout and gain versus input power on the transistor. Measurements (symbols) and model (solid line).

CONCLUSIONS

In this paper a new empirical non-linear model for SOI MOSFET's (FD and PD) has been presented. This model is based both upon close form expressions of the non-linear drain current and gate charge. The parameters of the model can be easily extracted using ICCAP optimiser and the comparisons in terms of static and dynamic performances

are in good agreement with the experimental ones. Finally, single tone large signal measurements have been made and compared with simulations. As a conclusion, this non-linear model can be useful for the design of centimetrique and millimetrique non-linear circuits (mixers or oscillators).

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