A NEW RELIABLE FABRICATION-PROCESS FOR InP BASED HEMTs AND MMICs WITH GATE LENGTH FROM 0.06 TO 0.2 μm

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***Abstract*-- we present a complete fabrication process and measured results for InP based HEMTs and MMICs. A major effort has been focused on the development of new and reliable gate and via-hole process both for InP based HEMTs and MMICs. A single exposure is required to define both the footprint and the head of the T-gate by modulation of the exposure doses. The developed gate and via-hole process is reliable and suitable for volume production of InP-HEMTs and MMICs with high yield. A complete MMIC chip includes mesa resistors, microstrip transmission lines, HEMT transistors, and ground via holes. A cutoff frequency f_T of 100 GHz and maximum oscillation frequency f_{max} of 200 GHz was obtained from 0.1 μm gate lattice matched AlInAs/GaInAs/InP based HEMTs.**

1. INTRODUCTION

For millimeter wave applications, the T-shaped gates are required for the production of high performance HEMTs and MMICs to achieve very small gate length and hence low gate resistance. A number of processes [1-4] have been described where a single and/or multiple electron-beam lithography steps has been used to define a resist profile in the multilayer resist system. Triple or bi-layers of polymethylmethacrylate (PMMA) and the copolymer (PMMA-AAM) are commonly used electron beam resists to define the T-shaped gate [1]. However, these resists have non-polar solvent developers that can be chosen to have a certain, but not complete selectivity. This together with the small difference in the resist sensitivity, results in a small process window. It is also difficult to control the ratio between the cross-section and the gate length. Other gate processes where combined optical and e-beam exposures [5-6] have also been reported, but they require accurate alignment.

In this letter, we report on a novel process with a tri-layer resist with completely selective developers and moderately low exposure doses. The process has shown to be very reliable and fast with good control of the gate lengths and give a high yield, and is therefore suitable for mass production. We have produced gate lengths from 0.06 to 0.2 μm in the same process run. Furthermore, reliable via-hole and passivation processes have been developed and applied on InP based HEMTs and MMICs. The passivation process was developed using 850Å sputtered Si_3N_4 at room temperature, while the via-hole process was developed using wet chemical etching.

11. FABRICATIONS PROCESSES

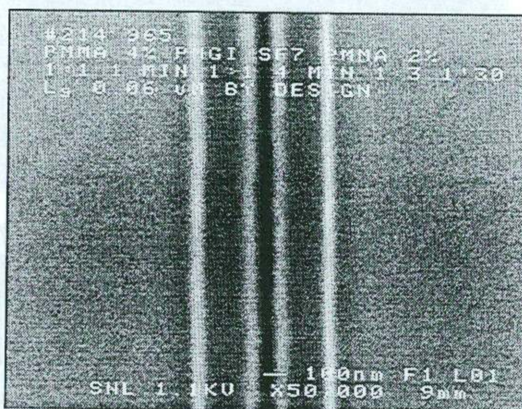
First, mesas and source-drain ohmic contacts were prepared according to our standard optical lithography process [1]. A 240 nm thick bottom layer of PMMA (950K) was then spun on the substrate. The second resist was 400 nm thick layer of PMGI (Shipley Inc.) and the third layer (top) was 70 nm thick layer of PMMA (950). Each resist layer was followed by a 5 minutes bake at 170°C.

A JEOL 5DII was used for a single exposure of the resist with a 50 keV electron beam. A low dose exposure defines the width of the head and a high dose exposure defines the footprint. A 500 nm wide rectangle with a dose of 150 μC/cm^2 was exposed to define the head and a rectangle with varying width from 60 to 200 nm was exposed to define the footprint of the gate with an exposed dose of 450 μC/cm^2. The two resists have completely selective developers that give excellent control over development of the bottom PMMA layer. The top layer is developed in a 1:1 mixture of methylisobuthylketone (MIBK) and isopropanol(IPA) for 60 sec and then rinsed in an IPA and blown dry with nitrogen. The second layer is developed in an aqueous developer (Shipley MF322 with 50 % in water) and then rinsed in a water. The third layer is developed for 90 s in MIBK:IPA (1:3) followed by rinsing in an IPA and blown dry with nitrogen. A low acceleration voltage (1.1 kV)

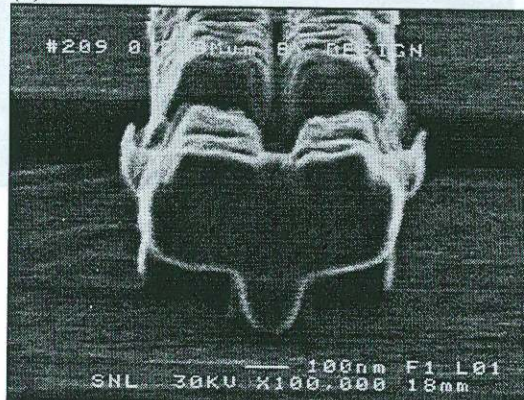
scanning-electron-microscope (SEM) was used to inspect the resist profile after development and can thus adjust the gate length with further development of the bottom layer (if require). Figure 1a shows the resist from the top where the gate length is defined to 0.1 μm and Fig. 1b shows a corresponding T-shaped gate-profile. After plasma descumming, the gate recess etch was done with selective wet etchant (citric acid: H_2O_2) for 50 s. The evaporated gate metals were Ti, Pt and Au (200, 100 and 3200 Å). After gate lithography, thick metal processing step was performed to facilitate the bonding of the devices and to define the microstrip transmission lines on the MMIC chip. Thick metals were electron beam evaporated using Ti/Au (500/1000Å) system.

The passivation process of our devices is based on sputtered Si_3N_4. In order to avoid damage of devices, silicon nitride was sputtered in two steps with optimum sputtering parameters (i.e. rf power, pressure, time etc.). First a very thin layer of 50 Å Si_3N_4 was sputtered with 42 W rf power for 15 min to protect the device surface and then 800 Å Si_3N_4 was sputtered with 100 W rf power for 60 min to achieve a total of 850 Å Si_3N_4 passivation layer. This multiple sputtering step also facilitate a better step coverage of the devices. The flow rate was 30 sccm and the pressure was 15 mTorr. Finally, the Si_3N_4 was etched on unwanted areas with NF_3 plasma with a flow of 30 sccm at 100 W rf power and for 30 sec. Figure 2 shows the 850 Å Si_3N_4 passivated 0.14 μm gate device.

The via-hole process in our HEMTs and MMICs is based on wet chemical etching. The devices/MMICs chip was thin down to 80 μm after mechanical/chemical polishing to achieve a mirror quality surface. The SiO_2 (2000Å) was sputtered to use as a mask before spinning photoresist on the surface. SiO_2 also helps for better adhesion and step coverage. The via-hole patterns (80 μm diameter from the top) were obtained by optical lithography technique. The wet etching was performed using CH_3COOH: HBr: $K_2Cr_2O_7$ solution (1:1:1) at 54 °C. The etch rate was 15-20 μm/min. In order to achieve good uniformity of the via-holes, the devices were stirred continuously in the solution. Finally, the chips were sputtered with Ti/Au (500/3000Å) on the back side of the wafer and then 4 μm Au was electroplated at the end. To facilitate the dicing/scribing on the backside of the wafer, the metal was etched at the scribing position after optical lithography step. Figure 3 shows the via-holes on the backside (Fig.3a) and on the front side of the MMICs chip. The uniformity of the via-hole is quite obvious. All holes were through with approximately 40-50 μm diameter at the bottom and 50-60 μm lateral etching at the top.



(a)



(b)

Fig. 1 The resist seen from the top after the development (a) and corresponding T-shaped gate profile (b) for 0.08 μm gate device.

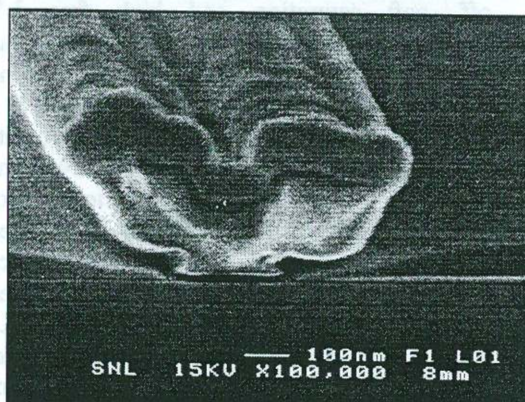


Fig. 2 Sputtered 850 Å Si_3N_4 on 0.14 μm gate InP HEMT device

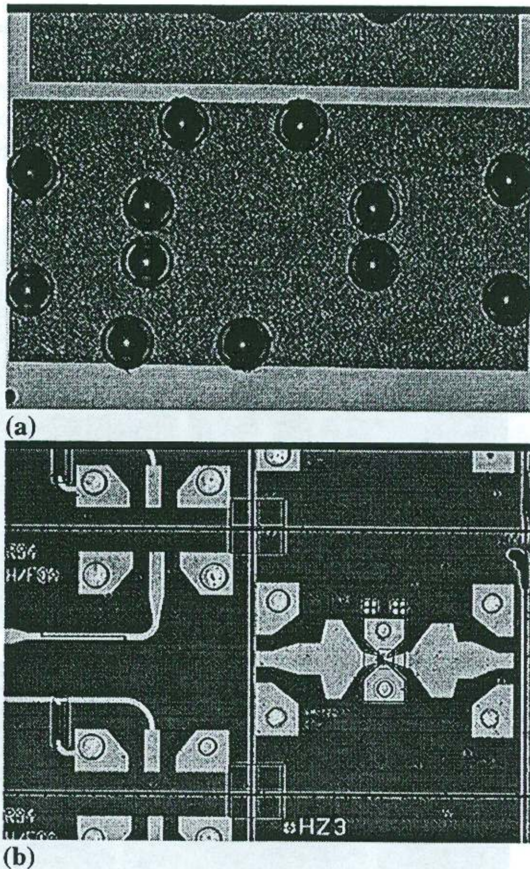
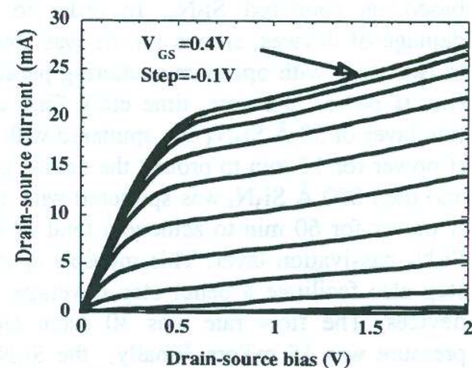


Fig. 3 Via holes on the back side (a) and on the front side (b) of ready MMIC chip.

111. RESULTS AND DISCUSSION

The developed gate, passivation and via-hole process has been applied on AlInAs/GaInAs/InP based lattice matched MBE and MOCVD grown HEMTs and MMICs. The transistors show complete pinch off, soft saturation and kink free I-V characteristics. The measured extrinsic peak transconductance was around 420 mS/mm and the gate-drain breakdown voltage (defined at 1 mA/mm) was around 3.5-4 V for 0.1 µm gate InP-HEMT device. Figure 4 shows the measured I-V and transfer characteristics of 0.1 x 100 μm^2 lattice matched AlInAs/InGaAs/InP HEMT. The frequency performance of the transistors was measured with an HP8510 C network analyzer from 0.5 to 50 GHz. The extrapolation of the current and unilateral power gain gives a cut-off frequency f_T of 100 GHz and maximum oscillation frequency f_{max} of 200 GHz, respectively for 0.1 µm gate device. Figure 5 shows the measured gain performance of 0.1 x 100 μm^2 lattice matched AlInAs/InGaAs/InP HEMT. At Q band, single stage MMIC gives a gain of 12 dB with a 3 dB gain bandwidth of around 24 GHz. A single stage MMIC at W-band (85 GHz) gives a gain of 8.8 dB with a 3 dB gain bandwidth of 10 GHz. Two stage W-band MMIC (14 dB) gives a gain of 14 dB with a 3 dB gain bandwidth of 10 GHz. Finally, a two stage MMIC at 109 GHz gives a gain of 7 dB as shown in the figure 6. Including losses from the bonding wires at the input and output, the actual gain from the two stage MMIC at 109 GHz was 11 dB. This MMIC was measured in a fixture, while the first three MMICs were measured using on wafer probing system. All MMICs were stable at given biasing condition in the desired frequency band.



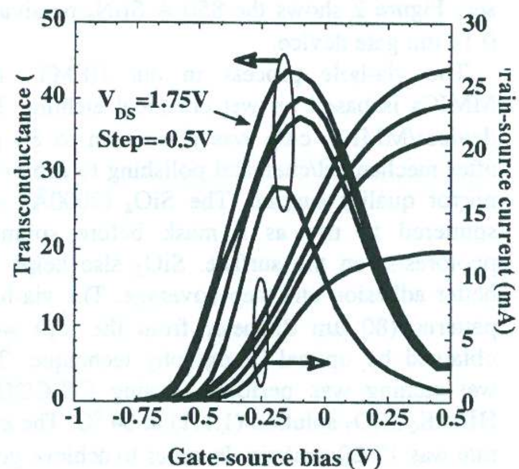


Fig. 4 Measured I-V (top) and transfer characteristics (bottom) of 0.1 x 100 μm^2 lattice matched InP-HEMT device

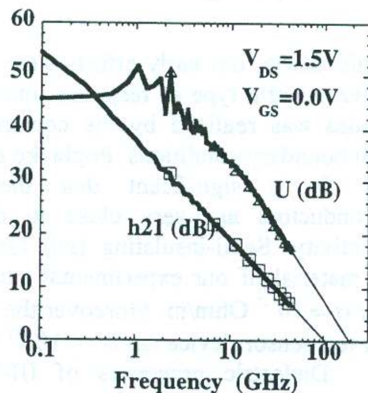
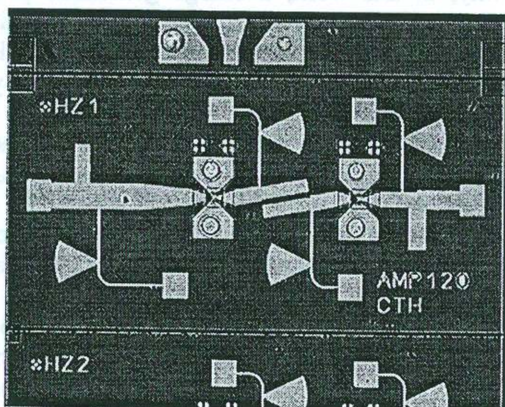


Fig. 5 A measured gain of 0.1 x 100 μm^2 AlInAs/GaInAs/InP HEMT



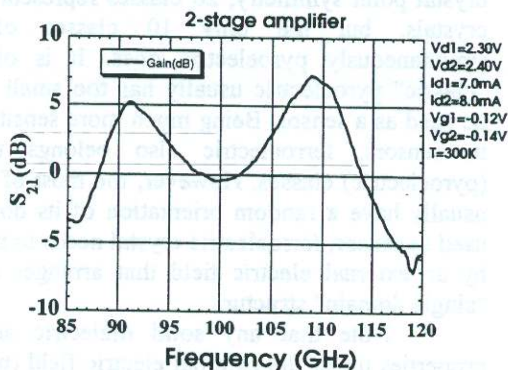


Fig. 6 Layout (top) and measured gain (S_{21}) performance of two stage W-band MMICs with a maximum gain at 109 GHz

IV. CONCLUSION

In conclusion, a novel, fast and reliable processes for making T-shaped gates, via-holes and passivation of HEMTs and MMICs have been developed. The gate process uses two PMMA layers and one PMGI resist layer which have completely selective developers that result in a large process window. Using this process scheme, gate lengths from 60 to 200 nm have easily been made in the same process step. The passivation process using sputtered Si_3N_4 is quite safe and via-holes process gives excellent uniformity. The processed InP-HEMTs show excellent dc and rf-performance. The processes have a good control of the gate lengths and give a high yield, and is therefore suitable for mass production of HEMTs and MMICs.

V. REFERENCES

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