Modeling of LT-GaAs and LT-$Al_{0.3}Ga_{0.7}As$ MISFET Devices

Rapeta V.V.V.J. Rao, T.C. Chong[†], L.S. Tan[†], W.S.Lau[†], J.J. Liou[‡]

Centre for Wireless Communications, National University of Singapore, Singapore
e-mail: cwcrjr@leonis.nus.edu.sg
WWW: http://www.cwc.nus.edu.sg
[†]Department of Electrical Engg., National University of Singapore, Singapore
[‡]Electrical Engineering Deptt., University of Central Florida, Orlando, Florida, USA

***Abstract* — A theoretical model is developed for LT-GaAs and LT-$Al_{0.3}Ga_{0.7}As$ MISFETs and is compared with experimental data. This model is based upon the analytical solution of Poisson's equation, the current continuity equation and the Chang-Fetterman velocity-field equation. When the device is operating in the linear region and knee region the one-dimensional Poisson equation has been considered. When the device is in the saturation regime, the two-dimensional Poisson equation has been solved analytically. The resulting output current-voltage characteristics are in excellent agreement with experimental data.**

I. INTRODUCTION

Metal-Insulator-Semiconductor GaAs Field Effect Transistors (MISFETs) with low-temperature (LT) grown GaAs or $Al_{0.3}Ga_{0.7}As$ as gate insulators have demonstrated remarkable power capability[1-5]. To our knowledge, however, there is currently no CAD model. A simple analytical model is required to describe the device behaviour for power amplifier circuit design, and at the same time taking into account of high field domain effect on the overall performance of the circuit. We have developed a reliable physical analytical model, which can be used for fast and economical design of power amplifier circuits. In our approach to developing an analytical model for LT-GaAs and LT-$Al_{0.3}Ga_{0.7}As$ MISFET devices, we used the Chang-Fetterman velocity-field equation[6], which gives a true physical description and an excellent approximation of the velocity-field dependence of GaAs. For the high-field domain in the saturation regime, we used the method developed by Chang and Fetterman[7] to solve the two-dimensional Poisson equation analytically. This paper is based on the model developed by Chang and Day[8] for GaAs MESFETs. We have calculated the MISFET *I-V* characteristics for LT-layer insulator thickness of 250Å and 500Å to demonstrate the insulator thickness dependence and compared with the experimental data.

II. MISFET MODEL DEVELOPMENT

The steady-state electron-drift velocity-field relation[6] used in this paper is

$$v = \frac{\mu E}{\sqrt{1+\left(\frac{E-E_0}{E_c}\right)^2 u(E-E_0)}} \qquad (1)$$

where v is the electron drift velocity, E is the electric field, μ is the low field mobility, $E_c=v_s/\mu$ is the critical field, v_s is the saturation drift velocity, $u(E-E_0)=1$ if $E \geq E_0$ and $u(E-E_0)=0$ if $E<E_0$, and

$$E_0 = \tfrac{1}{2}\left(E_T + \sqrt{E_T^2 - 4E_c^2}\right) \qquad (2)$$

where E_T is the threshold field at which the electron drift velocity attains the maximum value and over which the differential velocity becomes negative. The negative differential velocity of GaAs is due to the transfer of electrons from a high mobility, low-energy valley to a low mobility, high-energy valley. (2) is derived from (1) by setting $dv/dE\big|_{E=E_T} = 0$. In Fig. 1, the velocity-field dependence of (1) is compared to the experimental data by Ruch et al[9] and Houston et al[10] for μ=8000 cm^2/V-s, $v_s=8.5\times10^6$ cm/s and E_0=4 kV/cm.

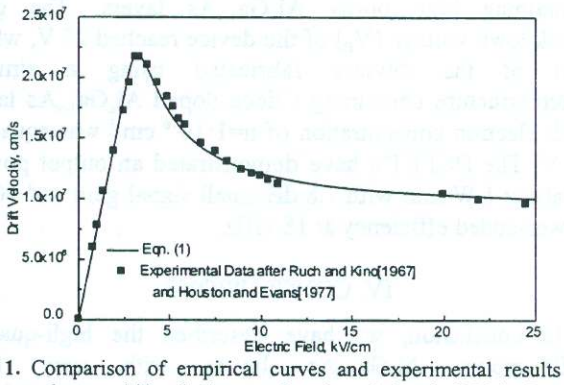

Fig. 1. Comparison of empirical curves and experimental results on electron drift velocity as a function of electric field in GaAs at 300° K.

Fig. 2 shows the structure of a GaAs MISFET. The analysis we present here is based on the usual assumptions, namely, we assume that the space charge region is entirely

devoid of carriers and that the semiconductor is of uniform n-type doping. Under the assumption of uniform doping and Lile's[9] model for the surface potential, ψ_s, the gate voltage, V_G, can generally be expressed as the sum of the voltage drop V_{ins} in the insulator, the surface potential, ψ_s, and the built-in voltage, V_{bi}:

$$V_G = V_{ins} + \psi_s + V_{bi} \tag{3}$$

Although the LT-layers are behaving like insulators the energy bandgap of these layers is the same as that of $Al_xGa_{1-x}As$ material. The Schottky built-in voltage, V_{bi}, is taken as the value determined for MESFET devices. V_{ins} is given by the expression,

$$V_{ins} = \frac{t}{\varepsilon_{ins}}(Q_s - Q_{ins} - Q_{ss}) \tag{4}$$

where Q_{ins} is the charge in the insulator due to arsenic precipitates and deep traps, Q_{ss} is the surface states charge, t is the insulator thickness, ε_{ins} is the permittivity of insulator and $Q_s=qN_Dh(x)$. q is the electron charge and N_D is the carrier concentration. $h(x)$ is the depletion width and is determined from the solution of one-dimensional Poisson equation:

$$V(y) = -\frac{qN_D y^2}{2\varepsilon_s} + \frac{qN_D h}{\varepsilon_s}\left(y + \frac{\varepsilon_s}{\varepsilon_{ins}}t\right) + V_0 \tag{5}$$

where $V_0 = V_G - V_{bi} - \frac{t}{\varepsilon_{ins}}(Q_{ins} + Q_{ss})$ and ε_s is the permittivity of GaAs.

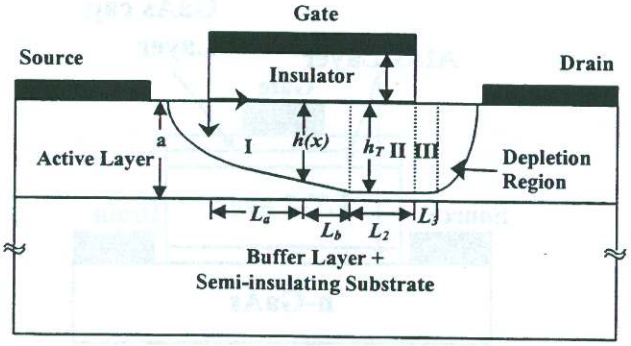

Fig. 2. Schematic diagram of a LT-GaAs/LT-$Al_{0.3}Ga_{0.7}As$ MISFET indicating the channel length, L, channel width, Z, and channel thickness, a.

For modeling purposes the device geometry has been divided into two regions, the area defined by the extremities of the gate, termed the intrinsic FET, and the area beyond the gate, which includes the source, drain, and unmodulated channel, termed the parasitic elements. Depending on the applied drain and gate voltages, the I-V characteristics of the MISFET can be divided into three regions: the linear region, knee region (or quasi-saturation region), and saturation region.

A. Linear Region

The channel current, I_c, in this region can be derived from the total current density in the channel by Ohm's law and using (1):

$$J_x = \sigma E(x) = q\mu N_D E_x(x) = qN_D v(x) \tag{6}$$

where σ is the channel conductivity for uniform doping concentration, $E_x(x)=dV/dx$ is the longitudinal electric field. The carrier transport area is given by

$$AREA = [a - h(x)]Z \tag{7}$$

Therefore the channel current can be expressed as

$$I_c = q(a - h(x))Z\mu N_D E_x(x) \tag{8}$$

Using expression $dV/dh = (qN_D/\varepsilon_s)(h + t(\varepsilon_s/\varepsilon_{ins}))$ derived from the one-dimensional Poisson equation, and integrating (8) from 0 to L, we obtain[11]

$$L = \frac{q^2 Z\mu N_D^2}{I_c \varepsilon_s}\left\{a\left[\frac{h_L^2 - h_0^2}{2}\right] - \left[\frac{h_L^3 - h_0^3}{3}\right] + \frac{\varepsilon_s}{C_{ins}}\left(a[h_L - h_0] - \left[\frac{h_L^2 - h_0^2}{2}\right]\right)\right\} \tag{9}$$

where $h_0 = h(x=0)$ and $h_L = h(x=L)$. h_0 and h_L can be calculated by applying the boundary conditions $V(h_0)=I_cR_S$ and $V(h_L)=V_D-I_cR_D$ in (5), where R_S and R_D are source and drain resistances respectively.

The maximum depletion width for the linear region h_a can be determined by substituting E_0 in (8) for $E_x(x)$. Using one-dimensional Poisson equation to determine h_L and with $h_L<h_a$, we can evaluate the maximum drain voltage for the linear region.

B. Knee Region

As the drain voltage increases, the electric field under the channel is not entirely below E_0. This means that we should divide the channel under the gate into two regions: $0<x<L_a$ with the electric field below E_0; and $L_a<x<L$ with the electric field between E_0 and E_T. L_a can be obtained from (9) by replacing h_L with $h_a=h(x=L_a)$. For $L_a<x<L$, the channel current is

$$I_c = qZN_D\mu\int_h^a \frac{E}{\sqrt{1+\left(\frac{E-E_0}{E_c}\right)^2}}dy \qquad (10)$$

Using expression $dV/dh=(qN_D/\varepsilon_s)(h+t(\varepsilon_s/\varepsilon_{ins}))$ and integrating (10) from $x=L_a$ to L and noting that $L_b=L-L_a$, we get

$$L_b=\frac{2V_p}{a^2E_T}\int_{h_a}^{h_L}\left(h+\frac{\varepsilon_s}{\varepsilon_{ins}}t\right)\left(1+\sqrt{(1+c^2)\beta^2-c^2}\right)dh \qquad (11)$$

where $\beta=qN_D\mu E_cZ(a-h)/I_c$, $V_p=qN_Da^2/(2\varepsilon_s)$, and $c=E_c/E_0$. The channel current I_c can be calculated from the equation $L=L_a+L_b$.

The electric field in the knee region is smaller than E_T. Suppose that at $x=L$, $E=E_T$ and $v=\mu E_T=\mu E_0(1+c^2)^{1/2}$. The maximum depletion width for the knee region h_T can be determined by substituting E_T in (8) for $E_x(x)$. Using (5) to determine h_T and with $h_L<h_T$, we can evaluate the maximum drain voltage for the knee region.

C. *Saturation Region*

If the drain voltage is increased further, the electric field in the channel at the drain side can become larger than E_T. . L_a can be obtained from (9) by replacing h_L with $h_a=h(x=L_a)$. For $L_a<x<L_a+L_b$, by replacing h_L with $h_T=h(x=L_a+L_b)$ in (11), one can determine L_b. We next need to solve the two-dimensional Poisson equation,

$$\frac{\partial^2V}{\partial x^2}+\frac{\partial^2V}{\partial x^2}=-\frac{qN_D}{\varepsilon_s} \qquad (12)$$

for the high-field regions, shown as regions II and III in Fig. 2, by using the boundary conditions $E_x(x,h_T)=E_T$ for regions II and III, continuity of the potential across the surface, transverse field vanishes at the channel, and the electric field along the channel is continuous for the determination of L_2, and L_3. The channel current can be calculated by using expressions for L_a, L_b, L_2, L_3, and $L=L_a+L_b+L_2$ for a given set of gate and drain voltages.

D. *Drain Current Calculation*

The drain current is given by[8]

$$I_D=I_c+\frac{V_D-I_c(R_S+R_D)}{R_P} \qquad (10)$$

where R_p is the parallel resistance associated with the buffer layer.

III. RESULTS

For verification of our model, we considered 250Å thick and 500Å thick LT-layer MISFET devices. The LT-layer is either LT-GaAs or LT-$Al_{0.3}Ga_{0.7}As$ sandwiched between two 100Å thick AlAs layers, which serve as barrier layers for the outdiffusion of excess arsenic. The top 100Å thick AlAs layer is capped with 100Å thick undoped GaAs layer grown at conventional temperature. Therefore, the total gate insulator system consists of 100Å GaAs cap Layer/100Å AlAs layer/LT-layer/100Å AlAs layer. All the LT-layers in this study were grown at 280°C and subsequently *in-situ* annealed at 600°C for 10mins under As_4 overpressure. All the conventional layers were grown at 600°C. The active layer consists of a 1800Å thick GaAs layer doped to $2.2\times10^{17}cm^{-3}$ with Si. A cross-section of the fabricated MISFET structure is shown in Fig. 3. Fabrication of the MISFET structures were reported elsewhere[12]. The saturation drift velocity, v_s, was taken as 7×10^6 cm/s for all the samples. In our calculations Q_{ss} has been taken as 0 C/cm^2. The built-in voltage, V_{bi}, has been taken as 0.8 V. The rest of the parameters used for calculating the theoretical curves are listed in Table 1. The measured and calculated results for the MISFETs are shown in Fig. 4. They are in close agreement thus validating our analytical model. The model we have developed demonstrates clearly the dependence of LT-layer thickness on device characteristics.

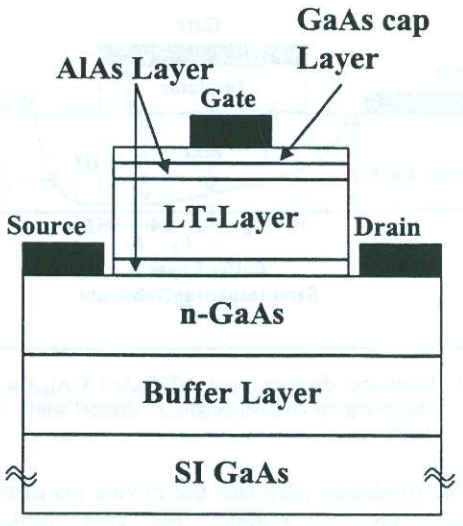

Fig. 3. Schematic diagram of the fabricated MISFET structures.

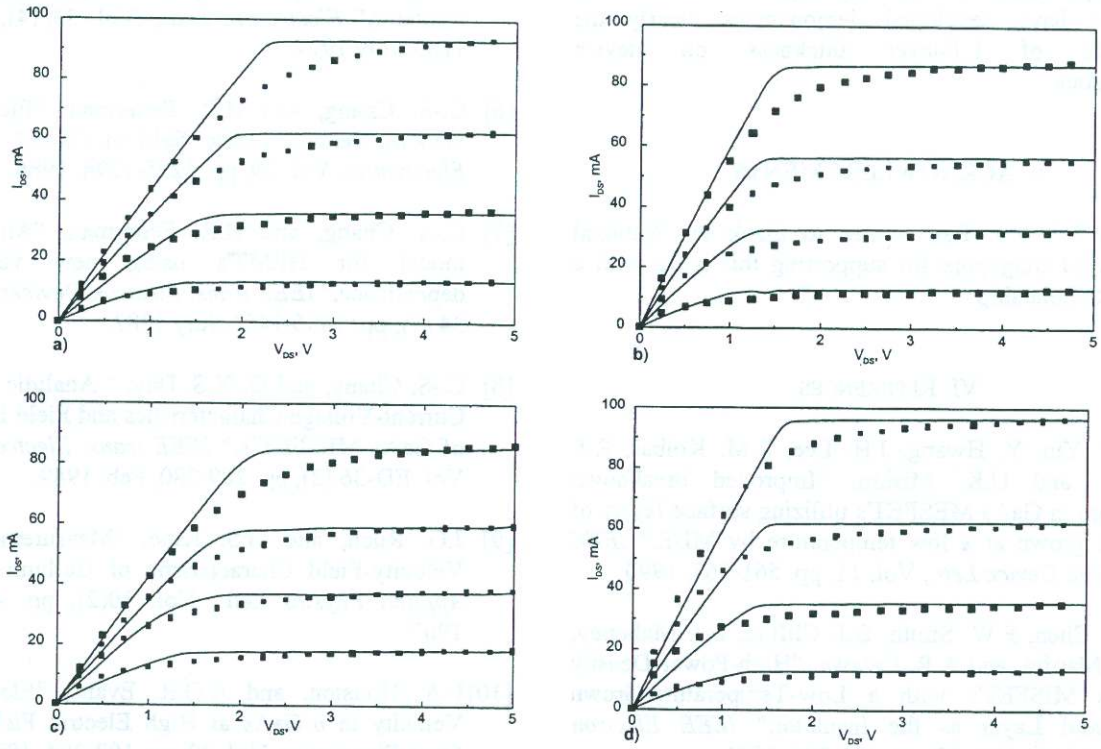

Fig. 4. Comparison of the theoretical (solid line) and measured (solid square) results of drain current versus drain voltage for four different gate voltages (2V,0V,-2V,-4V): a) 500 Å thick LT-$Al_{0.3}Ga_{0.7}As$ MISFET device b) 250 Å thick LT-$Al_{0.3}Ga_{0.7}As$ MISFET device c) 500 Å LT-GaAs MISFET device d) 250 Å LT-GaAs MISFET device.

Table 1. The parameters used for calculating the theoretical curves.

LT-layer	E_T (V/cm)	μ (cm^2/V-s)	N_T (cm^{-3})	R_D/R_S (Ω)	R_P (kΩ)
250Å LT-GaAs	4100	4000	7.2×10^{17}	5	10
500Å LT-GaAs	4100	3900	3.6×10^{17}	8	5
250Å LT-$Al_{0.3}Ga_{0.7}As$	3800	4000	7.2×10^{17}	5	10
500Å LT-$Al_{0.3}Ga_{0.7}As$	4000	4000	3.6×10^{17}	8	10

N_T : Traps or equivalent As-precipitates concentration

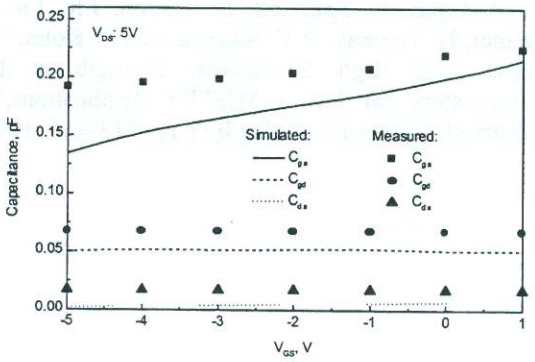

Fig. 5. Comparison of intrinsic capacitances C_{gs}, C_{gd}, and C_{ds} between simulated and measured data.

Three distinct capacitances which relate incremental changes in charge to incremental terminal voltages are calculated. Fig. 5 shows these three capacitances versus gate bias for a fixed drain voltage of 5V. These results clearly show that both experimental and measured results exhibit similar kind of trends. The discrepancies in the magnitudes of the measured and calculated values of C_{gs}, C_{gd}, and C_{ds} are within the experimental error.

IV. CONCLUSIONS

An accurate quasi-analytical model for the output *I-V* characteristics of LT-GaAs/LT-$Al_{0.3}Ga_{0.7}As$ MISFET's was described. Theoretical calculations for *I-V* characteristics using our model are in excellent agreement with the experimental data. This model can also be used to

derive the bias-dependent small-signal parameters such as transconductance, and gate capacitances in order to predict the device performance under large signal conditions. The model we have developed demonstrates clearly the dependence of LT-layer thickness on device characteristics.

V. ACKNOWLEDGMENTS

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