Influence of recess extension on double heterostructure metamorphic HEMT for power application at 60 GHz

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This paper presents the influence of the recess extension on the power performance of double heterostructure $Al_{0.65}In_{0.35}As/In_{0.35}Ga_{0.65}As/GaAs$ metamorphic HEMT's in the millimeter wave range. Depending on the recess extension, devices exhibit an extrinsic cut-off frequency varying from 80 to 120 GHz. Output power measured at 60GHz with passive load pull bench can reach a power density of 340mW/mm with 6.5 dB linear gain and 21%PAE.

INTRODUCTION

For low noise and power applications in the millimeter wave range, AlInAs/GaInAs/GaAs metamorphic HEMT is a good alternative to pseudomorphic HEMT (GaAs substrate) or lattice matched HEMT's (InP substrate). On InP, record cutoff frequencies up to 400GHz have been obtained [1,2,3]. Increasing the Indium contents of the channel permits to obtain more velocity but reduces breakdown. So it should be optimized to obtain the best trade off between cutoff frequency and a high voltage breakdown necessary for power amplification purposes. Realization of lattice matched devices is only possible with an InP substrate which is more expensive and brittle than GaAs substrate and only for an Indium contents near 50%. Several studies in our laboratory show that the best results for power amplification are obtained with an Indium content close to 30% [4]. One possibility to aim this Indium ratio is using a metamorphic structure associated with a GaAs substrate. For this kind of devices, the active layers are grown on a compositionally grade metamorphic layer. This buffer layer permits to lattice any GaInAs channel Indium content.
To our knowledge the best published result at 60 GHz has been obtained by Sanders[5]. They have designed a MMIC based on metamorphic HEMT on GaAs substrate. This MMIC can provide 305mW/mm with 41% PAE.

If a large work has been done [6,7] to optimize epilayers for power applications in millimeter waves range, no complete study was done concerning the recess topology. This paper presents the performances of a double heterostructure $Al_{0.65}In_{0.35}As/In_{0.35}Ga_{0.65}As/GaAs$ metamorphic HEMT's with 4 different topologies of recess.

After describing the epilayer and the technological process, all characterisation results are presented, including the large signal measurements performed at 60 GHz.

EPILAYER AND TECHNOLOGICAL PROCESS

Metamorphic $In_{0.35}Al_{0.65}As/In_{0.35}Ga_{0.65}As$ HEMT layers (MM-HEMT) were grown by solid source molecular beam epitaxy on two inch GaAs (100) substrates. A schematic cross section of the epitaxial structure of the MM-HEMT is shown in figure 1.

Layer	Thickness
$Ga_{0.65}In_{0.35}As$ 6×10^{18} cm^{-3}	25 nm
$Al_{0.65}In_{0.35}As$	20 nm
δ_{1Si} : 7.5×10^{12} cm^{-2}	
$Al_{0.65}In_{0.35}As$	5 nm
$Ga_{0.65}In_{0.35}As$	15 nm
$Al_{0.65}In_{0.35}As$	5 nm
δ_{2Si} : 1.8×10^{12} cm^{-2}	
$Al_{0.65}In_{0.35}As$ buffer	300 nm
$Al_{1-x}In_xAs$ graded buffer	
GaAs substrate	

Figure 1: Epilayer struture

Hall effect measurements are used to determine the sheet carrier density (Ns) and electron mobility (μ_n). At 300 K, we measured a typical Ns of 3.5×10^{12} cm^{-2} with a corresponding μ_n of 8000 cm^2/V.s. At 77 K the mobility

increased to about 23000 $cm^2/V.s$ while the sheet density remained the same.
T-gate devices were fabricated. They were isolated by Mesa formation using wet chemical etching ($H_3PO_4/H_2O_2/H_2O$). Ge/Au/Ni/Au was electron beam evaporated for the ohmic contacts and followed by a rapid thermal annealing. The typical ohmic contact resistivity was on the order of 0.15 Ω·mm. The devices have a double recess structure. The first recess was realized by dry etching while the narrow recess was realized by wet etching using a selective succinic acid and hydrogen peroxide solution. The 0.15-µm T-gates were defined by electron beam lithography using a bi-level resist profile and the Ti/Pt/Au gate metalization was electron beam evaporated.

Finally, devices are passivated using PECVD Si_3N_4 for stabilising the AlInAs surface. The recess topology is shown in figure 2. The gate lengths is 0.15µm and 0.1µm for the devices tested and two gate widths were used : 2*25µm and 2*50µm.

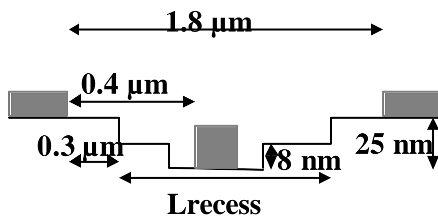

Figure 2: Recess extension definition

Lrecess is the length of the first recess extension. Four different Lrecess are studied in this paper : 0.3µm 0.6µm 0.9µm and 1.2µm.

DC MEASUREMENTS

First, I-V characteristics were plotted for each device. The highest current density measured is 540mA/mm at Vds=2V and Vgs=0.6V. This value was reached with the narrowest recess extension and decreases as the recess extension increases. This is shown in figure 3 for a gate development of 2*25µm*0.15µm.

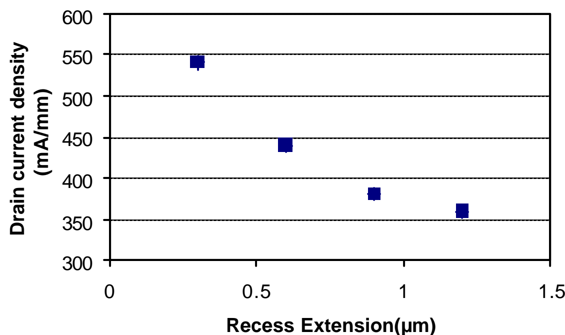

Figure 3: Drain current density versus recess extension

This decrease is attributed to surface effects which induce parasitic extension of the depletion area under the second gate recess.

Then, breakdown measurements (shown in figure 4) were performed in diode configuration.

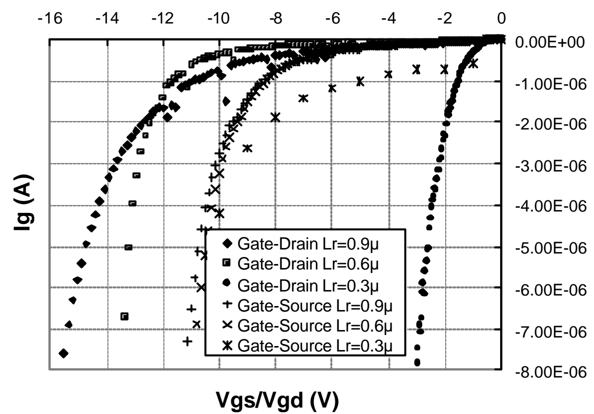

Figure 4: Reverse characteristic for both gate-drain and gate-source in diode mode

As expected, a reverse voltage between gate and source higher than 10V can be applied for all the components. For the gate-drain diode the results are quite similar except for the devices with the smaller recess extension which have a maximum reverse voltage that is not better than 4V . This result will limit the highest drain to source voltage that can be applied for power amplification applications.

Breakdown characteristics in transistor mode have also been plotted for all the components to see the influence of impact ionization in the channel. For all the components it is difficult to obtain the well known bell-shaped curves that characterize impact ionization effect. It is certainly because the high leakage current of the gate-drain and gate-source diodes in transistor mode "hides" the ionization effect, that involves a smaller reverse gate current. That means there would be no real influence of the impact ionization effect in the channel for power applications with these devices. A high current due to ionization impact limits the maximum power that can be delivered by the transistor because of the increase of the reverse gate current near the A class bias point [8,9]

RF MEASUREMENTS

Scattering parameters were measured up to 40 GHz to determine the potentialities of devices (gains) and the small equivalent circuit using a well known home method [10]. Additionnal Sij measurements were performed in the 50-75 GHz band

Two representative parameters of the device RF behavior have been studied in this paper : MAG (Maximum available Gain) measured at 60 GHz and intrinsic transconductance gm deduced from measurements in the 0-40 GHz band (figure 5). The results clearly demonstrate that RF parameters are better as Lrecess decreases.

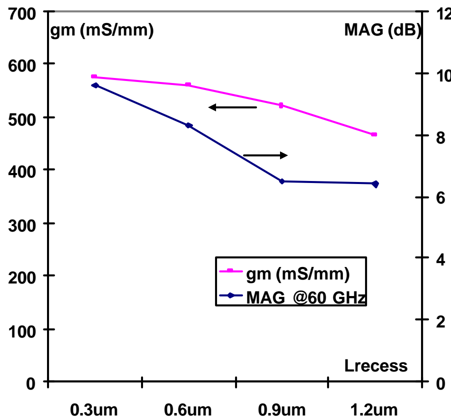

Figure 5 : Intrinsic gm and MAG vs Lrecess

Further measurements have shown the same evolution for f_T. As it has been said yet for breakdown characteristics, a parasitic extension of the depletion area due to surface effects appears between gate and drain. The wider the recess is, the larger this extension is, increasing the effective gate length. Thus, it can explain why better RF parameters are obtained with the smaller recess extension.

Large signal measurements will give information on the global performance of the device, considering together the opposite aspects for power : large recess for high breakdown and small recess for RF parameters.

LARGE SIGNAL MEASUREMENTS

Large signal measurements were performed at 60 GHz using a passive load pull bench. The device is on wafer tested. Coaxial to rectangular waveguide transition is done just after the probes. Manual waveguide tuners are used to present the different input and output loads. Optimal matching is considered when output power is maximum. Corrections are performed to obtain the power gain and the drain output power. To compare power capabilities, devices have been tested at different bias points, and the response is systematically stopped as the gate current density reaches 1mA/mm.

A typical result is given in figure 6. Maximum output power density is 340mW/mm at 60GHz, with 6.7 linear

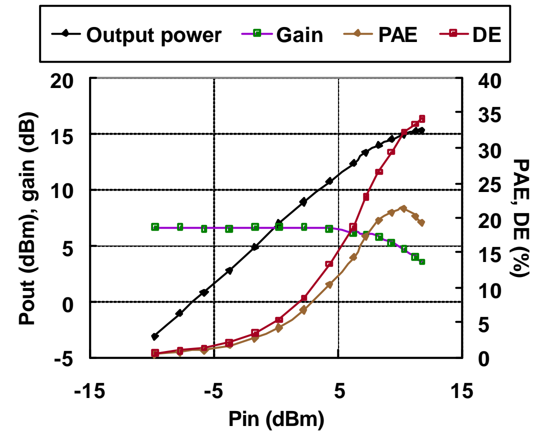

*Figure 6 : Power response of a device (2*50µm*0.1µm gate) at 60 GHz. Biasing point is Vds=3V ; Vgs= 0.2V*

dB gain and 35 and 21% of drain efficiency and PAE respectively with bias point at Vds=3V and Vgs=0.2V.

This device demonstrates a very good linearity and the P_{1dB} obtained is 220mW/mm. This value is close to P_{max} so large power can be raised with only a small loss of linearity.

Large signal measurements were done on several devices with several Lrecess parameters. Figure 7 shows maximum power density for the four different recess extensions and for two values of gate length 0.1µm and 0.15µm. The gate development of the transistors tested is 2*50µm. We can notice that the maximum power density decreases as the recess extension decreases. The results in term of power density for the two different gate lengths are similar but the very best value was obtained with the 0.15µm gate length.

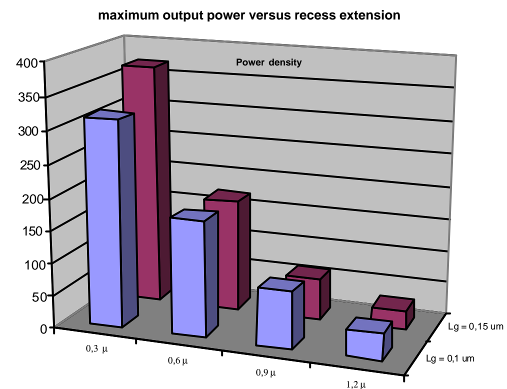

Figure 7 : Comparison of output power density (mW/mm) at 60 GHz versus Lrecess

To compare results of all the devices in term of linearity we have defined a linearity criterion expressed as the

ratio of Pmax and P1dB or Pmax(dBm) - P1dB (dBm) in dB. Figure 8 compares the linearity performance of the devices using this criterion; we can also notice that the best value is always obtained with the narrowest recess. For all the other recess extension it seems that a value of 0.1µm for gate length give slightly better results than 0.15µm

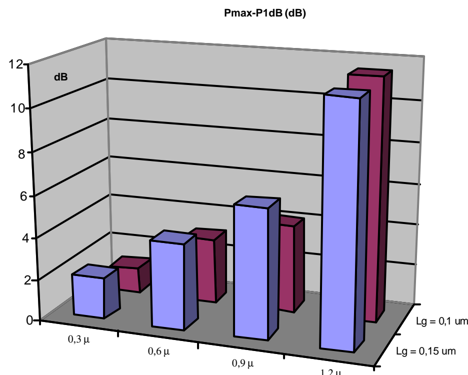

Figure 8 : Influence of Lrecess on the linearity criterion Pmax (dBm) – P1dB(dBm)

As a conclusion, large signal measurements have shown that a value of 0.3µm for Lrecess gives very good results in term of maximum power density and a very good behaviour in term of linearity.

CONCLUSION

In this paper, we investigate the influence of the double recess extension on power performance at 60GHz of metamorphic HEMT's. Measurements have demonstrated, as expected, a good breakdown behavior of the devices with the largest recess extension but poor power performance. Despite of a worse reverse drain-gate DC characteristic, devices with the smallest Lrecess have given a very good maximum power at 60GHz with highly linear gain and better MAG and Gm. This shows that if a good breakdown behavior of the components generally expected for power amplication is important to rise a high output power, the RF behavior of the devices is essential. The study made in this paper clearly demonstrates that increasing the recess extension improves DC reverse characteristics of the HEMTs but degrades RF gains, maximum current density and large signal behavior.

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