Nonlinear characterization of microwave transistors by the means of pulsed I(V) and pulsed S-Parameters measurements

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***Abstract*—A versatile pulsed I(V) and 40 GHz pulsed S parameters measurement system of microwave transistors is described. Capability of discrimination between thermal and trapping effects with a pulse set-up is demonstrated. A method to measure electrically the thermal resistance and capacitance of transistors with a pulse set-up is proposed. Finally, it is explained how to derive transistor nonlinear characteristics from these measurements for modeling purposes.**

I. INTRODUCTION

Between the physics of transistors and the efficient CAD of high performance active MMICs, the characterisation and modeling of transistors is an essential key point. The transistor models for first-pass CAD success have to take into account I(V) characteristics, RF characteristics, thermal characteristics, slow dynamics characteristics. In other words, an up-to-date model is nonlinear and non quasi-static. Numerical analysis of inner transistors is helpfull to understand electronic and/or thermal phenomena, but the results of 2D or 3D analysis usually need to be calibrated by measurements. Time consumption of simulations with physics-based model is still prohibitive for design engineers.

Thus, an efficient nonlinear model of microwave transistors is a based on measurements [1][2]. The various intrinsic phenomena (current gain, breakdown, diode conduction, trapping effects, thermal effects...) must be clearly separated during the characterisation processes and at the level of the model equations and/or topology. Up-to-date nonlinear measurement techniques of microwave transistor are pulsed I(V) measurements, pulsed S-parameters measurements, multiharmonic active load-pull measurements in CW or pulsed mode, time domain RF measurements. For the time beeing, pulsed I(V) and pulsed S-parameters are intensively used for model derivation, and load-pull or time domain measurements are used for device and/or model verification. The main reason for that is the capability of pulsed set-up to separate phenomena.

This paper will describe a 40 GHz pulsed I(V) and pulsed S-parameters measurement system, and the associated measurement-based modeling method.

II. PULSED I(V) and S-PARAMETERS MEASUREMENTS

The characterization of microwave devices should be realized with measurement conditions as close as possible to the final operating conditions (thermal state, traps...), with the capability to perform accurate acquisitions of nonlinear characteristics. This simple idea is the foundation of the pulsed measurement principle. A number of pulsed I(V) or pulsed S-parameter systems have been proposed [3]-[7]. They rely on the measurement of I(V) and RF data during short rectangular pulses describing the characteristics around the DC bias point.

Starting from the DC bias point, short pulses describe isothermally the device behavior. Pulses from 150 ns to 1 µs are used, depending on the device. The measurement principle for a FET is shown in Fig. 1. Vgs0, Vds0 and Id0 correspond to the quiescent point, and Vgsi, Vdsi, Idi are the pulsed point values. The device temperature changes slightly during the pulses (depending on the dissipated power

during the pulse versus the DC bias dissipated power), and returns to the bias temperature after a few µs. Approximately 200 pulsed points are required in order to plot the complete nonlinear input and output characteristics of a transistor for a DC bias point.

A given transistor has absolute ratings provided by its manufacturer, the pulse measurements can overrun these ratings up to breakdown. Pulses up to 100 Volts or 7 Amps are available on our setup, and the bias level can be up to 50 Volts. Matching resistor networks at the input and output of transistors are adjusted in order to limit the currents and to optimize the generators and measurement accuracy.

The pulse duration, delay, transition and duty cycle must be adapted to the DUT, as a compromise :
– pulse width must be large enough for the quality of measurement acquisition,
– pulse width must be much smaller than thermal time constant for quasi isothermal characterization,
– pulse width must be smaller than trapping time constant, if traps exist,
– pulse duty cycle must be large enough to ensure the thermal state is driven by the DC quiescent point,
– large overshoots of voltage must be avoided by the mean of pulse delay and transition settings.
A duty cycle of 0.1 % to 5 % is usually acceptable, but it must be checked for each transistor. Pulse width from 300 ns to 600 ns are usually a good trade-off.

Temperature dependance of transistors is of prime importance, the temperature is a command of active devices. Thermal measurements are made with the control of the device external temperature (with a thermal enclosure or a thermal wafer chuck). If thermal resistance(s) and thermal time constant(s) (several Rth/Cth pairs can be considered for intrinsic device, substrate, radiator...) of a transistor are available, circuit simulators can compute the device temperature and feed it back to the model [8].

Small signal pulsed S-parameters are performed by superposition of RF stimulus and measurement during the I(V) pulses. A vectorial network analyzer with short pulses capability is used for isothermal measurements of transistors. The RF source is modulated with an on/off rectangular stimulus signal synchronized with I(V) pulses. We can notice that a pulsed mode for a network analyser diminishes the accuracy of acquisitions (the RF average energy injected in the DUT is divided by the duty cycle). All classical calibration methods are available for pulsed measurements, with their respective advantages and drawbacks (Standard, LRL, LRM, LRRL...). Fig.1 summerizes the hardware organization of the pulsed set-up.

III. NONLINEAR PHENOMENA CHARACTERIZATION AND MODELING

Three frequency domains are to be considered : I(V) DC nonlinear behavior, RF nonlinear behavior and slow dynamics (thermal, trapping effects) at intermediate frequencies. The key point is to characterize separately and accurately each phenomena, and to derive a unique model with a consistent behavior from DC to RF.

DC characteristics are usefull to compute the quiescent bias point, they contain the nonlinear characteristics of drain (or collector) current generator of transistors. Self-heating of transistors is unavoidable, it is a drawback for two reasons. On one hand, it modifies I(V) characteristics, they are not equithermal, thus they can not be used to model a RF cycle (fig. 2). On the other hand, the self-heating can damage the device, very hot domains or breakdown characteristics can not been investigated by DC measures.

Pulsed I(V) characteristics are performed at an intermediate frequency domain, the small thermal drift during pulses can be neglected. Thus, from I(V) pulsed measurements, we can derive isothermal I(V) characteristics that are consistent with the RF nonlinear Gm and Gd characteristics (if no trapping effects occur). Breakdown and dangerous domains of characteristics can be investigated by short pulses. Slow dynamics due to trapping effects can be put in evidence (ie capture of electrons in MESFETs can occur during pulses, but emissions of traps can not been completed fig. 3 [9][10]). Pulsed I(V) measurements

give a way to separate thermal and trapping effects, all trapping effect characterizations are performed at a constant temperature, and all thermal characterizations are performed for a given level of traps. Thermal measurements under pulsed conditions take advantage of the embedded Schotkky diode of FETs (or the base-emittor diode for HBTs) for temperature determination. The calibration of the voltage of diode conduction versus temperature with a thermal enclosure and the measurement of the self-heating versus the dissipated DC power give the thermal resistance of devices (fig. 4). Moreover, the analysis of characteristic drifts during pulses (Vbe voltage for HBTs, RF gain for FETs) determines the thermal time constant of intrinsic devices [8][11] (fig. 5).

Pulsed RF measurements are performed during the steady-state of I(V) pulses. With small signal broadband (2 Ghz to 40 Ghz) measurements of transistors, one can extract or optimise an equivalent scheme of intrinsic device, after extrinsic elements removal (determination of extrinsic elements is an other question, key points can be found in [12] [13]). The intrinsic scheme determination is performed for each pulsed point of I(V) characteristics, thus the nonlinear behavior of elements (ie Cgs, Gm, Gd, Ri, Cbe, Cbc...) is detetermined versus the command voltages and for the DC bias point.

The pulsed I(V) and pulsed RF measurements can be performed for several bias points (A, AB, B,.. class) and for several surrounding temperatures. A unique set of model parameters for a given transistor is able to describe all its hot uses, including radar pulses. Only three commands are to be considered in a nonlinear model ot transistor : two voltages and the temperature. This approach provides versatile models that handle self-biasing, self-heating and trappings effects dynamically.

We use an equivalent scheme description for the intrinsic part of transistors. At least, two good reasons can be invocated : ease of introduction in modern CAD softwares, capability to model thermal and trapping effects as new sub-circuits of the equivalent scheme. Resistance-capacitor time-constants of thermal effects (and, if required, of trapping effects) will modify the nonlinear behavior of the model versus frequency from DC to RF. Nonlinear characteristics of elements are modeled by equations with optimization of parameters or by approximation splines. Integration of charges is required for 2-dimensionnal reactive elements like Cgs(Vgs,Vds). The thermal dependance of each nonlinear element is taken into account. This approch allows to use the same model in differents circuit simulator algorithms : HB, time domain, transient envelope. A nonlinear versatile FET model including breakdown, thermal effets, trapping effects is proposed fig. 6.

Some measure and/or model results are now proposed. First, the modeled output impedance of a MESFET versus frequency(fig. 7) : we can notice, from DC to RF, the effect of thermal and trapping time constants. Fig. 8 shows trapping effects due to DC bias point on I(V) characteristics, measure and model are compared ; fig. 2 demonstrate the DC capability of the model. Fig. 9 shows the capability of an electrothermal model with two thermal resistances to represent the crunch phenomenon. Comparisons of RF measurements (from multi-harmonic or multi-tone load-pull characterization) and simulations with transistor models including slow dynamics present very good agreements for large signals, with an improved confidence in simulation results.

Conclusion

Pulsed measurement techniques have proven their capabilities to characterize accurately, efficiently and separately various nonlinear phenomena in microwave transistors. Models derived from these measurements implement clearly each phenomenon, thus they reach an improved versatility. They handle accurately a large number of electrical conditions (DC to RF, various biasing conditions, various RF signals) with a single set of parameters. The measurement and modeling techniques described in this paper are used daily for CAD of up-to-date nonlinear MMICs.

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Figures

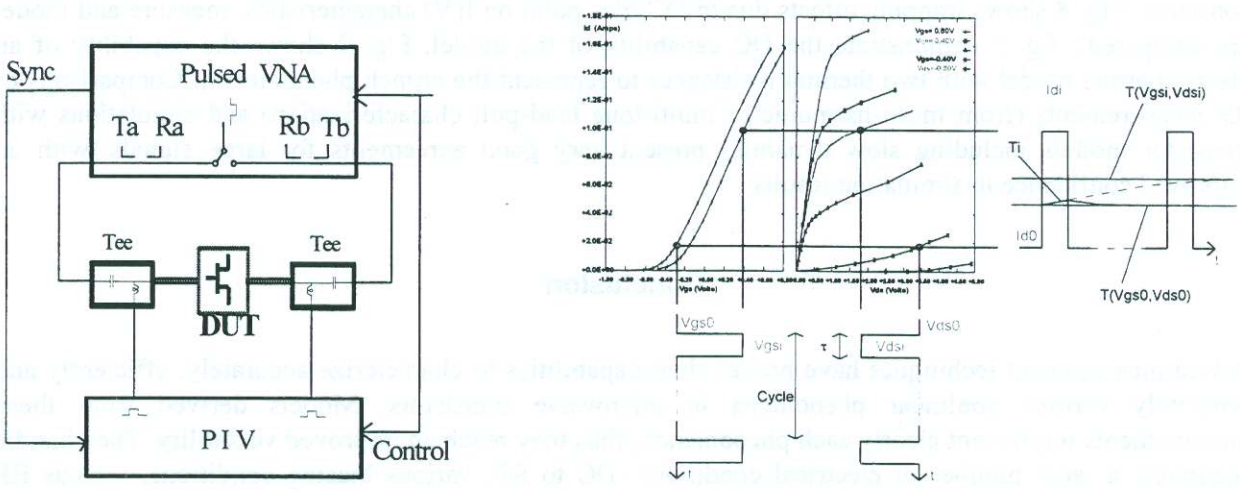


Figure 1 : Pulsed set-up and pulsed measurement principle

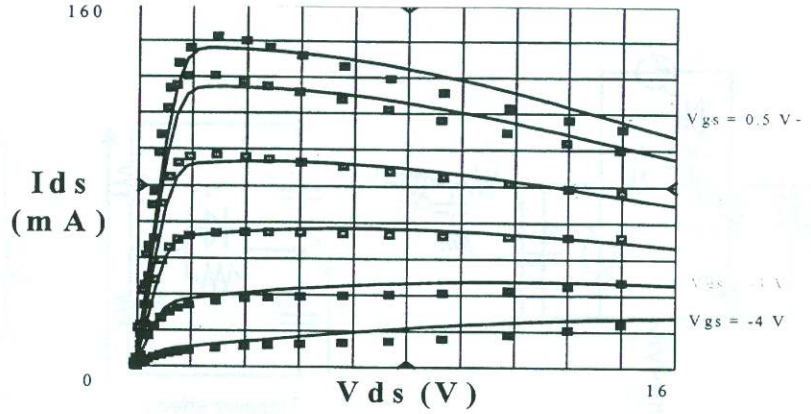


Figure 2 : I(V) DC measurements (points) and model(lines)

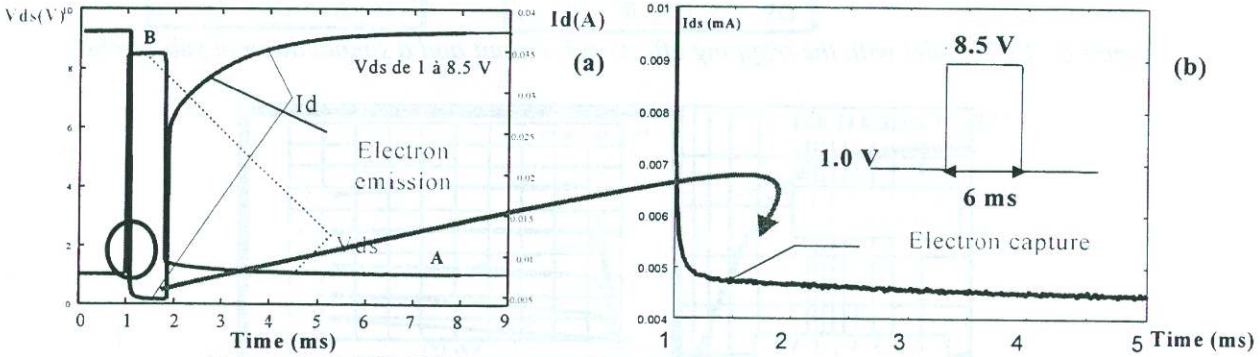


Figure 3 : MESFET Trapping effects : emission and capture of electron

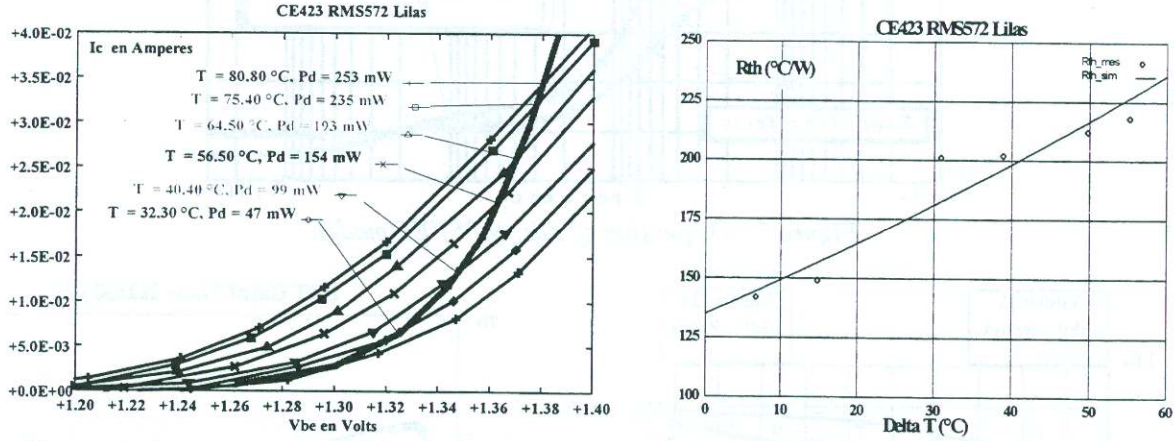


Figure 4 : Determination of Rth for HBT (comparison of DC and pulsed Ic(Vbe) characteristics)

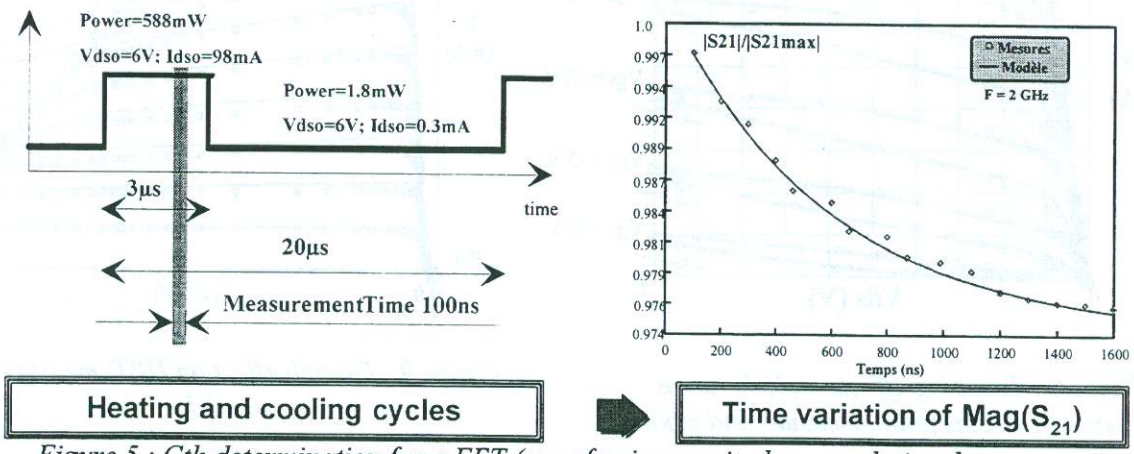
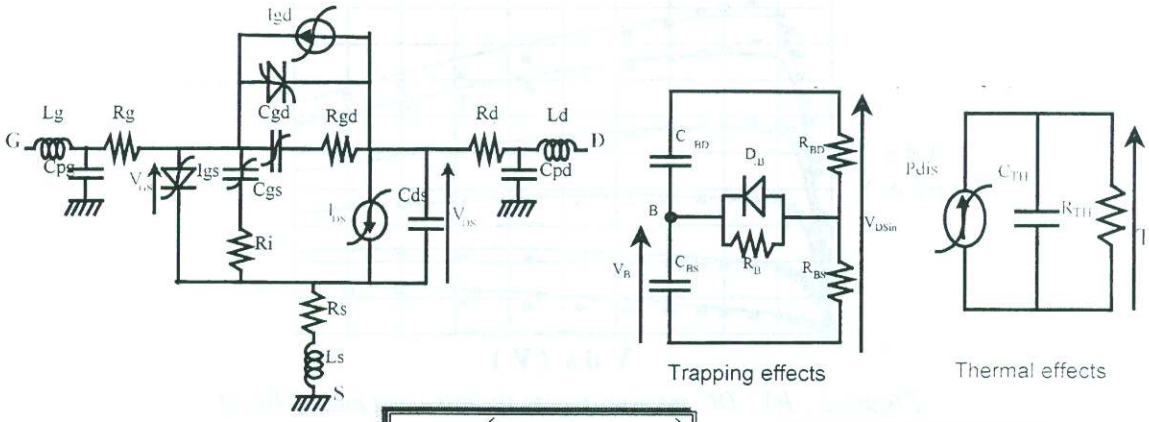


Figure 5 : Cth determination for a FET (use of gain magnitude as a relative thermometer)



$$I_{DS} = f\left(V_{GS\_B}, V_{DS}, T\right) \qquad V_{GS\_B} = V_{GS} - \alpha_B \times V_B$$

Figure 6 : FET model with the trapping effects sub-circuit and a simple thermal sub-circuit.

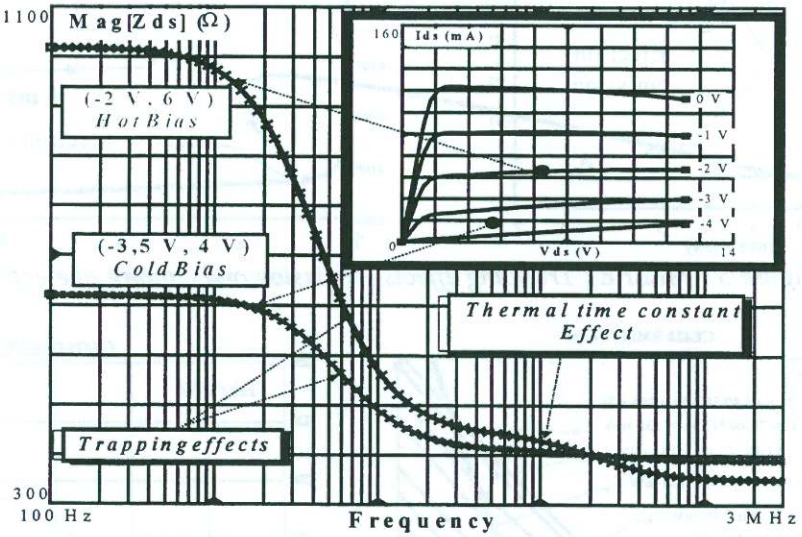


Figure 7 : Dispersion of Zds, MESFET model.

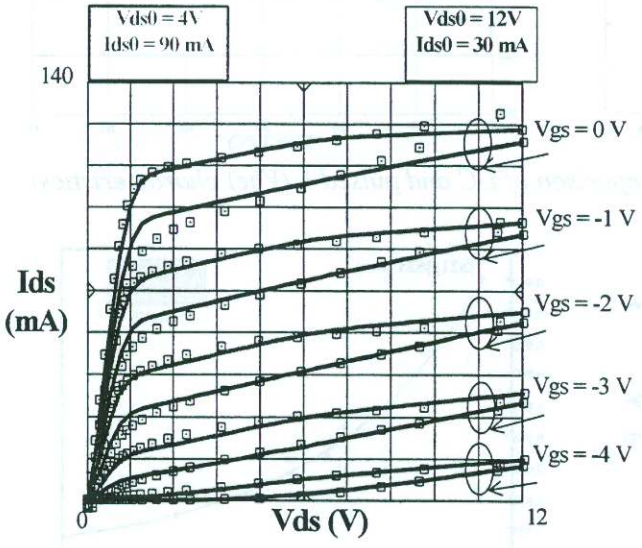


Figure 8 : Trapping effects on I(V) versus isothermal DC bias point, measure and model

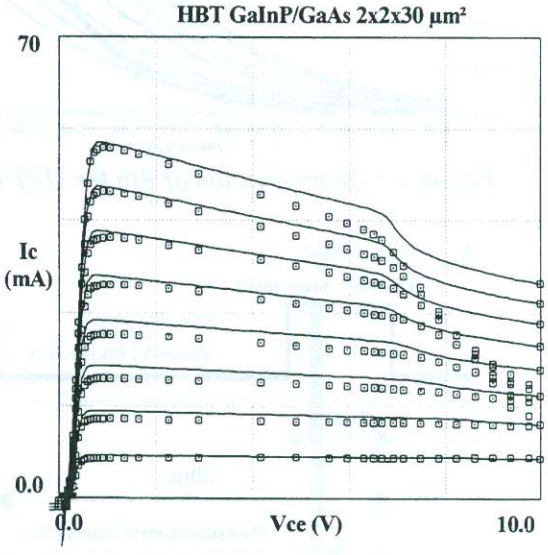


Figure 9 : Crunch effect on HBT, measure and model