Analysis of Correlation between Breakdown Characteristics and Gate-Lag Phenomena in Narrowly-Recessed-Gate GaAs MESFETs

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Effects of surface states on breakdown and gate-lag phenomena in narrowly-recessed-gate GaAs MESFETs are studied by two-dimensional (2-D) analysis. It is shown that the breakdown voltage could be raised when moderate densities of surface states are included. However, in a case with relatively high densities of surface states, the breakdown voltage could be drastically lowered when introducing a narrowly-recessed-gate structure. It is suggested that there is a trade-off relationship between raising the breakdown voltage and reducing the gate-lag.

INTRODUCTION

To understand high-voltage phenomena in GaAs MESFETs and HEMTs, such as drain-to-source breakdown, is very important for realizing high-performance microwave power devices and ICs, which are now receiving great interest, particularly for mobile communication applications. To achieve high breakdown voltages, so-called a recessed-gate structure has been utilized (Walker (1)), where the existence of surface depletion layer due to surface states is regarded as an origin of the high breakdown voltage. On the contrary, recently, the (narrowly) recessed-gate structure is used to reduce surface-state-related anomalies such as frequency-dependent transconductance and gate-lag (Kohno et al (2), Wakabayashi et al (3)). So, in this work, to get a detailed insight into recess effects and surface-state effects on the breakdown and gate-lag phenomena, we have made 2-D simulation of narrowly-recessed-gate GaAs MESFETs including surface states. As a result, we have found that the breakdown voltage could be rather lowered in some cases by introducing the recess structure, and that there may be a trade-off relationship between raising the breakdown voltage and reducing the gate-lag.

PHYSICAL MODEL

Fig.1 shows a modeled device structure analyzed here. The surface states are considered on the planes between source and gate and on the planes between gate and drain. As a surface-state model, we adopt Spicer's unified defect model (Spicer (4)), and assume that the surface states consist of a pair of deep donor and deep acceptor and they distribute uniformly within 5 Å from the surface. As to their energy levels, the following case based on

experiments is considered as in previous works ((3), Horio and Wakabayashi (5)): $E_{SD} = 0.87$ eV, $E_{SA} = 0.7$ eV (Wieder (6)). Here E_{SD} is energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is energy difference between the deep acceptor's energy level and the top of valence band.

Basic equations to be solved are Poisson's equation, continuity equations for electrons and holes, and rate equations for the deep levels. They are expressed as follows ((3), (5)).

1) Poisson's equation

$$\nabla^2 \psi = -\frac{q}{\varepsilon}(p - n + N_D - N_A + N_{SD}{}^+ - N_{SA}{}^-) \qquad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n + G - (R_{n,SD} + R_{n,SA}) \qquad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p + G - (R_{p,SD} + R_{p,SA}) \qquad (3)$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{SD} - N_{SD}{}^+) = R_{n,SD} - R_{p,SD} \qquad (4)$$

$$\frac{\partial}{\partial t}N_{SA}{}^- = R_{n,SA} - R_{p,SA} \qquad (5)$$

where $N_{SD}{}^+$ and $N_{SA}{}^-$ represent ionized densities of surface deep donors and surface deep acceptors, respectively. R_n and R_p are the electron and hole loss rates via the deep levels, respectively, and the subscript (SD, SA) represents the corresponding deep level. G represents a carrier generation rate by impact ionization.

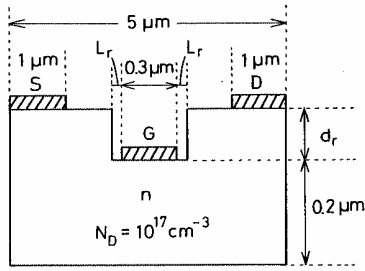The above equations are put into discrete forms and are solved numerically.
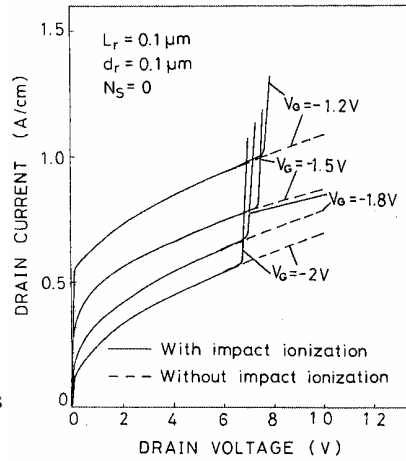

Fig.1 Modeled recessed-gate GaAs MESFET analyzed here.

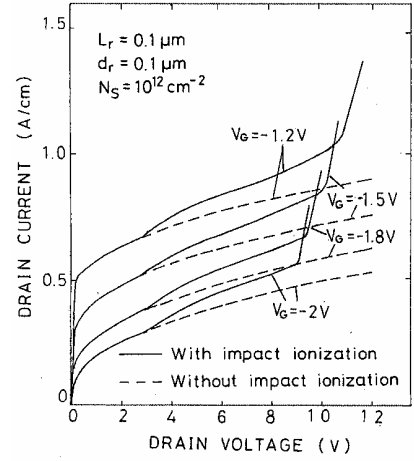**Fig.2** Calculated drain characteristics of a recessed-gate GaAs MESFET. Surface states are not included.

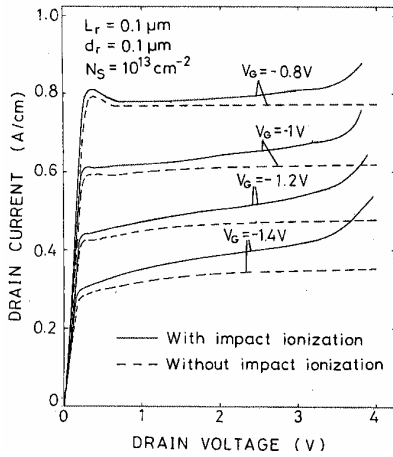**Fig.3** Calculated drain characteristics of a recessed-gate GaAs MESFET with low surface-state density of 10^{12} cm^{-2}.

Fig.4 Calculated drain characteristics of a recessed-gate GaAs MESFET with high surface-state density of 10^{13} cm^{-2}.
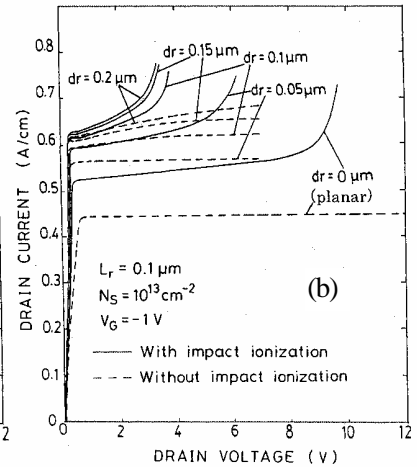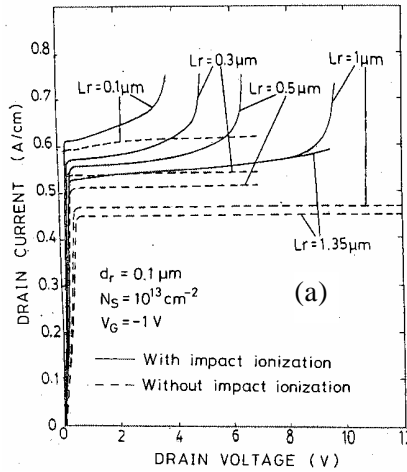

Fig.5 Calculated I_D-V_D curves for the case of surface-state densities of 10^{13} cm^{-2}, as parameters of L_r ((a)) and d_r ((b)).

BREAKDOWN CHARACTERISTICS

Figs.2, 3 and 4 show calculated drain characteristics of narrowly-recessed-gate GaAs MESFETs ($L_r = 0.1$ μm, $d_r = 0.1$ μm). Without surface states (Fig.2), drain currents increase steeply around 7 V, which is due to an increase in gate current itself due to generated holes. With relatively low surface-state densities of 10^{12} cm^{-2} or 2×10^{19} cm^{-3} (Fig.3), the characteristics show a slight kink around 3 V and a clear increase in drain currents (breakdown) beyond 10 V. This voltage is higher than that in Fig.2. The kink is attributed to a space-charge effect originated from (generated) hole capturing by

surface states ((5)). With high surface-state densities of 10^{13} cm^{-2} or 2×10^{20} cm^{-3} (Fig.4), a steep increase in drain currents occurs at as low as 3 ~ 4 V. We will discuss the last case further by describing the dependence of recess parameters (L_r, d_r).

Fig.5 shows calculated I_D-V_D curves of recessed-gate GaAs MESFETs (with surface-state densities of 10^{13} cm^{-2}) as parameters of distance between gate and recess edge L_r ((a)) and recess depth d_r ((b)). As L_r becomes longer, the breakdown voltage becomes higher, which can be naturally understood. On the other hand, we also see that as d_r becomes deeper, the breakdown voltage becomes lower than that for the planar structure ($d_r = 0$

μm), indicating that the breakdown voltage becomes low by introducing a recessed-gate stru cture.
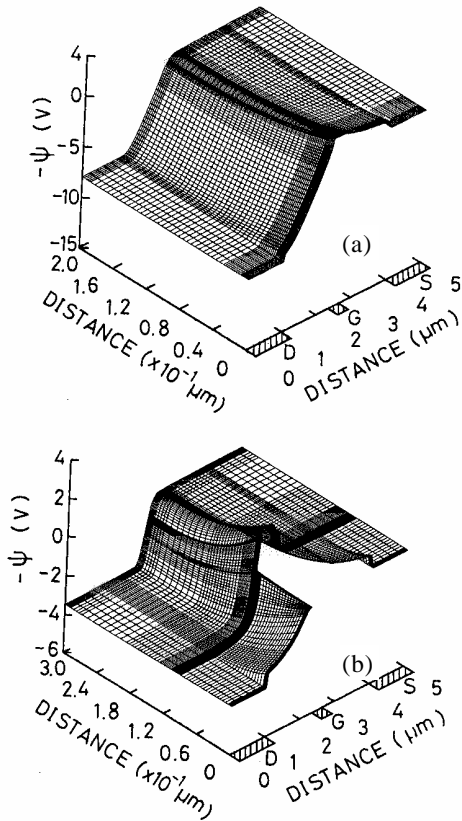

Fig.6 Comparison of potential profiles of GaAs MESFETs with surface-state densities of 10^{13} cm^{-2}. (a) planar structure ($V_D = 8$ V, $V_G = -1$ V), (b) recessed-gate structure with $L_r = 0.1$μm and $d_r = 0.1$μm ($V_D = 3.5$ V, $V_G = -1$ V).

Fig.6 shows a comparison of potential profiles between (a) planar structure and (b) narrowly-recessed-gate structure ($L_r = 0.1$ μm, $d_r = 0.1$ μm). In the planar structure, the drain voltage is almost uniformly applied between gate and drain (1.35 μm). But in the recessed-gate structure, the voltage drop between gate and recess edge (0.1 μm) is quite large, which is a cause of the lower breakdown voltage (3 ~ 4 V).

GATE-LAG PHENOMENA

Next, we describe the gate-lag phenomena. Fig.7 shows calculated turn-on characteristics of recessed-gate GaAs MESFETs (with surface-state densities of 10^{13} cm^{-2}) as parameters of L_r ((a)) and d_r ((b)). In general, the drain currents remain low values for some periods and begin to increase slowly, showing the gate-lag behavior. This is due to the slow response of surface states (Horio and Yamada (7)). As L_r becomes shorter or d_r becomes

deeper, the gate-lag is reduced, because the surface-state effects are reduced ((3)). A discussion why the gate-lag is smaller with impact ionization was presented at the
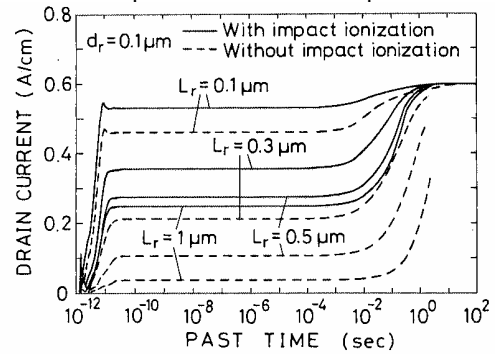
(a)
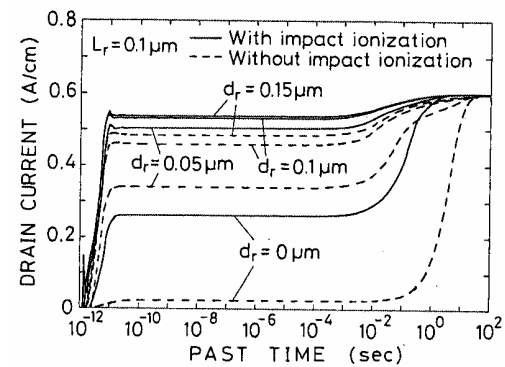
(b)

Fig.7 Calculated turn-on characteristics of recessed-gate GaAs MESFETs as parameters of (a) L_r and (b) d_r. Surface-state densities are 10^{13} cm^{-2}.
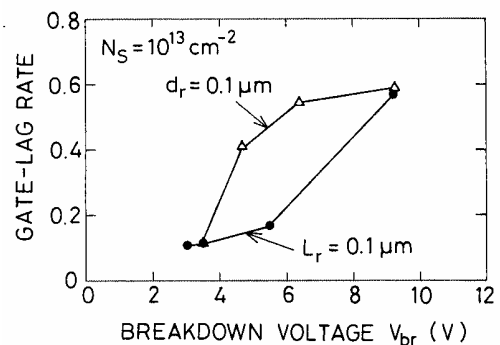

Fig.8 Relationship between gate-lag rate and breakdown voltage of recessed-gate GaAs MESFETs. Data are taken from Fig.5 and Fig.7.

previous conference (Horio et al (8)).

Fig.8 shows the gate-lag rate versus breakdown voltage for the recessed-gate GaAs MESFETs, which is obtained

from the data in Fig.5 and Fig.7. Here the lag rate is defined as

$$\text{Lag Rate} \equiv \frac{I_D(\text{ON}) - I_D(t = 10^{-6} \text{ s})}{I_D(\text{ON})} \quad (6)$$

where $I_D(\text{ON})$ is the drain current in the ON state, and $I_D(t = 10^{-6} \text{ s})$ is the drain current at 10^{-6} sec after the gate voltage is switched on. It is seen that there is a trade-off relationship between raising the breakdown voltage and reducing the gate-lag. This type of trade-off is also reported experimentally in PHEMTs (Huang et al (9)).

CONCLUSION

2-D simulation of breakdown characteristics in narrowly-recessed-gate GaAs MESFETs has been performed considering surface-state effects. It has been shown that the breakdown voltage could be raised when moderate densities of surface states are included. However, in the case with relatively high densities of surface states, the breakdown voltage could be drastically lowered when introducing the narrowly-recessed-gate structure. It is suggested that there may be a trade-off relationship between raising the breakdown voltage and reducing the gate-lag.

ACKNOWLEDGEMENT

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