PHYSICS OF FUTURE ULTRA HIGH SPEED TRANSISTORS – PART II: NEW CONCEPTS

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Abstract — SiGe/Si - MODFETs have obtained encouraging results with maximum oscillation frequencies for p- and n-channel devices around 100 GHz. The SiGe/Si system is the only one with nearly symmetrical transport properties of holes and electrons. Future development of silicon based ultra high frequency devices will be strongly influenced by integration demands, quality of MOS gates on heterostructures, strained layer engineering and band ordering. Devices which exploit tunnelling, coherent transport and transit time effects will gain importance. Room temperature tunnelling via SiGe quantum wells and quantum dots is proposed and partly tested. Resonance phase operation may allow oscillators with defined frequencies above the conventional frequency limits.

I. INTRODUCTION

With the shrinkage of device dimensions into the deep submicrometer regime quantum effects appear which manifest themselves as minor correction that may limit device reliability. But using quantum effects in a proper way can improve existing devices and create new device functionality. In widespread use in III/V opto- and microelectronics is the reduction of dimensionality of carrier movement by quantum wells, -wires, -dots. Quantum confinement influence mobility and density of state distribution of the carriers. Quantum confinement lasers and modulation doped field effect transistors (MODFET or HEMT, high electron mobility transistor) are the most prominent examples of these devices. Another important effect is tunnelling through barriers. A good overview about possible device structures is given by A. Zaslavsky [1]. The potential for high speed operation is nicely demonstrated by the submillimeter (700 GHz) operation of a resonant tunnelling diode oscillator [2]. Recently, research groups at IBM and Daimler-Chrysler [3] obtained excellent results with SiGe/Si MODFET devices. For both channel types maximum oscillation frequencies f_{max} around 100 GHz were reported (p-channel 85 GHz, n-channel 120 GHz). Now it gets more clear, that the development of ultrahighspeed silicon microelectronics will deviate in some important aspects from the III/V directions. The main reasons are the higher effective masses in silicon which make resonant tunnelling less favourable, the specific band ordering at silicon heterojunctions which require strained layer engineering, the favourable use of MOS gates, and the integration needs with conventional Si microelectronics. Strained layer engineering and integration aspects require a so called *virtual* substrate, which consists of a Si substrate with a surface layer with another lattice constant than Si. A straightforward solution would be a Si-substrate with a *relaxed* SiGe layer on top of it. Unfortunately, at the moment these virtual substrates suffer either from poor crystal quality or unacceptable thick overlayers (up to 10 µm [4]). But recently several attempts were made to improve the quality. One attempt [5] uses point defect injection to promote relaxation in a less than 100 nm thick overlayer.

II. HETERO-FIELDEFFECT TRANSISTORS

The classical MODFET has a Schottky type gate electrode. In the SiGe/Si system the p-channel is created by a thin SiGe layer, the n-channel is created by a thin, tensily strained Si layer [3]. That means a mandatory usage of *virtual* substrates for n-channel and complementary devices. The band ordering at the unstrained Si / compressive strained SiGe interface confines holes to the SiGe side and does not influence the movement of electrons across the interface. At the tensile strained Si / compressive strained SiGe interface the electrons are confined to the Si side, the holes to the SiGe side. This not very usual bandordering is called type II ordering and it requires the specific strain situation in SiGe/Si. The main question for the future development are: How can one use MOS gates and how can one combine n-channel and p-channel devices to a manufacturable complementary heterofieldeffect transistor (HFET)? The vertical structure [6] could simply consist of a virtual substrate, both channels (Ge, Si) and possibly a SiGe/Si cap (Fig. 1) for a buried n-channel.

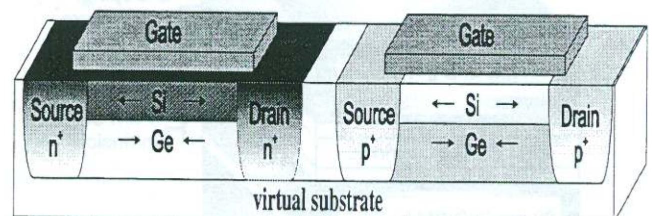

Figure 1: Scheme of a hetero-CMOS. The strain in the layers is indicated by arrows (Si tensile strain, Ge compressive strain). The n-MOS (left) has a electron channel in Si, the p-MOS (right) has a hole channel in Ge.

The channel is automatically selected by the choice of the source/drain doping, because the electrons jump in the Si channel and the holes in the Ge channel [7].

The challenges for material scientists and device engineers will be the high strain, the virtual substrate quality and the low process temperature budget. This unique strained Si/Ge will be the only known material combination with symmetrical, good carrier properties (both n, p mobilities are expected to be within 1500 - 3000 cm^2/Vs). All other complementary FET channels suffer from poor hole properties.

A completely different concept foresees shrinkage of the gate length below 70 nm by vertical MOSFETs. The otherwise problematic short channel effects will be suppressed by a SiGe heterobarrier [8]. High-speed with very short channel length will be obtained when parasitic capacitances can be reduced which is not an easy task with vertical MOSFET structures.

III. ROOM TEMEPRATURE TUNNELLING

Tunnelling junctions yield regions with negative differential resistance in the forward characteristics. Resonant tunnelling in SiGe/Si [9] exhibited weak negative characteristics at room temperature with rather low peak to valley current ratios (PVCR). Recent experiments [10] have revived the interest in interband (Esaki) tunnelling. With δ-doped structures with an thin intrinsic SiGe-layer (Fig. 2) high current densities (several kA/cm^2) and interesting negative resistance behaviour (Fig. 3) could be observed at room temperature [11]. We expect a further increase of the tunnelling efficiency with selfordered quantum dots arranged within the intrinsic region of a pin junction [12]. To our knowledge the substantial growth problems connected with doping of the selfordered array are not solved, yet. Selfordered growth of a quantum dot array may be accomplished by the so called Stranski-Krastanov growth mode in which a strained material (e.g. Ge on Si) create a very thin wetting layer (≈ 0.5 nm thick) on top of which islands with nanometer dimensions nucleate (for details, see [13]). Such improved tunnelling junctions could be used for fast current injection in three terminal transit time devices as shown schematically in Fig. 4. The Esaki-tunnelling is controlled by the voltage V_{EB}, the injection into the drift region is of the Zener type.

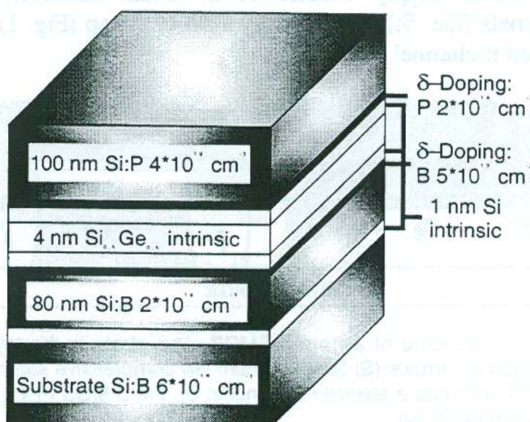

Figure 2. Structure of the SiGe-pin tunnel junction.

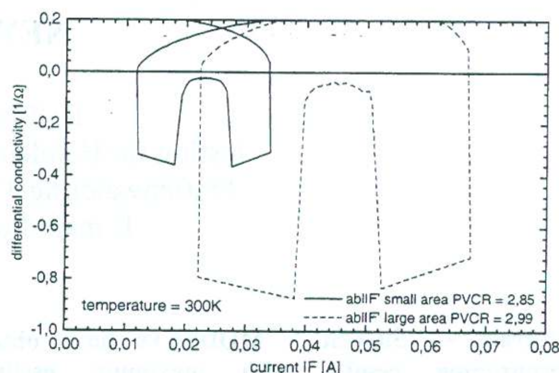

Figure 3: Differential conductivity as function of forward current I_F

IV. COHERENT TRANSISTORS

The most powerful solid-state oscillators in the mm-wave regime are made from two-terminal devices. Why are diodes faster than transistors? A simple fact is given by the lower parasitics of a two-terminal device, but also time delays during transport across a space charge layer are differently utilized. Whereas in a transistor the delay time is considered as a reduction of transit frequency, e.g. in an Impatt diode the delay is designed to generate a π-phase shift between current and voltage at the desired operation frequency. Therefore, considerations were given to exploit the transit time delay also in three terminal devices. A clear concept was proposed by S. Luryi [14] with a coherent transistor where the delay during diffusion through the base was considered. In a base of a BJT a carrier pulse entering from the emitter side broadens during its diffusive transport through the base. With step graded heterostructures the broadening can be reduced considerably. At a frequency ω the pulse at the collector side enters the drift region with a phase shift $\omega\tau_B$. Further phase shift adds during drift through the collector space charge region. According to H. Jorke [15] a gain above the standard frequency will be available if the structures are optimized for coherent transport (Fig. 5). The operation with phase delays around π is called resonance phase operation [15].

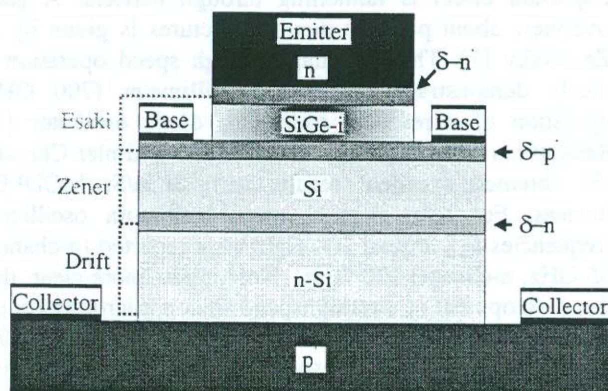

Figure 4: Three terminal transit time device tunnelling injection into the drift region

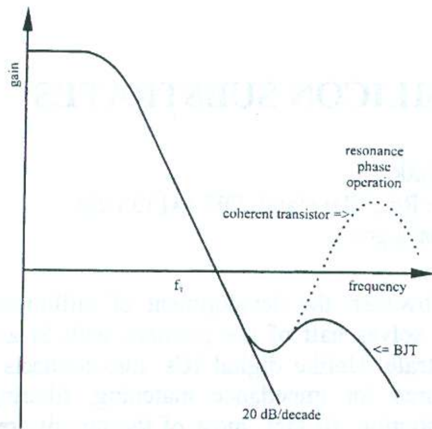

Figure 5: Gain as function of frequency. Compared is a BJT with a coherent transistor.

V. CONCLUSIONS

The SiGe-HBT has started as first silicon based heterojunction transistor which came into volume production. Specific low breakdown voltage transistors will soon reach the f_T = 200 GHz limit.

Both, n- and p-channel MODFETs are now around f_{max} = 100 GHz. The material system Ge/Si is the only one which offers *symmetrical* transport properties for complementary n- and p-channel devices.

For future importance of complementary HFET devices the application of MOS gates and manufacturing issues will be crucial. An inherent advantage of strained Si/Ge is the transport of holes in Ge and that of electrons in Si.

In the past Si based heterostructure devices followed closely the development in the III/V area. The high priority of integration aspects, the excellent quality of MOS gates, the high effective mass and the specific band ordering at heterointerfaces will force the development of Si based heterodevices into different directions. We see interband tunnelling (Esaki) via quantumwells and –dots, coherent transport and exploitation of transit time effects as essential ingredients of future ultra high-speed silicon devices.

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