Investigation of He^+-ion bombardment in the fabrication of planar InP/ InGaAs HBT structure

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ABSTRACT

We have investigated He^+-ion bombardment on lattice-matched multi-layer InP/ $In_{0.53}Ga_{0.47}As$ and $In_{0.5}Ga_{0.5}P$/ GaAs heterojunction bipolar transistor (HBT) structures. The bombardment of these structures was tested with a single energy implantation of helium-ions at 600 keV with a dose of $3x10^{15}$ cm^{-2} at room temperature. Post implant annealing was performed for 60s from 50 to 575°C. Maximum achievable sheet resistance of $3x10^7$ W/sq was recorded for the GaAs-based base and collector layers of the InGaP/ GaAs HBT structure and $8x10^4$ W/sq for the InGaAs-based collector layer of the InP/ InGaAs HBT structure. Comparison of annealing characteristics of bombarded GaAs- and InP- based HBT structures as a function of annealing temperature are reported here.

I. INTRODUCTION

InP-based devices have made remarkable progress in recent years in the field of optoelectronics, microwave and milimeter-wave electronics. Despite the presence of a more widely used and more mature GaAs-based technology, devices such as InP/ InGaAs HBT which offer material compatibility with long wavelength photonic devices such as photodetectors and lasers operating in the wavelength range of 1.3 to 1.55 µm, is becoming an important technology for telecommunications and signal processing. There are a number of inherent advantages of these devices, such as lower turn-on voltages (0.2 V) as compared to GaAs-based HBTs (0.8 V) [1] and higher speed, demonstrating the application of low power circuits.

The fabrication of these devices usually employ wet chemical etching to contact each transistor layer and for device electrical isolation. Unfortunately, there are various problems associated with mesa etching in the manufacturing of InP/ InGaAs HBT, including problems with step coverage. However, ion bombardment is an alternative route to mesa fabrication, allowing a planar self-aligned device to be fabricated.

Ion bombardment is widely used in III-V device technology, mainly for creating highly resistive regions for device isolation. They serve similar purposes as mesa etching. Device isolation by bombardment is used to restrict current flow to active regions of a device, in this case a transistor, without having to cross-talk with other devices in the same wafer. Ion-bombardment also provides sufficient insulating surface for construction of passive elements such as capacitors and transmission lines, which are required for monolithic circuits. One of the main advantages of applying this technique is the elimination of problems associated with mesa etching, such as metal and material step coverage.

Due to the narrow-bandgap of InGaAs, there is currently no effective bombardment technique available to electrically isolate the material and therefore mesa etching remains the only available technique. This step in the fabrication of HBTs is not a straightforward step since the height of the transistor is about 1.5 µm, making the step coverage very difficult. Moreover, from the reliability point of view, there are more advantages in fabricating transistors with planar geometrical structures.

II. METHOD

N-p-n single HBT based in InP/ InGaAs and InGaP/ GaAs structures were grown by metal-organic chemical vapour deposition (MOCVD). Figures 1 and 2 show a schematic device layer structure used for sheet resistance measurements of various layers of the HBT structures. TLM patterns were fabricated prior to implantation on the HBT structures using HBT metallisation on the following regions, for InP/ InGaAs HBT: emitter capping (n^+-InGaAs), base (p^+-InGaAs) and collector (n^+-InGaAs) layers; and for InGaP/ GaAs HBT: emitter capping (n^+-InGaAs), base (p^+-GaAs) and collector (n^+-GaAs) layers.

Ni/AuGe/Ni/Au metal system was used for the emitter cap and collector layers while Au/Zn/Au was used for the base layers, in both the HBT structures. The TLM technique is very convenient method to determine the bombarded sheet resistance since the same TLM patterns are usually fabricated on the wafer together with the transistor, avoiding extra patterns for electrical isolation test. TLM measurements were obtained using the four-point probe method from an automated controlled system. The test structures were bombarded at room temperature with $^4He^+$ at 600 keV to the optimum dose of $3x10^{15}$ cm^{-2} to achieve the highest resistivity with an ion current density <0.5 $\mu A/cm^2$ using a 2MV High Voltage Implanter. The experiment was performed with the sample surface tilted by 7° with respect to the beam incidence direction to minimize ion channelling. Post implant annealing was performed at temperatures between 50 and 575°C for 60 seconds by rapid thermal annealing (RTA) in flowing nitrogen ambient, with samples placed below respective substrates in order to prevent diffusion occurring at higher temperatures.

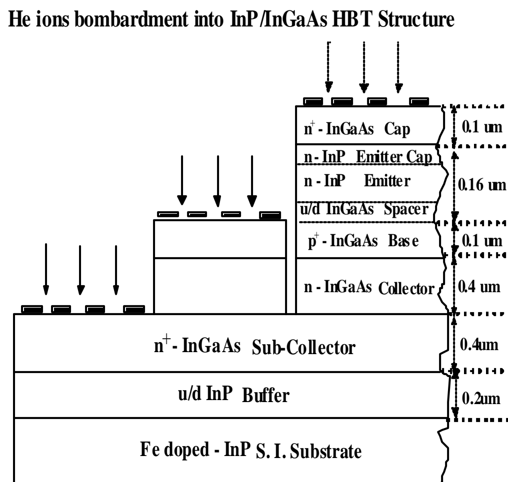

Fig.1: TLM patterns fabricated on various layers of the InP/InGaAs HBT structure.

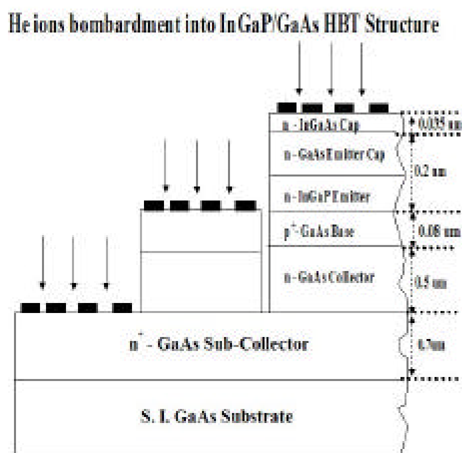

Fig.2: TLM patterns fabricated on various layers of the InGaP/GaAs HBT structure.

III. RESULTS

Damage vacancy concentration profile of various ions (H^+, He^+, O^+, Fe^+) bombarded into InP/ InGaAs HBT layer structure, determined by Transport of Ions in Matter (TRIM) simulations [2] is shown in figure 3.

The end of range of 600 keV He^+-ions is about 2.1 µm, intentionally placed away from the device epitaxial layer, to provide a uniform defect concentration in the active device layer. We have also included profiles of 250 keV H^+-ions, 2.5 MeV O^+-ions, and 4.5 MeV Fe^+-ions providing similar projected range. The peak damage in all ions is intentionally placed away from the active layers to avoid complication due to complex defects.

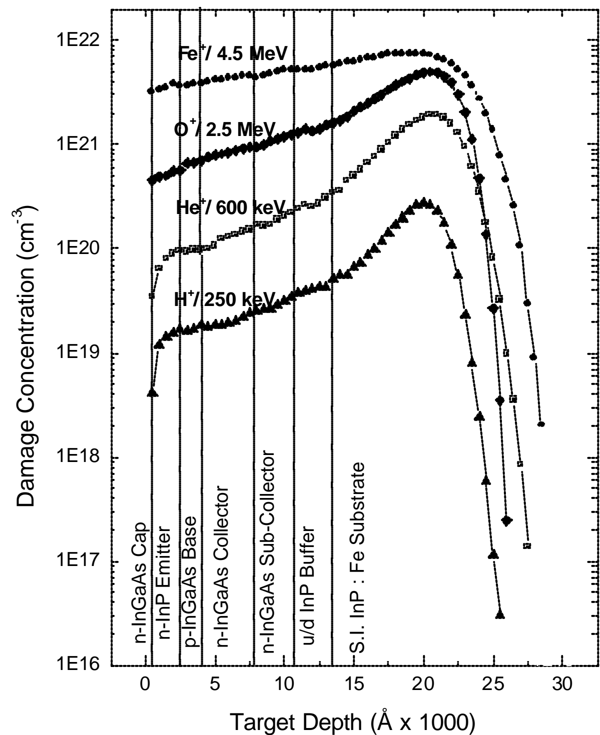

Fig.3: Damage distribution for bombardment of H^+/ He^+/ O^+/ Fe^+ ions in InP/ InGaAs HBT structure simulated by TRIM [2].

He^+-ions are preferred when compared with H^+-ions for two reasons: He^+-ion produces greater damage and secondly they avoid the undesirable hydrogen passivation of carbon atoms forming in the p-type base of the transistor [3]. Further observation from figure 3 is that Fe^+-ion bombardment shows a more uniform damage distribution through the structure, when compared with the other ion species, indicating to be a good candidate to electrically isolate both the narrow- and wide- bandgap materials. However, due to complex deep level traps created by Fe^+, higher

annealing temperature (up to 800°C) is required and this may not be feasible for HBT structure due to problems associated with Fe^+ in-diffusion and crystal lattice imperfection.

The variation of bombarded sheet resistance, R_{sh} for the whole InP/ InGaAs and InGaP/ GaAs HBT layers; emitter capping, base and collector layers is illustrated in figure 4. Both the as-bombarded samples show similar increase in R_{sh} when compared with their initial R_{sh} before bombardment (see table 1). This indicates that the bombarded samples show similar characteristics to those of before annealing showing damage created to be independent of the material properties. Increase in R_{sh} is due to the removal of carriers by deep level traps created by the bombardment. Observations show that below 200°C, the as-bombarded R_{sh} for both samples remain constant, indicating that the activation of deep level traps created by He^+-ions require anneals at temperatures > 200°C. After 200°C, R_{sh} increases with increasing annealing temperature as a result of reduction in electron hopping conduction. Optimum annealing temperature, where the R_{sh} reaches the peak value, for InP/ InGaAs HBT is 350°C, whereas for the InGaP/ GaAs HBT is about 550°C. Any further increase in annealing temperature leads to annihilation of deep level traps and should ultimately reach the initial value of R_{sh}.

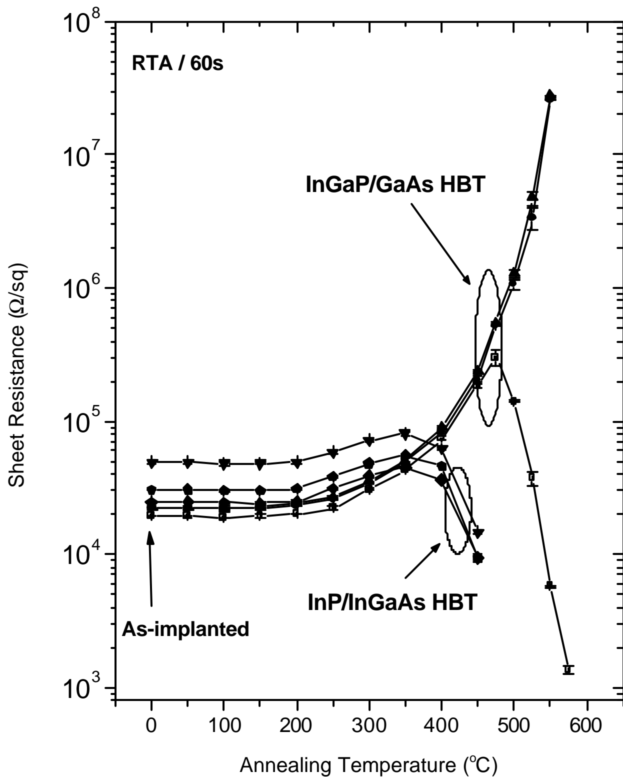

Fig.4: Graph of sheet resistance as a function of annealing temperature on InP and GaAs HBTs bombarded at 600 keV/ He^+/ $3x10^{15}$ cm^{-2}/ RT.

GaAs-based materials may require a much higher optimum annealing temperature to achieve maximum R_{sh} due to their bandgap properties. A wide-bandgap GaAs material may contain more deep level traps compared to the narrow-bandgap InGaAs material, requiring higher temperature to sufficiently remove carrier traps, preventing hoping conduction and achieving maximum R_{sh}. It is interesting to point out that the maximum R_{sh} for all the layers in the InP/ InGaAs HBT occurs at the same annealing temperature of 350°C.

It is also interesting to note that unlike the annealing characteristics observed for the InP/ InGaAs HBT, the results show very similar R_{sh} for both the n- and p- type GaAs materials (i.e. base and collector layers) through out the annealing process. The GaAs-based HBT was not further annealed after 550°C due to degradation of ohmic contact leading to poor or unstable measurements. Based on previous studies [3], the optimum annealing temperature for the InGaP/ GaAs HBT is about 550°C.

Figure 5 shows a simple comparison of post-anneal R_{sh} as a function of annealing temperature for the cap layers of both HBTs, and a single layer GaAs (collector layer).

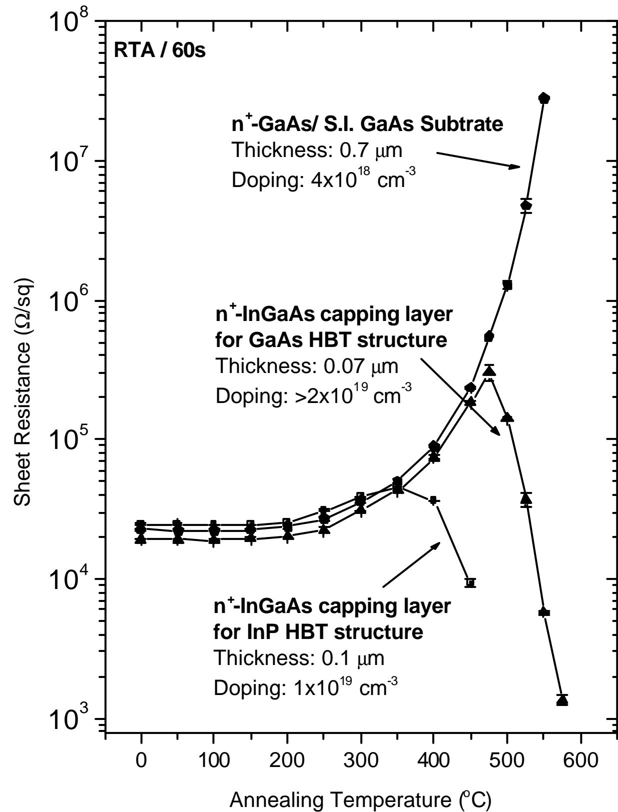

Fig.5: Comparison of post-annealed R_{sh} for the cap layers of both HBT structures and the collector layer of the InGaP/ GaAs HBT.

Table 1: R_{sh} analysis of InP/ InGaAs and InGaP/ GaAs HBT structure

Materials	Conductive Type/ Doping (cm^{-3})	$R_{sh\ (initial)}$ (W/sq)	$R_{sh\ (as\text{-}implanted)}$ (W/sq) ($1x10^4$)	$R_{sh\ (max)}$ (W/sq)	Optimum annealing temp. (^oC) @ 60s
InGaAs Cap layer for GaAs HBT	n^+ / >$2x10^{19}$	25	1.9	3.0 $x10^7$	475
GaAs Base	p^+ / $4x10^{19}$	340	2.2	2.6 $x10^7$	550
GaAs Collector	n^+ / $4x10^{18}$	3	2.3	2.8 $x10^7$	550
InGaAs cap layer for InP HBT	n^+ / $6x10^{19}$	27	2.5	$4.5x10^4$	350
InGaAs Base	p^+ / $5x10^{19}$	604	3.0	$5.6x10^4$	350
InGaAs Collector	n^+ / $2x10^{19}$	5	4.9	$8.1x10^4$	350

From figure 5, it was determined that maximum R_{sh} achievable for the narrow-bandgap InGaAs material is lower than the material grown on the GaAs-based HBT, having different optimum annealing temperature, at 350°C and 475°C, respectively. We believe that a much higher maximum R_{sh} for the emitter layer of the GaAs-based HBT (n^+-InGaP) can be achieved. The maximum value has not been reached in this test due to the limiting factors introduced by the narrow-bandgap InGaAs cap layer. If the bombardment was conducted without the cap layer, it would have been possible to achieve the expected R_{sh}. Observations also show that a slightly higher maximum R_{sh} for the InGaAs material grown on the GaAs-based HBT compared to the InP-based HBT. This may suggest that the presence of a wide-bandgap GaAs material from the InGaP/ GaAs HBT structure influencing the bombarded region, as compared to the narrow-bandgap of InGaAs material from the InP/ InGaAs HBT structure.

IV. CONCLUSION

In this paper, we have shown detailed analysis of annealing characteristics of He^+-ion bombardment into InP/ InGaAs and InGaP/ GaAs HBT structures. Maximum R_{sh} of $8x10^4$ and $3x10^7$ Ω/sq was achieved for n^+- InGaAs and GaAs materials, respectively. Results suggest that the narrow-bandgap cap layer introduced for GaAs HBT can reduce the overall bombarded R_{sh} of the structure.

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