MEMS-IC integration for RF and millimeterwave applications

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Abstract — **This paper reports on the MEMS-IC integration for microwave and millimeterwave applications. The integration is based on the System In Package (SiP) approach achieving high performances and integration density level at microwave and millimeterwave frequencies thanks to the mixing of state-of–the-art technologies both for active (SiGe or RF-MOS technologies) and passive (dielectric based technology) devices/circuits. This concept can also take full benefit of the MEMS technologies to provide various smart functionalities to microsystem. The proposed approach is illustrated through different applications which outline the design issues of such heterogeneous microsystem.**

I. INTRODUCTION

Microsystem integration is one of the most crucial challenges for future microwave and millimeterwave applications. The objectives are to achieve high degree of integration with more and more functionalities (reconfigurable and tunable behaviour, self testing, …) while achieving high performances, small size and weight, low power consumption and better cost.

The single chip transceiver (System On Chip –SoC– approach) seems to meet all the requirements but suffer, at microwave and millimeterwave frequencies, from the low quality factor of some passive devices especially inductors.

System in Package (SiP) solution in which multi-chip are assembled on a substrate can then be a powerful (in term of performances) alternative to SoC [1], [2]. In this approach the substrate integrate all the critical passive devices –critical for global performances– and then must be chosen as low-losses as possible. The substrate can also provide the package of the whole microsystem (thus the name of the approach).

This paper presents the mixed technologies uses toward the SiP integration for microwave and millimeterwave applications. Then we present the design issues of such microsystem through several realized applications- which take benefit of the followed approach.

II SYSTEM IN PACKAGE TECHNOLOGY

SiP microsystem performances are highly related to the integrated technologies ones. Moreover, the design step needs to consider all the potentialities and limitations of the various technologies in order to define suitable system architecture and its optimal partitioning. This paragraph presents considered the state-of–the-art technologies both for active (SiGe or RF-MOS technologies) and passive (dielectric based technology) devices/circuits which will be integrated into the whole microsystem.

SiGe technology

During the fifteen past years, SiGe HBT technology has been developed and improved with respect to the frequency performances, the noise, the linearity, the reliability and power consumption [3]. Nowadays, the state of the art of f_T value for SiGe HBT transistors is 350 GHz with an associated f_{MAX} value of 170GHz [4]. Except this heroes result, the state of the art reports active devices operating up to 200 GHz both for digital (evaluated by f_T) and analog (evaluated by f_{MAX}) circuits. Figure 1 shows the evolution of the silicon-germanium technologies with respect to the two main indicators: the transition frequency (f_T) and the maximal oscillation frequency (f_{MAX}). The results indicate that the trend is to improve both f_T and f_{MAX} in order to be able to cover with a similar technology a microsystem that will feature advanced analog and digital circuits.

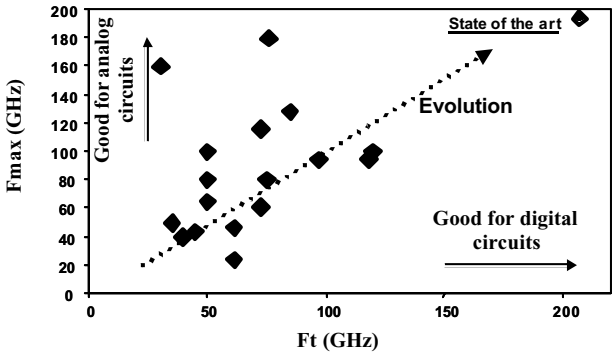

Figure 1 : Evolution of frequency performances of SiGe technologies

Passive devices and SiP technology

Beside the attractive capabilities of the active devices, we have to consider the performances of on-chip passive ones. In the past, it was claimed that silicon substrate will

not be able to afford passive elements featuring high quality factor and high self resonant frequency. The situation is not so clear at microwave and millimeterwave frequencies.

About integrated capacitors, figure 2 presents the self resonance frequency of MIM capacitors available into a SiGe BiCMOS technology versus the capacitor values. We have plotted a forbidden zone where the capacitances will not be useable (in grey in the figure). Note that a capacitor of 1.3pF features a resonance frequency larger than 30 GHz, so it can be used for circuit design.

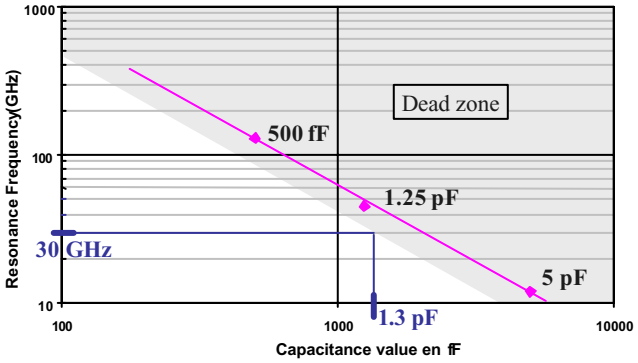

Figure 2 : Self resonance frequency evolution versus capacitor values

Concerning the inductors, the situation is more complex as inductors exhibit poor quality factor and low self resonant frequencies without specific precautions. Nevertheless, it is possible to optimize both the inductor value and the quality factor through specific design [5], [6]. For instance, a simple way to overcome losses in inductors [7] is to stop the field lines penetration into the silicon substrate by adding a thin conductive layer underneath the substrate. Figure 3 shows two inductors featuring a value of 0.75 nH realized through two different ways. We can observe that adding Nepi layer gives a great improvement of the quality factor in the millimeterwave range. Furthermore, an impressive self resonance frequency of 64 GHz has been measured.

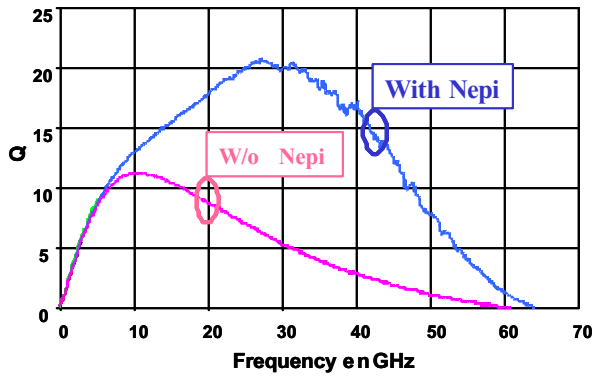

Figure 3 : *Measurements of the quality factor versus frequency for integrated inductors*

Despite all the researches to improve the inductor quality factor, they still remain too low (10 to 20) for plenty of applications. One solution to ensure high performances to circuits and systems is then to realize passive devices and circuits (inductors, capacitors, resistors, RF-MEMS switches or variable capacitors, lines, hybrids, …) on a low loss technology and to flip-chip the active circuits to realize the desired microsystem as illustrated in Figure 4.

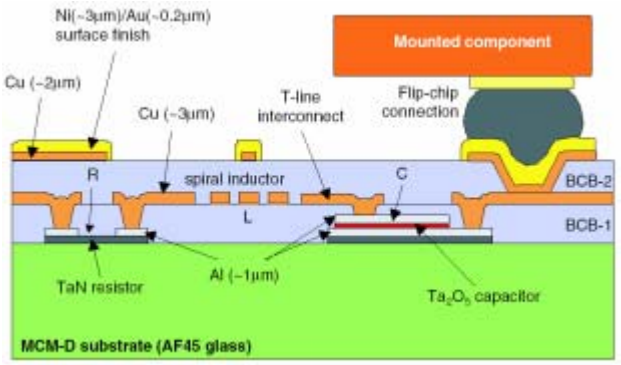

Figure 4: MCM technology for SiP integration of microwave microsystems

Thanks to this technology, some high performances circuits have already been published like a Quadrature Couplers design from 10 to 15 GHz which exhibits losses of only 0.2 dB at 15 GHz [8].

III. Design Methodology : Co-Design Approach

This part outlines the design issues of SiP microsystem. The design methodology can -and then must- go beyond the simple way which consists in designing the blocks individually and then connect them all together. We indeed have to define:

- the considered technologies both for active and passive part of the microsystem,
- the system architecture considering the selected technologies (for chips and integration),
- the efficient partitioning between the technologies,
- the characteristics of the frontiers connections (characteristic impedance, capacitive or inductive behavior, length…) between chips.

All the design issues will be outlined through different applications operating at microwave and millimeterwave frequency range.

Mixed technologies: VCO

The first application deals with a Voltage Controlled Oscillator whose resonator is integrated in the low losses substrate (see Figure 5) as the active circuit is realized with a SiGe technology. It is indeed well known that the phase noise depends on:

1. the low frequency noise of the active devices used,
2. the quality factor of the passive components.

To minimize the phase noise of VCO, or to keep it constant and to decrease the power consumption, we take benefit of the SiP concept by mixing two optimum technologies:

1. the SiGe technology ensures a low level of low-frequency noise of the active circuit,
2. the MCM-D technology (Figure 4) provides high quality passive components.

The Figure 5 presents the resulting SiP VCO : the SiGe chip is mounted using flip-chip process on the MCM-D substrate which integrate the high quality factor inductors. This application then demonstrates the powerful of mixing technologies through the SiP concept as one technology can not solve alone the two design issues (low noise of actives and high quality factor of passives) simultaneously and the combination of two efficient technologies translates into a real improvement of the circuit performances.

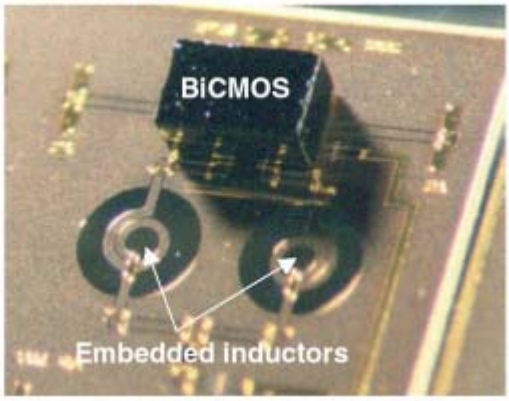

Figure 5 : Microphotography of the SiP VCO

As experimental results, keeping the output power constant, the phase noise performances are improved by 6dB and the power consumption is divided by a factor two.

A crucial design issue corresponds to flip-chip connections used for the assembly of the active chips on the passive substrate. These connections have to be:

- optimized to ensures high level of performances of the passive devices including their connections (the benefit of the passives can not be inhibited by the performances of the interconnections)
- modeled precisely to be taken into account during the design step.

System partitioning: Integrated image rejection mixer

The design of complex microsystem can not consist in connecting several blocks designed independently but must consider all the benefits of the heterogeneous technologies (SiGe or CMOS actives and MCM or silicon based passive technologies) before and during the design step. One crucial point is the definition of the architecture and partitioning of the functions which must consider all the involved technologies. For example, some passive functions can be integrated with the active technologies as there is no benefit to integrate them on the low-losses substrate.

An illustration of suitable partitioning can be proposed through the realization of an integrated image rejection mixer operating at 20 GHz which involves (see Figure 6):

- a RF quadrature coupler at 20GHz
- a IF quadrature coupler at 1GHz
- two LO 180° power dividers at 19GHz
- two IF 180° power combiners at 1GHz
- two (double balance) mixers
- a VCO at 19 GHz

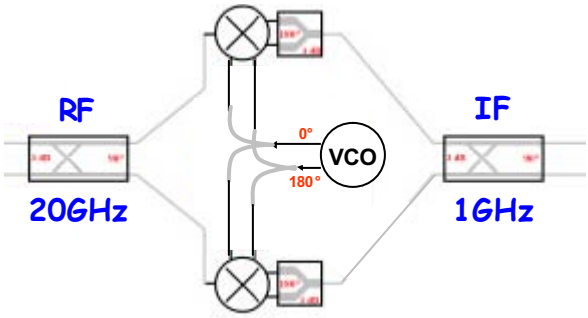

Figure 6 : Image rejection mixer

Considering the selected technologies (SiGe and MCM-D), a global design reports that the SiGe technologies can integrate all the passive functions operating at 1GHz and there is no benefit to integrate them using the MCM-D substrate.

An other degree of freedom which can be used to optimize the global performances can be the reference (characteristic) impedance of the passive functions (and then the connecting lines between subsystem blocks) which could be optimized and different from 50 Ω.

An other advantage of the SiP approach compared to the SoC one concerns the yield of the whole microsystem as all the building blocks can be tested and selected separately before the integration.

Smart microsystem : Redundant front-end receiver

Finally, the RF-MEMS technologies can also be integrated with active circuits in order to have tunable and/or reconfigurable behavior. The Figure 7 presents a silicon integrated microsystem for millimeterwave space communications, which is a redundant low noise front-end using MEMS technologies. The redundant character is ensured by a MEMS-based *Single Pole Double Throw* (SPDT) which addresses the RF signal in the selected amplifier path constituted by filters and LNA. The LNAs are then flip-chiped on the MEMS-circuits substrate.

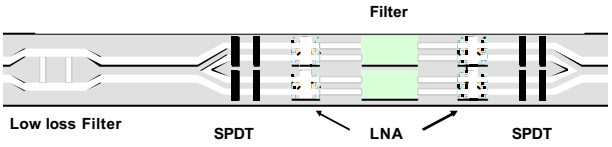

Figure 7 : MEMS based redundancy front-end for secured millimeterwave communications

The Figure 8 presents the MEMS-based SPDT which exhibits impressive performances: only 0.6 dB insertion loss and 21dB isolation were measured at 30GHz [9]. These results represent a real improvement compared to the active devices based (1dB less for the insertion losses compare with the FET based SPDT at the same frequency) even if we add the loss of the flip-chip mounting bumps and then justify the hybrid integration of MEMS and ICs.

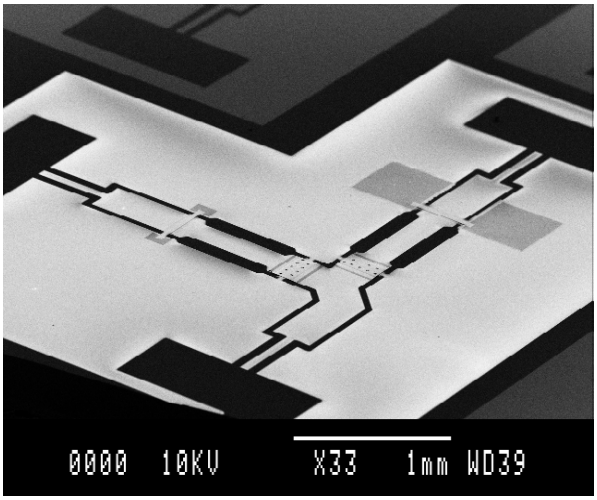

Figure 8 : Microphotography of the MEMS-based SPDT

Moreover, the MEMS technologies can also solve testing issues of complex microsystem as we can use MEMS switches to design self testable microsystem. The SPDT could be the heart of such concept and we then have to define a design strategy to ensure efficient self testing procedure.

IV. CONCLUSION

This paper reports on the System In Package (SiP) integration approach for microwave and millimeterwave applications. This approach ensures high level of performances as it mixes different state-of–the-art technologies both for active (SiGe or RF-MOS technologies) and passive (dielectric based technology) devices/circuits. The integration technology needs to be associated to a design methodology to take full benefit of the various technologies and to define efficient system architecture and partitioning. Moreover, the heterogonous integration approach allows the massive use of MEMS technologies which leads to the design of high performances and high functionalities (reconfigurable, self testable behavior) microsystem operating at microwave and millimeterwave frequency range.

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