High frequency low noise potentialities of down to 65nm technology nodes MOSFETs

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***Abstract* — 65nm n-MOSFETs show state-of-the-art cut-off frequency with f_t =210 GHz and microwave low noise and high gain properties(NF_{min}= 0.8dB and G_{ass}=17.3 dB at 12 GHz). As compared with the previous nodes, the high frequency properties of these MOSFETs continue to be in agreement with the downscaling trends.**

I. Introduction

The most important market of CMOS technology is driven by digital circuits and high-speed processors. By the downscaling process, the increasing performance of CMOS in term of f_t, f_{max} and high frequency noise enlarge the domain of applications of this technology and particularly for the realization of low noise, low consumption RF circuits and systems. Since the last 5 years, the objectives, was essentially oriented to the few GHz frequency range for mobile applications. Recent works [1], [2] show the potentialities of CMOS-based LNA in the millimeter wave range using 90nm SOI CMOS technology. Even if the performances of such mm-wave CMOS circuits are lower than III-V MMICs, the situation can change in the near future, by using high resistivity substrate (>1kOhm-cm), to obtain high quality passives, and by the improvement of HF characteristics of the next technology nodes (65 and 45 nm). In section II, the experimental DC, AC and HF noise characteristics of 65 nm bulk-CMOS devices, processed by ST Microelectronics, will be presented. In section III, these characteristics will be compared and discussed with the previous bulk and SOI CMOS technology nodes. Finally, one potential scenario concerning the mm-wave low noise potentialities of the 45nm node in V and W-bands will be discussed.

II. DC, AC AND HF NOISE CHARACTERISTICS OF 65nm BULK-CMOS

A. DC Characteristics

Fig. 1 depicts the main DC characteristics of a bulk n-MOSFET. This device involves 50 gate fingers of 2µm each (total gate width of 100µm) while L_{poly} is of 55nm. The maximum DC transconductance is of 1.1 S/mm at Vds=0.8V and is close to 1.2 S/mm at Vds=1.2V while the maximum drain current density is close to 750 mA/mm. It should be noted that such DC characteristics are comparable with commercially available 100nm P-HEMT technologies. Moreover, this device presents a high transconductance close to 700mS/mm at very low current density (50mA/mm) predicting HF low noise behaviors.

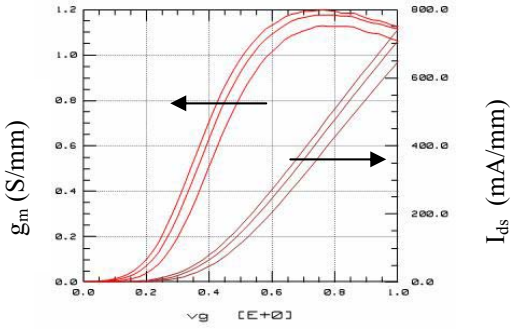


Fig.1. Experimental DC normalized drain current and transconductance versus V_{gs} for V_{ds}=0.8, 1 & 1.2V. n-MOSFET 50x2x0.055 µm².

In this technology, it is proposed two kinds of V_{th}, low V_{th} devices (against higher off-state leakage current) well suited for HF performances and higher V_{th} devices (with lower off-state current) for high speed digital applications. In this work, we focus our studies on low V_{th} devices. This technology is not too aggressive in term of gate oxide thickness allowing a good trade-off between channel control efficiency with high on-state drain current and reasonable gate leakage current. As shown in Fig.2, such devices present no critical gate current, for high frequency low noise amplifier applications, lower than 10 A/cm².

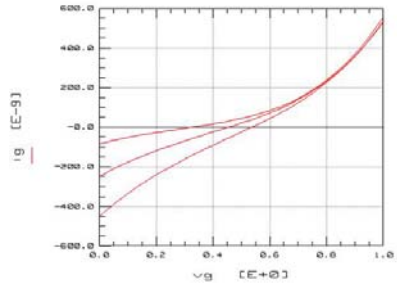


Fig.2. Experimental DC leakage gate current versus V_{gs} for V_{ds}=0.8, 1 & 1.2V. n-MOSFET 50x2x0.055 µm².

B. AC Characteristics

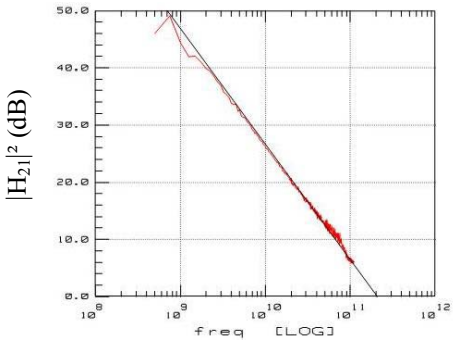


Fig.3. $|H_{21}|^2$ versus frequency; V_{ds}= 1V; I_{ds}=400 mA/mm; n-MOSFET 50x2x0.055 µm².

On-wafer S-parameters measurement was performed up to 110 GHz using 1mm coaxial probes (Ni contacts) and ®Agilent XF8510 VNA. The S-parameters plans correspond to the active part of the device and defined using a two-steps calibration procedure. First, a off-wafer LRM calibration procedure defines the reference planes at the probe tips and secondly the CPW accesses, embedding the device are deduced using a dedicated on-wafer open test structure. The efficiency and quality of this calibration and de-embedded procedures are shown in Fig.3 where the short-ended current gain depicts a perfect slope of -20dB/dec up to 110 GHz. The maximum values of f_t, f_{max} are respectively of 210GHz and 160 GHz. The small signal equivalent circuit are deduced from measured S-parameters (0.5-50 GHz) versus different bias conditions. As shown in Fig. 4, the intrinsic transconductance is higher than 1.4 S/mm with g_m over g_d ratio higher than 6.7 (close to 9 at low noise bias conditions) that denotes a moderate influence of short channel effects. Fig. 5 shows the total gate to source capacitance C_{gin} and total gate to drain capacitance C_{Miller}, directly extracted from the Y-parameters. These capacitances result both from intrinsic charge control capacitances and electrostatic fringing capacitances due to the overlap and spacer regions and inter-electrodes capacitances. C_{Miller} does not really depend of the bias conditions. Its value, close to 0.3pF/mm, contributes strongly to the degradation of the C_{gin} over C_{Miller} ratio (only 1.5 in low noise bias condition) limiting f_{max} and the minimum noise figure [13]-[14].

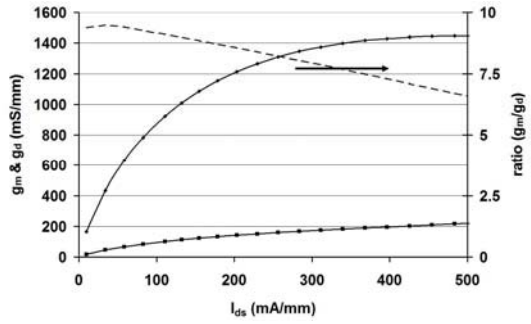


Fig.4. Intrinsic AC g_m (diamond), g_d (square) and its ratio (dashed line) versus the drain current density. V_{ds}= 1V; n-MOSFET 50x2x0.055 µm².

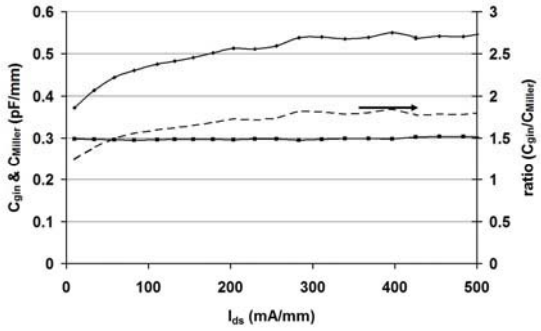


Fig.5. Intrinsic C_{gin} (diamond), C_{Miller} (square) and its ratio (dashed line) versus the drain current density. V_{ds}= 1V; n-MOSFET 50x2x0.055 µm².

C. High Frequency Noise Characteristics

Noise figure measurements are carried out in the 6 to 20 GHz frequency range. The commonly used noise parameters NF_{min}, R_n and Γ_{opt} are extracted from these measurements using the F50 method. These device presents very low noise and high gain properties with NF_{min}= 0.8dB and G_{ass}=17.3 dB at 12 GHz (Fig.6).

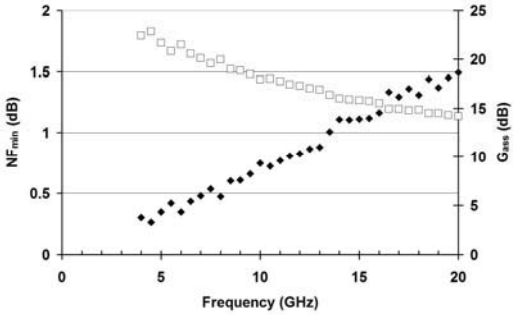


Fig.6. NF_{min} and G_{ass} versus the frequency; V_{ds}= 1V; Ids=110 mA/mm; n-MOSFET 50x2x0.055 µm².

III. COMPARISON AND DISCUSSION

As shown in Fig. 7, f_t is at the state-of-the-art for this technology node. The lower value of f_{max} with respect to f_t is mainly due to the gate resistance and fringing capacitances. Optimized gate topology device, not available in the PCM, with gate finger width close to 1µm should present f_{max} close to f_t.

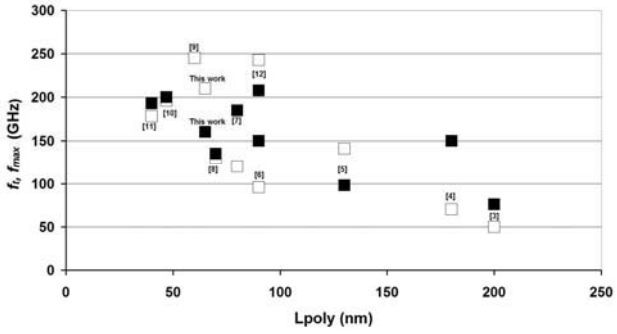


Fig.7. State-of-the-art f_t (black squares) and f_{max} (white squares) for bulk and SOI n-MOSFETs (ref. [3]-[12]).

These studied devices present also ultra low noise characteristics as shown in Fig. 8 with a NF_{min} less than

0.4dB (G_{ass} higher than 22dB) at 6GHz. This result is one of the best published.

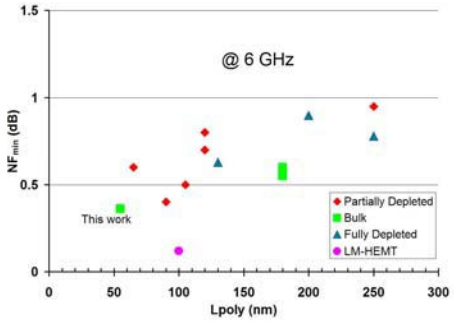


Fig.8. State-of-the-art of *NFmin* at 6GHz for bulk and SOI n-MOSFETs.

B. Discussion of the effect of the downscaling process on the HF noise properties.

The objective of this paragraph is to verify the noise properties along the downscaling process, described in [13] by adding this new technology node. The experimental verifications of the down scaling dependence of the noise sources and electrical parameters (g_m, c_{gsi}…) of different technology nodes MOSFETs are not easy. Indeed, we do not known accurately the actual channel length of the studied MOSFETs. Moreover, we have to compare these different MOSFETs in the same relative intrinsic bias conditions. To overcome these difficulties, we have chosen two criteria of comparison.

- For the five considered MOSFETs, we have compared the noise sources, g_m, C_{gsi} at the same

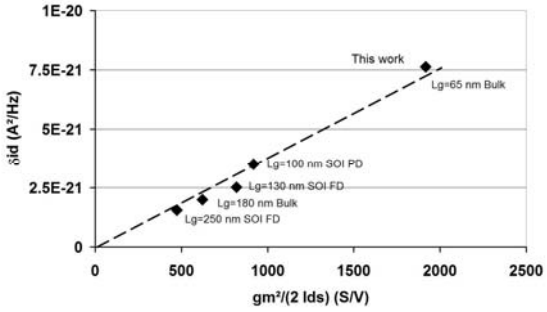
$$\frac{2I_{ds}(A/m)}{g_m(S/m)} \approx (V_{gs} - V_{th}) \quad (1)$$

For the following results, this criterion is applied in low noise bias conditions.

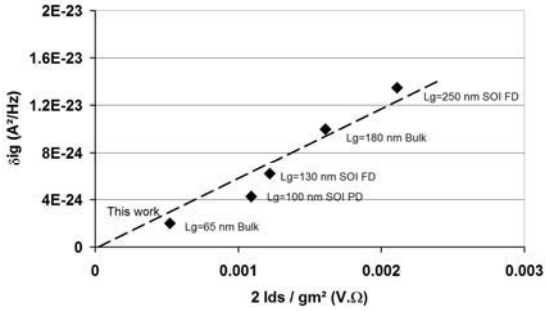
- We consider, as scaling parameter, the ratio

$$\frac{g_m{}^2(S/m)^2}{2I_{ds}(A/m)} \approx \frac{\mu\varepsilon}{t_{ox}L_{ch}} \quad (2)$$

I_{ds} is normalized DC drain current while g_m is deduced from AC measurements (broadband S-Parameters).
These criteria are chosen in saturation bias condition and strong inversion regime. For a same electrical field (V_{ds} is scaled down), μ is assumed to be constant in these bias conditions; then the scaling factor (equation 2) is assumed to be proportional to $\frac{1}{t_{ox}L_{ch}}$. As seen in Fig. 9a and 9b, the measured δ_{id} is proportional to this scaling factor while δi_g is proportional to $\frac{2I_{ds}(A/m)}{g_m{}^2(S/m)^2}$. Moreover, Fig. 10 shows that measured values of g_m are also proportional to the scaling factor. Finally, the measured values of C_{gsi} (Fig. 11) are not strongly dependent of the down scaling process, for instance the variation of C_{gsi} between the FD 130 nm and the bulk 65 nm is very low. These experimental variations of the intrinsic noise sources δ_{id} and δi_g and the electrical parameters g_m and C_{gsi} confirm that well known dimensionless P, R and C [14] noise parameters are not strongly dependent of the down scaling process even for 65nm MOSFETs. The limitation of the noise properties comes rather from the electric parameters (access resistances, fringing capacitances…) [13].



(a)



(b)

Fig.9. Current noise sources for different technology nodes at 6 GHz (the total gate width is fixed at 50 µm for all the devices) versus a down scaling factor for the same (V_{gs}-V_{th}) chosen in low noise bias conditions: (a) Drain current noise source versus $g_m{}^2$ / (2 I_{ds}), (b) gate current noise source versus (2 I_{ds}) / $g_m{}^2$.

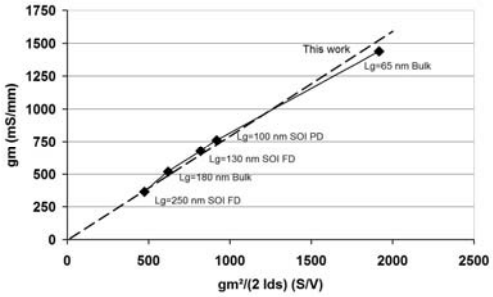


Fig.10. Intrinsic transconductance for different technology nodes versus $g_m{}^2$ / (2 I_{ds}).

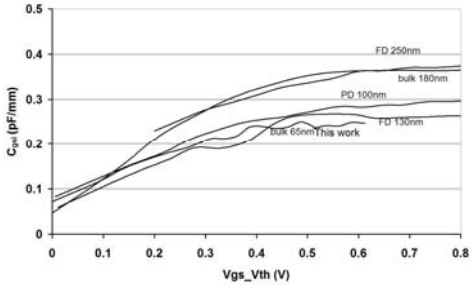


Fig. 11. C_{gsi} versus the gate voltage overdrive (V_{gs}-V_{th}).

	R_g (Ω)	R_s (Ω.mm)	R_d (Ω.mm)	g_m (mS/mm)	g_d (mS/mm)	C_{gin} (pF/mm)	C_{Miller} (pF/mm)	T_{out} [15] (K)
65	1.78	0.07	0.13	1155	133	0.50	0.30	1500
45	2.3	0.07	0.13	1890	240	0.54	0.34	1500

TABLE I: Equivalent circuit of 65nm n-MOSFET (measured) and for hypothetical 45nm (extrapolated)

IV. PERSPECTIVES OF NOISE PROPERTIES OF THE FUTURE GENERATION OF MOSFETS

The objective of this paragraph is to give an order of magnitude of the HF noise properties of the next generation of MOSFET (45nm) by using the previous experimental results. By considering NF_{min} and G_{ass} (Fig. 6.), this 65nm technology could be very attractive to low noise, low power applications up to Ka band (26 – 40 GHz). Indeed NF_{min} is close to 2.3 dB and G_{ass} close to 12dB at 30 GHz. But it should be interesting to know if the next generation could be reached the civil applications in the V and W bands. By multiplying the scaling factor (equation 2) by 1.7 (maximum theoretical value is 2.09) between the 65nm and 45nm and using the experimental results of paragraph III., we obtain the hypothetical noise result shown in Fig. 12 for a 50x0.5 µm MOSFET. Although this simulated NF_{min} does not reach the InP-based 100nm HEMTs ones (close to 1 dB at 77GHz), these hypothetical performances are quite promising both in term of noise figure and associated gain (respectively ~1.8dB and ~10dB at 77GHz). The electrical parameters used for the simulation are reported in table I. This hypothetical noise performance added to low loss transmission lines realized on high resistivity SOI substrate could be attractive for V and W bands low cost applications.

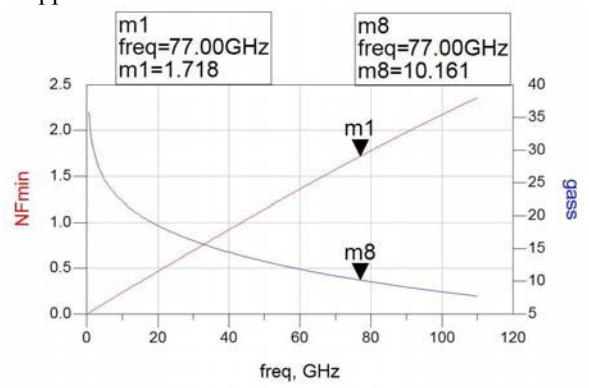


Fig. 12. Extrapolated NF_{min} and G_{ass} of a hypothetical 45nm MOSFET (50x0.5µm).

V. CONCLUSION

This study relates the high performance of 65nm bulk n-MOSFETs in term of cut-off frequencies and microwave low noise properties at the state-of-the-art. This technology presents high f_t of 210 GHz and ultra low noise and high gain characteristics (NF_{min}= 0.8dB and G_{ass}=17.3 dB at 12 GHz) allowing high interests for low cost up to Ka band applications. Moreover, this experimental study proves that the high frequency noise properties of this node continue to follow the downscaling process what is a very good trend for the following node (45nm) for low cost V and W bands low noise, low power applications.

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