On-state safe operating area of GaAs MESFET defined for non linear applications

N. Ismail[1], N. Malbert[1], N. Labat[1], A. Touboul[1], J-L. Muraro[2], F. Brasseau[2], D. Langrez[2]

[1]Laboratory IXL, University Bordeaux 1, 351 cours de la Libération, 33405 Talence CEDEX, France, Tel : 33 540 00 2859

[2] Alcatel Space, Toulouse, 26 Avenue JF Champollion, 31037, France

Abstract — **This paper provides a new approach to evaluate the transistor safe operating area at nominal operating conditions which has been demonstrated on MESFET technology. It consists on performing on-state and off-state accelerated DC step stresses for bias conditions which can be reached by the Vds and Vgs sweeps in overdrive conditions. Both on-state and off-state stresses shown different degradation modes which can be attributed to the different stress bias conditions. On the one hand, the on-state stress corresponds to the impact ionization regime where the drain-gate voltage is considered as an accelerating factor for the device degradation. On the other hand, the off-state stress is performed for bias conditions which correspond to the gate leakage current regime in the reverse Igs-Vgs characteristics where the drain-gate voltage and the gate current are considered as an accelerating factor for the device degradation.**

I. Introduction

For space applications, solid state amplifiers, based on compound semiconductor devices, can operate under critical conditions with high gain compression. These particular specifications correspond to overdrive operation conditions. Nowadays, the methodology to guarantee component lifetime with safety margins is based on standard specifications for space and military applications such as ECSS, MIL, …They require to apply derating coefficient to the maximum parameters (voltage, current, temperature, …) allowed by the component manufacturer [1]. Hence, the standard specifications are not satisfactory due to :

- Cautious definition of the component max ratings,
- Inadequacy between the required performances of the application and the transistor operating area defined by standards; it is particularly for non linear applications for which the overdrive specifications require operating the amplifier under high gain compression. In this case, these operating conditions are covered by specific RF life-tests to assess the reliability of the circuits.
- Absence of realistic definition of the dynamic Safe Operating Area (SOA) of the transistor.

This work presents a new approach, based on results of on-state and off-state DC step stresses, to evaluate the safe operating area of the transistor, candidate to operate in overdrive conditions.

The technology under test is a GaAs MESFET with 0.5µm long and 6x50µm wide gate. Accelerated stress tests were performed using a BILT System BE100. Current-voltage (I-V) measurements, monitored by a HP4142B semiconductor parameter analyser, were performed periodically to record the device parameters drifts. Prior to the stress, all devices were submitted to a stabilizing step during 48 hours.

II. Definition of the device operating area before stress

Fig. 1 presents the on-state breakdown loci, measured for several gate current conditions and using the Gate-current Extraction Technique [2], for the MESFET technology. Before performing any stress, it is necessary to determine the operating area within which the device operates without burn-out. The on-state breakdown loci measured from low to high breakdown conditions show that, the higher breakdown condition, the closer on-state breakdown loci (Fig. 1). The operating area limit corresponds to the grey dashed line joining the exponential region extreme points of each on-state breakdown locus. Operating the transistor out of this region leads to its destruction since Vdg values become larger than the gate-drain breakdown voltage BVdg.

III. Accelerated DC step stresses in the on-state regime

The methodology consists in applying accelerated voltage step stresses with bias conditions (Vds, Vgs) defined by the following sequence: an identical value of Ids is adjusted at the beginning of each step and |Igs| is increased for each step until the evolution of Ids or Igs, exceeds 10% over one step. The duration of each step is 48 hours. Several sequences are performed for different values of Ids located in the device operating area. After performing the stress sequences, the couples of points (Igs; Ids), which correspond to the stress conditions, allow to define the limit of the safe operating area of the device. It is important to point out that this area represents a safe operating area for non linear applications since the accelerated DC step stresses are performed in regions, which can be reached by the Vds and Vgs sweeps in real overdrive operating conditions.

We have applied this methodology for four stress sequences with Ids values of 0.33, 3.3, 10 and 16.6 mA/mm respectively. The evolution of the monitored parameters during the stress is an increase of Ids and Igs. For each value of Ids, we have reported in

(Ids; Igs) mA/mm	(**0.33**;-0.01)	(**0.33**;-0.02)	(**3.3**; -0.04)	(**3.3**; -0.08)	(**10**; -0.05)	(**10**; -0.08)	(**16.6**;-0.08)	(**16.6**;-0.12)
(Vds; Vgs) V	(15; -2.5)	(15.5; -2.5)	(16; -2.4)	(16.7; -2.6)	(15.5; -2.1)	(16; -2.2)	(15.7;-2.04)	(16.1;-2.08)
Degradation of (Ids; Igs) %	(+8; +13)	(+14; +15)	(+5; +4)	(+30; +53)	(+1; +0.3)	(+2; +20)	(+1 ; +8)	(+1 ; +26)

TABLE I

DEGRADATION OF Ids AND Igs AFTER STEP STRESSES PERFORMED WITH SUCCESSIVE INITIAL VALUES OF Ids OF 0.33, 3.3, 10 AND 16.6 mA/mm.

(Vgs; Vds) V	(**-3**; 10)	(**-3**; 12)	(**-3**; 14)	(**-3**; 16)	(**-10**; 5)	(**-10**; 7)	(**-10**; 9)	(**-10**; 11)
Degradation of Idss (%)	-0.9	-0.9	-0.7	-0.5	-1	-0.9	-0.6	-0.3
Degradation of Vt (%)	+1	+1	+1	+1	-1	-1	-1	+1
Degradation of Gm (%)	+0.5	+0.05	-0.08	-1.9	-1.3	-0.7	-1	-2.2

TABLE II

DEGRADATION OF THE TRANSISTOR STATIC ELECTRICAL PARAMETERS AFTER THE OFF-STATE STEP STRESSES: SATURATION CURRENT Idss@Vds=3V AND Vgs=0V, THRESHOLD VOLTAGE Vt@Vds=3V AND Ids=1mA/mm AND TRANSCONDUCTANCE Gm@Vds=3V AND Vgs=-1V.

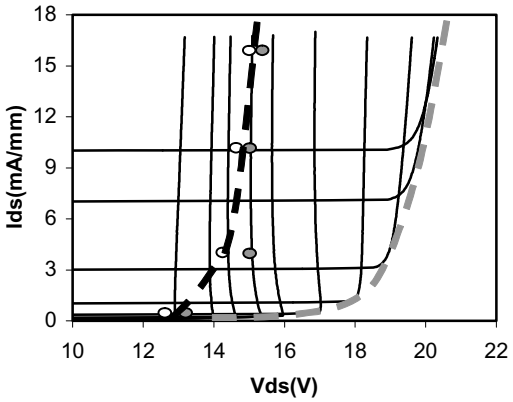

Fig. 1. On-state breakdown loci of the MESFET under test for different breakdown conditions: Ig=-0.016, -0.032, -0.05, -0.08, -0.13, -0.33, -1, -3, -7 and –10 mA/mm from left to right respectively. The grey dashed line defines the limit of the device operating area before stress and the black dashed line is the limit of the device safe operating area after stress. The white dots correspond to stress conditions inducing a drift of Igs or Ids lower than 10% whereas, grey dots correspond to stress conditions inducing degradation higher than 10%.

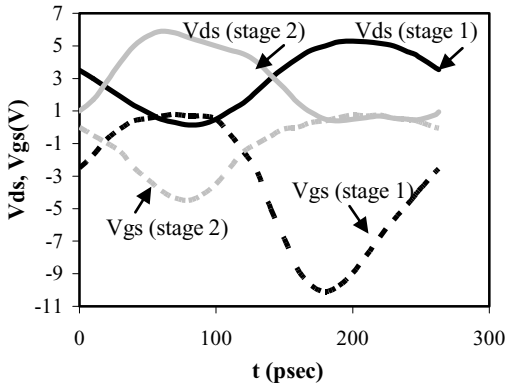

Fig. 2. Simulated drain-source and gate-drain voltage waveforms for Pin=+18dBm @ 3.8 GHz of the two stages amplifier based on MESFET.

Table I the stress bias point which corresponds to current shift lower than 10% and the one which corresponds to degradations higher than 10%.

From the evolution of parameters monitored during the stress sequences, the contour delimiting the safe operating area can be located between the different bias points of the performed stresses. Finally, the black dashed line in Fig. 1 is the limit of the safe operating area of the MESFET. It is important to point out that stress conditions were defined in correlation with satellite mission specifications. So, the choice of a more or less severe stress conditions leads to a shift to the left or the right of the contour delimiting the transistor safe operating area.

IV. ACCELERATED DC STEP STRESSES IN THE OFF-STATE REGIME

The simulated drain-source and gate-source voltage waveforms of a low level amplifier operating under overdrive conditions and composed of two MESFET stages (Fig. 2), point out that Vds sweeps between 0V and 6V and that Vds values are then included in the MESFET safe operating area.

Regarding Vgs sweeps during the amplifier overdrive operation, waveform calculation indicates that Vgs varies from 0.8V to -10V. The region which corresponds to Vgs higher than –2.6V is included in the MESFET safe operating area defined from the on-state stresses while the one corresponding to Vgs between -2.6V and -10V corresponds to off-state breakdown bias conditions. Consequently, we have performed 48 hours accelerated DC stresses at different bias conditions in the off-state breakdown regime [3].

The methodology consists in applying voltage step stresses with bias conditions defined by the following sequence: Vgs is held constant and Vds is increased step by step. We have performed DC stresses for different

sequences with Vgs values of -3V, -4V and –10V corresponding to the off-state breakdown regime.

As expected, these stresses have induced drifts of Igs and Ids higher than 30% while weak degradation of the device static characteristics are observed after the stresses (Table II).

Finally, we have observed that the Vds sweeps comprised between 0V and 3V are included in the safe operating area of the MESFET for Vgs higher than –2.6V. On the contrary, Vds sweeps comprised between 3V and 6V are located in a border zone of the MESFET operating area for Vgs between -2.6V and -10V. The operation of devices in this region must be validated by life-tests reflecting the real operation conditions in terms of life-test duration and electrical stress conditions.

V. COMPARISON OF THE DEGRADATION MODES OBSERVED AFTER THE ON-STATE AND OFF-STATE STRESSES

From the evolution of parameters measured after stresses and summarized in Table III, we have observed that the MESFET presents different degradation modes for the on-state and off state stresses.

The different degradation modes recorded after the on-state and off state stresses show their dependence on the stress bias conditions [4]. Indeed, on the one hand, the on-state stress is performed in impact ionization regime at high drain-source voltage [4]. On the other hand, the off-state stress is performed for bias conditions close to the gate-drain breakdown region without impact ionization mechanism at high gate-source voltage [5]-[6].

Electrical parameters	On-state stress	Off-state stress
Ids	Linear increase	Square root decrease then a linear increase
|Igs|	Linear increase	Square root decrease then a linear increase
Idss	Constant	Constant
Vt	Constant	Constant
Gm	Constant	Constant
I_{II}	Decrease	Constant until S3 then increase
$\|Ig_{leakage}\|$	Increase	Decrease until S3 then increase
BV-on	Decrease	Increase until S3 then decrease
BV-off	Decrease	Increase until S3 then decrease

TABLE III
THE DEGRADATION MODES RECORDED FOR THE MESFET AFTER THE ON-STATE AND OFF-STATE STRESSES DESCRIBED BY THE EVOLUTION OF THE STRESS BIAS CONDITIONS Ids, Igs, THE DRAIN SATURATION CURRENT Idss, THE THRESHOLD VOLTAGE Vt, THE TRANSCONDUCTANCE Gm, THE IMPACT IONIZATION CURRENT I_{II}, THE REVERSE LEAKAGE CURRENT ($Ig_{leakage}$), THE ON-STATE BREAKDOWN VOLTAGE BV-on AND THE OFF-STATE BREAKDOWN VOLTAGE BV-off.

After all DC stresses, the weak evolution of Idss, Vt and Gm suggests a weak evolution of the depletion region extension between gate and drain. This result means that hot electrons have induced weak interaction with traps located between gate and drain.

This hypothesis is confirmed by drain current transient measurements [7], performed before and after the "on-state" and "off-state" stresses. Indeed, after stress, the shape of the drain transients has not changed. This suggests that no new kind of traps were created during the stresses [8]. The slight change in the amplitude of the drain current transients after stress reveals a weak evolution of the density of the existing traps.

As stated in Table III, there is a threshold Vds value of the off-state stress bias conditions, for which the degradation modes change. Indeed, for stress sequences with Vgs=-3V and Vgs=-10V the degradation modes change for Vds=16V and Vds=11V, respectively and may be attributed to a degradation of the Schottky diode as shown in Fig. 4.

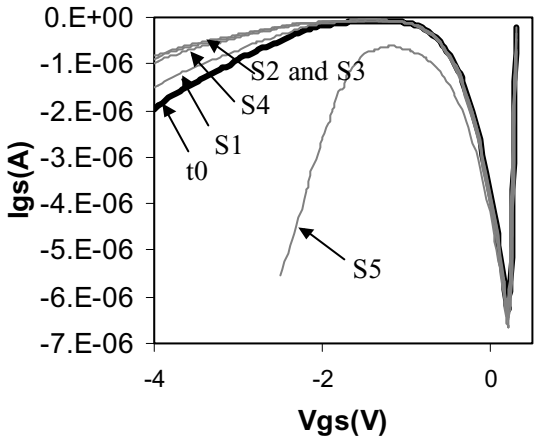

Fig. 3. Evolution of the MESFET reverse Igs-Vgs characteristics, for Vds=11V, before (black curve) and after (grey curves) off-state step stresses at Vgs= -10V.

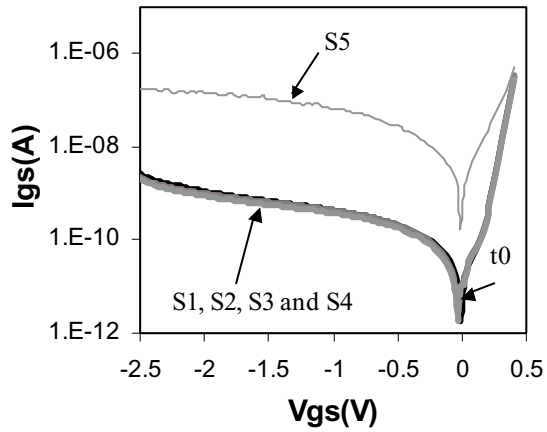

Fig. 4. Evolution of the MESFET Schottky diode characteristics before (black curve) and after (grey curves) off-state step stresses at Vgs= -10V.

We notice that the evolution of the on-state and off-state breakdown voltages is correlated with the evolution of the reverse gate leakage current of the MESFET

(Table III). In particular, the leakage current of the gate-drain diode first decreases until the step S3 of the off-state stress then it increases during the following steps S4 and S5, which lead to the successive increase and decrease of BV-on and BV-off (Fig. 3 to 5).

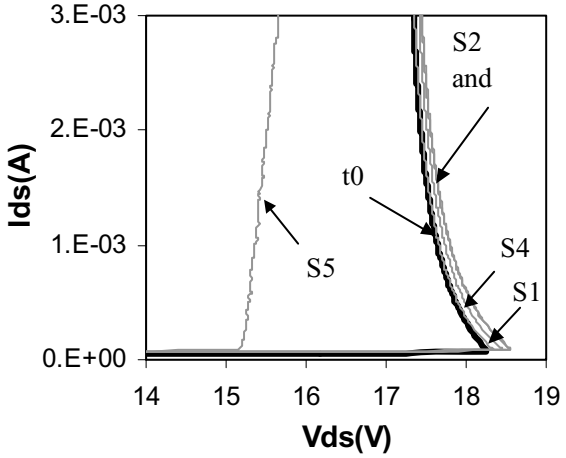

Fig. 5. Evolution of the MESFET on-state breakdown locus, for Igs=-1mA/mm, before (black curve) and after (grey curves) off-state step stresses at Vgs= -10V.

VI. Discussion and conclusions

A 4000 hours RF stress under 15dB gain compression @ 4 GHz has been performed on a low level amplifier operating in the C band and composed of two stages; each one based on a MESFET. The stress conditions correspond to the overdrive specifications. This stress has induced very weak degradation of dynamic (Fig. 6) and static performances of the amplifier.

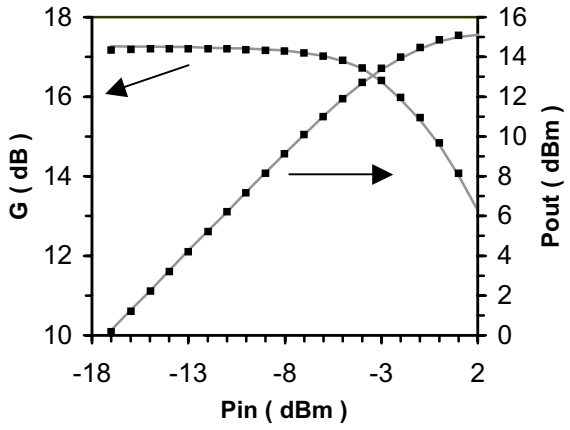

Fig. 6. Amplifier output power and gain versus input power before (black curves) and after (grey curves) 4000 hours life test RF under 15dB gain compression @ 4GHz.

Hence, the results of RF stress performed in non linear conditions confirm the methodology, used in this work, to define the transistor safe operating area for overdrive conditions. Indeed, the accelerated DC step stresses were performed in regions, which can be reached by the Vds and Vgs sweeps in overdrive real operating conditions. In our case, Vds and Vgs waveforms plotted in Fig. 2, show that the stage 1 of the amplifier is the worst case for the Vds and Vgs sweeps. We can estimate that the amplifier operates in overdrive conditions for about 100 picoseconds in a RF cycle. Hence, an estimation of the cycle number of the amplifier operation at overdrive conditions in the total satellite mission, allows to calculate the cumulative DC stress duration representative of the overdrive occurrence in the real operating conditions. The DC stress step duration of 48 hours is in agreement with the value estimated from Vds and Vgs waveforms in overdrive conditions and the operation frequency of the circuit.

Moreover, since during the RF stress, the Vds and Vgs values only reach critical ones for short duration, RF stress is assumed to provoke weaker degradation due to hot electrons, than the DC stress. As a consequence, the DC safe operating area is included in the safe operating area defined from accelerated RF stress performed in overdrive conditions. Therefore, the safe operating area defined from accelerated DC stress presents a more restricted and safe operating area for the transistor than the one that could be defined from RF stresses.

We have presented, in this paper, an evaluation of the MESFET safe operating area for non-linear operation in overdrive conditions. The methodology consists in applying accelerated DC step stresses in the breakdown regions. It has been validated by RF stress tests performed in overdrive conditions.

References

[1] J. L. Muraro, et al., "GaAs power MMIC: A design methodology for reliability," *Microelectronics Reliability,* Vol. 37, N°10/11, pp.1651-1654, 1997.

[2] M.H. Somerville, et al., "A new gate current extraction technique for measurement of on-state breakdown voltage in HEMT's," *IEEE Transactions on Electron Devices,* Vol. 19, N°11, pp. 405-407, November 1998.

[3] Sandeep et al., "A new Drain-Current Injection Technique for the Measurement of Off-State Breakdown Voltage in FET's," *IEEE Transactions Electron Devices*, Vol. 40, N°8, pp. 1558-15560, August 1993.

[4] M. Borgarino, et al., "Hot Electron Degradation of the DC and RF Characteristics of AlGaAs/InGaAs/GaAs PHEMT's," *IEEE Transactions Electron Devices*, Vol. 45, N°2, pp. 366-372, February 1998.

[5] R. Menozzi, "High-field phenomena and reliability issues in microwave heterojunction FET's," in *Proceedings of EDMO,* 1999, pp.75-80.

[6] R. Menozzi, et al., "Bias point dependence of the hot electron degradation of AlGaAs/GaAs Power HFETs," in Proceedings of GaAs IC, 1999, pp. 171-174.

[7] S.H. Lo SH and C. P. Lee, "Analysis of Surface State Effect on Gate Lag Phenomena in GaAs MESFET's," *IEEE Transactions Electron Devices*, vol. 41, no. 9, 1504-1511, 1994.

[8] N. Labat, et al., "Analysis of hot electron degradation in pseudomorphic HEMTs by DCTS and LF noise characterization," *Microelectronics Reliability* 37, pp. 1675-1678, 1997.