IC compatible MEMS technology

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***Abstract* – This paper deals with an Integrated Circuits (ICs) compatible MEMS technology, which is used to elaborate an ultra compact RF communication module centered at 24GHz. This technology uses conventional equipments and is in adequation with millimeterwave applications. A compatibility test protocol has consequently been defined in order to check that each technological step does not degrade the SiGe circuits' performances. Finally, the realized demonstrator present a total surface of only 9mm².**

I. INTRODUCTION

Miniaturization, low cost and high performances for microwave and millimeterwave applications represent the main leitmotivs of the future mass market communication modules. New technological solutions have consequently to be defined to fulfill all these requirements. Some researches are based on bulk or surface silicon micromachining techniques [1-2], others use polymers to elevate passive components for the lossy substrate [3-6].

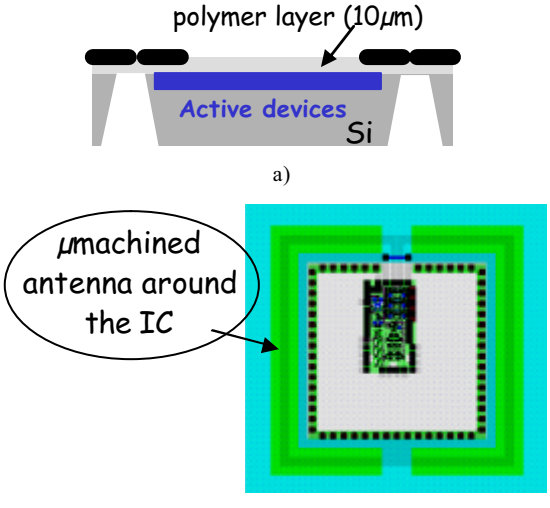


Figure 1. Schematic of an antenna with micromachined trenches: a) cross and b) top views

In this paper, a technological solution based on the post-processing of a suspended antenna around the integrated circuits using SiGe heterostructure is proposed, as indicated in Figure 1. Thanks to an appropriate antenna design [7] placed all around the ICs, the total surface of the communication module can be drastically reduced.

The corresponding 'above IC' technology presents many advantages. It is compatible with millimeterwave applications and only conventional equipments of microelectronics are employed. It implies indeed the use of a thick organic layer, which is employed as a dielectric membrane in our case, metallization layers for the antenna and the interconnections between the SiGe circuit and the antenna, and finally the substrate micromachining. In order to validate the use of all these technological steps on SiGe wafer without any deterioration of the active circuits, a specific protocol of compatibility has been developed and evaluated.

This compatibility test protocol will first be described and employed to define the limit temperature, which is IC acceptable. The second part of this paper will be dedicated to the 'above IC' technology description. Next part will present the final demonstrator.

II. : COMPATIBILITY TEST PROTOCOL: LIMIT POST-PROCESS TEMPERATURE ON SIGE CIRCUITS

In order to verify the compatibility of the post-process steps with the active circuits, a test protocol has been developed. It simply corresponds to measure test transistors before and after the technological stress. Several measurements have been evaluated:

- static performances with I(V)
- and low frequency noise measurements, which modification corresponds to changes in the SiGe heterostructure.

This protocol has been applied to define the limit temperature, which the circuits can sustain.

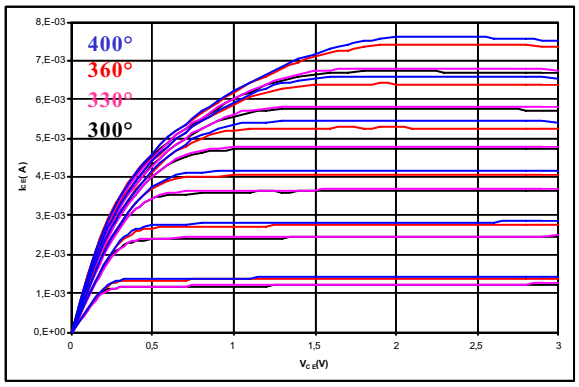


Figure 2. Static performances of a test transistor during a temperature ramp

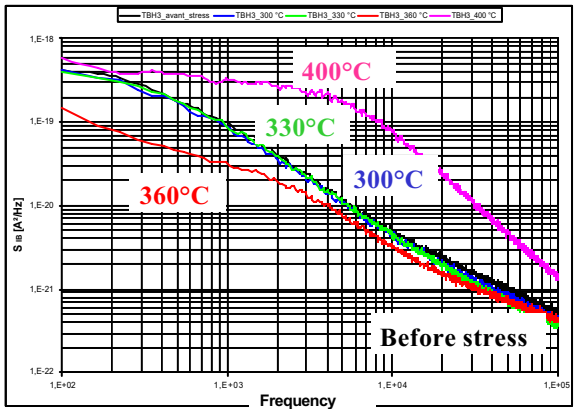


Figure 3. Low frequency noise density on the base current during ramp temperatures

A temperature ramp has thus been applied on the SiGe wafer, from 300°C up to 400°C.

The corresponding measurements, static and low frequency ones, are presented in Figure 2 and Figure 3 respectively. Both figures exhibit modifications with temperatures of 360°C and 400°C. The collector current is increased as well as the low frequency noise density on the base current. This clearly proves a strong impact of the temperature on the SiGe heterostructure, with the creation of generation-trap centers.

In conclusion, the limit temperature, which can be sustained by the active circuits, is situated between 330 and 360°C. The maximal temperature budget of the 'above IC' technology corresponds consequently to 330°C, in order to avoid any trouble.

III. 'ABOVE IC' TECHNOLOGY DESCRIPTION

The complete 'above IC' technology is described in Figure 4. The first step consists in thinning the substrate in order to minimize the final silicon etching time and suppress all remained dielectric passivations. After a cleaning step and a plasma treatment, the interconnections between the antenna and the active circuits are realized through an electroplating of 10µm thick into a corresponding photoresist mould. This mould is then replaced by a thick organic layer in benzocyclobuten (BCB from Dow Chemicals [8]). This polymer is spun on the wafer, patterned and then cured at 250°C to polymerize it. This organic layer has been chosen because of its low loss tangent particularly appropriate for high frequency applications and its low thermal budget. Composite mineral membranes, such as SiO_2/SiN requires indeed fabrication temperature up to 1000°C.

Next step deals with the antenna metallization. To enhance the adhesion of the metal on top of the BCB, a plasma treatment is performed just before the evaporation of a Ti/Au seed layer.

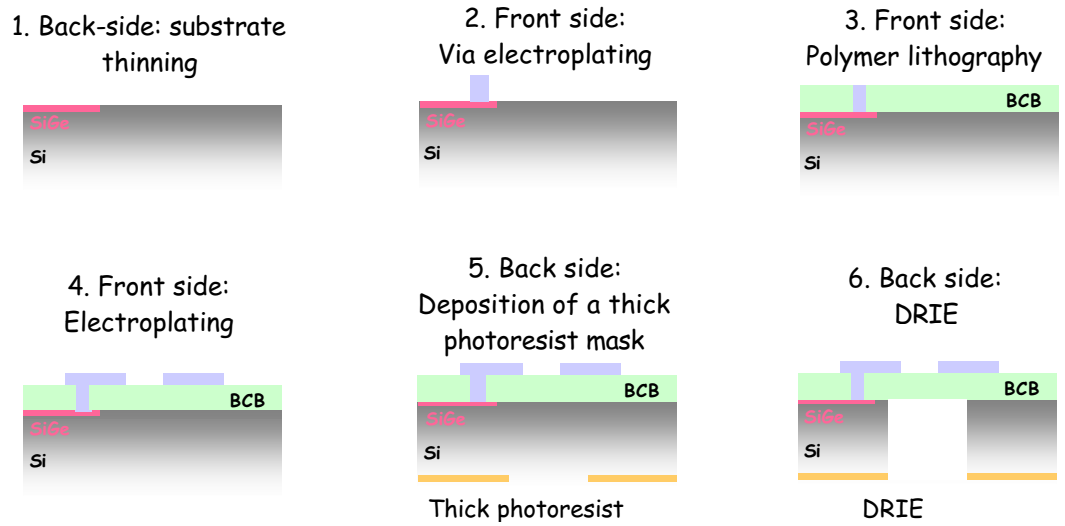


Figure 4. Micromachined above IC technological process flow

The 3µm thick antenna is then electroplated into a photoresist mould. This mould and the seed layer are then removed in the antenna slots. Finally, a photoresist of 10µm thick is then patterned on the back side side of the wafer and will serve as a mask during the silicon micromachining. This one is performed with the Deep Reactive Ion Etching (DRIE) technique in order to release the antenna under its slots.

The DRIE technique has been chosen for several reasons. First the wet etching, such as potassium hydroxide bath (KOH), induces large micromachined area, as the etching angles follow the silicon crystal plans (cf. Figure 5). This is absolutely not appropriate to realize ultra compact RF module.

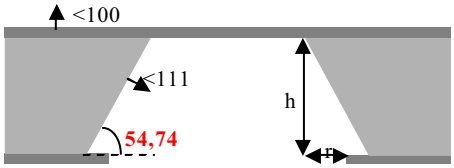
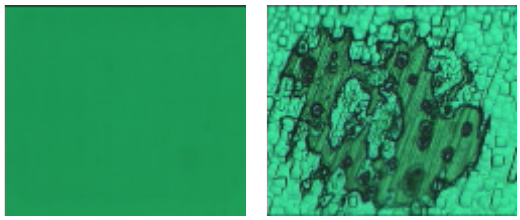


Figure 5. Wet silicon etching angles

The second drawback is driven by the back side mask required during the humid micromachining. Only few masks can resist to such an attack. Silicon nitride SiN is one of the main robust. However, because of the back side thinning of the substrate, the roughness is strongly accentuated and causes the mask to peel off, as shown in Figure 6.



a) b)

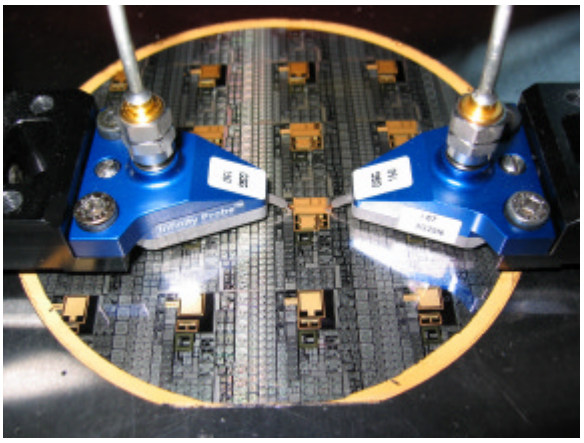
Figure 6. PECVD silicon nitride on a) standard Si wafer and b) SiGe wafer

On the other side the DRIE enables the realization of straight trenches, which really provide compacity to the module. The required mask may be a simple thick photoresist, easily removed at the end of the process.

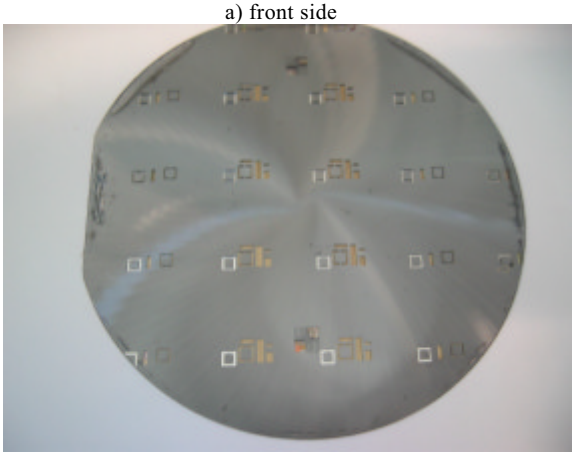
In both cases, the Si etching well stops on the polymer layer.

IV. PRE-VALIDATION OF THE 'ABOVE IC' TECHNOLOGY

In order to evaluate the compatibility of the technology, a dedicated area on SiGe wafers has been used to implement coplanar filters and various antennas, close to other ICs, but without any connection to the active circuits. Figure 7 presents the pictures of the front and back side of a post-processed wafer, including the silicon etching.



a) front side



b) back side

Figure 7. Pictures of a post-processed wafer

Each post-processed element (filters, antennas, CPW) has been successfully characterized and exhibited the expected performances. The SiGe test transistors have also been evaluated. The resulting low frequency noise measurements before and after process are identical.

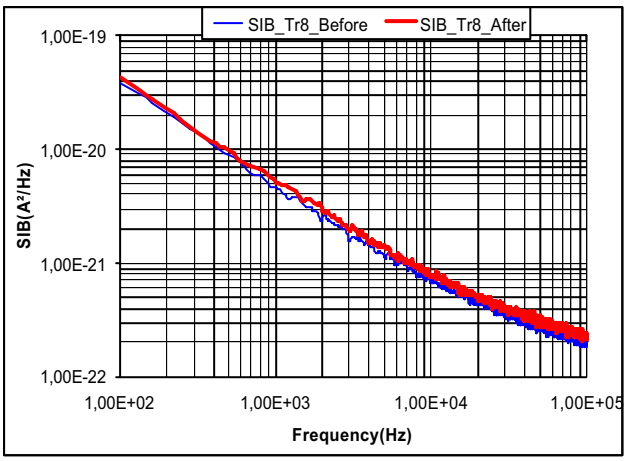


Figure 8. Impact of the post-process on the low frequency noise measurement

This result demonstrates the adequation of the post-processing with the ICs.

V. FINAL DEMONSTRATOR

Finally, the complete RF module centered at 24GHz has been designed. The corresponding layout has taken the post-processing antenna space into account, as indicated in Figure 9.

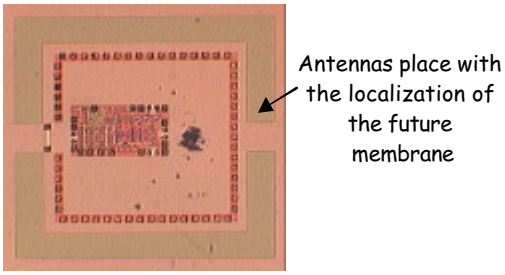
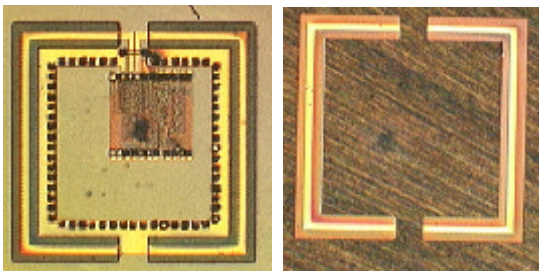


Figure 9. RF module before the post-processing

Figure 10 indicates the final demonstrator after the 'above IC' technology.



a) b)

Figure 10. Post-processed antenna with IC's : a) top side and b) back side

The post-processing has successfully been applied, including the interconnections between the antenna and the active devices.

VI. CONCLUSIONS

To conclude, an 'above IC' technology has been developed in order to realize ultra compact RF module. The antenna is placed all around the RF module based on SiGe heterostructures transistors. The post-process only implied conventional equipments in microelectronics. Its compatibility has been evaluated. No deterioration of the active circuits has been encountered. The final demonstrator centered at 24GHz only exhibits a surface of 9 mm².

ACKNOWLEDGEMENT

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