

# A High Gain-Bandwidth Product Distributed Transimpedance Amplifier IC for High-Speed Optical Transmission Using Low-Cost GaAs Technology.

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*This paper reports a distributed baseband transimpedance amplifier for optical links up to 10 Gb/s. The amplifier operates as a baseband amplifier with a transimpedance gain of 48 dB $\Omega$  and a DC-to-9 GHz bandwidth. Some innovative design techniques to improve gain-bandwidth performance at low and high frequency with an available low-cost GaAs MESFET technology have been developed.*

## INTRODUCTION

Optical links are regarded as the unique solution for multigigabit communication applications not based on electromagnetic transmission. Associated to the optoelectronic devices, microwave transimpedance amplifiers represent key components in term of noise figure and dynamic range.

Baseband front-end amplifiers operating from DC to several GHz are required from high speed optical transmission systems. Classical direct-coupled baseband transimpedance amplifiers have high gain but their high frequency performance is limited by the parasitic capacitances of the transistors. Their upper frequency limit is empirically known to achieve only a 30% of the transition frequency ( $f_T$ ) of the transistors (1). If we use commercially-available 0.5  $\mu\text{m}$  gate length GaAs MESFET's, which have the  $f_T$  of 20 GHz, we can achieve only a 5-6 GHz bandwidth with such lumped element design technique. Moreover, the achievable gain is very often too low and need further amplification stages to satisfy the receiver specifications.

On the other hand, the distributed amplifier technique has been widely applied in multioctave amplifiers. They are featured by artificial input and output transmission lines that are constructed combining external lumped inductors or transmission lines and the device capacitive elements. Such artificial lines have very high cut-off frequencies resulting in amplifiers exhibiting inherently wideband characteristics.

Bandwidth specification for a 10 Gb/s optical link requires a baseband front-end amplifier with an upper frequency limit of at least 7 GHz, 70% of the bit rate of 10 Gb/s, to equalize the 10 Gb/s NRZ pulse waveform. However, even if it is not difficult to obtain such bandwidth characteristics with a commercial 0.5  $\mu\text{m}$  GaAs MESFET technology, the resulting gain performance may be inadequate once more. This led us to develop new design techniques

to meet the gain-bandwidth specifications with the available technology.

This paper describes some innovative design techniques to improve gain-bandwidth performance at low and high frequencies. Making use of such techniques an amplifier IC with a high gain-bandwidth product using a low cost 0.5  $\mu\text{m}$  GaAs MESFET technology has been developed and tested.

## DESIGN GUIDELINES

In designing microwave distributed amplifiers, it is usually desirable to achieve the maximum gain-bandwidth product allowed by the selected transistor. The design targets are twofold : from one hand the achievement of a transimpedance gain higher than 45 dB $\Omega$  in a minimum bandwidth of 7 GHz, and on the other hand the compensation of the capacitive loading of the input photodiode to hold the required performance even with low-cost photodetectors in a 10 Gb/s optical link.

The distributed amplifiers have been extensively used for broadband applications, but hardly achieve the required gain characteristics due to the losses of gate and drain lines. The cascode pair has been used to obtain wide band characteristics providing a broadband loss compensation for the drain artificial line. In fact, at low frequencies output impedance is higher in the cascode pair than in the common-source MESFET, supplying higher output currents when loaded on a 50  $\Omega$  drain line. Moreover, the frequency behaviour of the real part of the output impedance compensates the drain line losses at higher frequencies. The former characteristics account for higher gains, the latter for wider bandwidths for the distributed amplifier (2),(3).

In many cases, distributed amplifiers do not have a flat gain response from DC. In fact, they can be coupled with a capacitor to form a multi-stage amplifier to achieve higher gain or cannot have DC matching termination to decrease their power dissipation. Moreover, the gain of a distributed

amplifier decreases at low frequency even if it is designed with DC terminations because the output impedance of the amplifier has a frequency dependence. At high frequency, the output impedance is almost the same as the image impedance of the artificial drain line constructed with the lumped inductors and capacitances of transistors. On the other hand, at low frequency, the output impedance becomes low because of the three active device output resistances ( $R_{ds}$ ) connected in parallel. The cascode configuration, however, features a higher impedance even at low frequency.

Moreover, we used a new active drain termination composed of a MESFET load (MDT) with gate and source shorted featuring high AC and low DC impedance behaviour. Moreover a series R-C termination shunts the MDT to properly load the drain line at high frequency. This termination allows a double result with respect to a simple resistor termination, i) the power dissipation to supply the drain bias current is reduced, ii) the DC gain coincides with that at high frequency. In fact, the termination impedance increases as the frequency decreases to compensate for the decrease of the output impedance of the amplifier (4).

The proposed distributed transimpedance amplifier consists of three cascode stages, each composed of two 0.5  $\mu\text{m}$  GaAs MESFET with 4x60  $\mu\text{m}$  gate periphery by Alenia-Marconi System (AMS). The artificial gate and drain line have been designed using spiral inductors or transmission lines when a low inductance value were required. Gate and drain terminations have dumping resistors  $R_f$  in series with RF blocking capacitors to reduce the parasitic effects of external inductances at the bias terminal. The complete circuit schematic is shown in Figure 1.

The input photodiode load has been represented by a current source shunted by a parasitic capacitance and a series inductor to take into account the wire bond mounting. The photodiode and MESFET parasitic capacitances act as a current sink at high frequency, determining the transimpedance gain cut-off frequency, leaving the  $S_{21}$  cut-off frequency practically unmodified. The photodiode capacitance has been included in the gate line, thus eliminating its parasitic effect until it is in the range of MESFET capacitances. In order to further decrease the circuit sensitivity against the changes of the photodiode capacitance, a peaking inductor has been introduced in the last FET drain load to obtain an inductive peaking effect in the high frequency corner of the transimpedance gain and to compensate the gain roll-off due to decreasing impedance in the gate line (2). However, a well balanced gate line should provide the same bandwidth for the transimpedance gain as  $S_{21}$  at the best.

Furthermore, being interested to the performance of the transimpedance gain rather than voltage or power gain of the amplifier, a new design technique

has been implemented to enhance the transimpedance gain frequency performance, leaving the  $S_{21}$  response unmodified. The transimpedance gain, in fact, is calculated from S-parameters as

$$G_{TZ} = Z_0 \frac{S_{21}}{1 - S_{11}}$$

where  $Z_0$  is the external line

characteristic impedance ( $Z_0=50 \Omega$ ). It is easy to understand that the transimpedance bandwidth increases if  $S_{11}$  increases toward unity when  $S_{21}$  starts falling down. On the other hand, the input matching is not an essential requirement for a transimpedance amplifier, therefore if the gate line response is shaped in order to obtain a large and smooth peak before cut-off frequency, the magnitude of  $S_{11}$  increases in the same way at the bandwidth edge, resulting in a transimpedance bandwidth beyond the  $S_{21}$  gain bandwidth limit. The above effect has been achieved tuning the gate line inductors in order to obtain the gain shaping at the desired frequency.

## EXPERIMENTAL RESULTS

The layout of the amplifier is shown in Figure 2, the chip size is 1.7x2.5 mm<sup>2</sup>. On wafer measurements of the circuit S-parameter have been performed. The resulting transimpedance gain with open input termination ( $G_{TZ}$ ), the forward power gain ( $S_{21}$ ) and the factor  $(1-S_{11})$  are depicted in Figure 3. For frequencies below 7 GHz a power gain of 12 dB results. The discussed effect on the corner frequency of the transimpedance gain due to  $S_{11}$  peaking is clearly visible. The initial specifications have been met with 48 dB $\Omega$  gain and bandwidth in excess of 7 GHz. The measured noise figure for different circuit current absorption ( $I_{bias}$ ) have been reported in Figure 4. The 3-dB bandwidth against the input photodiode capacitance distance from the design value is plotted in Figure 5, a photodiode having a capacitance of 0.3 pF was considered. The gain-bandwidth performance is maintained with distance up to  $\pm 0.3$  pF, demonstrating the effectiveness of the design improvement in terms of inductive peaking.

## CONCLUSIONS

This paper describes some innovative design techniques for distributed front-end amplifiers in optical receivers of a 10 Gb/s optical link. The proposed design methodology is based on the cascode configuration, active drain termination, and both gate and drain peaking techniques, to improve the gain-bandwidth performance at low and high frequency with low-cost GaAs FET technology and photodetectors. The initial specifications have been met with 48 dB $\Omega$  gain and bandwidth in excess of 7 GHz. The gain-bandwidth performance is maintained with input capacitance up to 0.5 pF, demonstrating the effectiveness of the design improvement in terms of inductive peaking.

## REFERENCES

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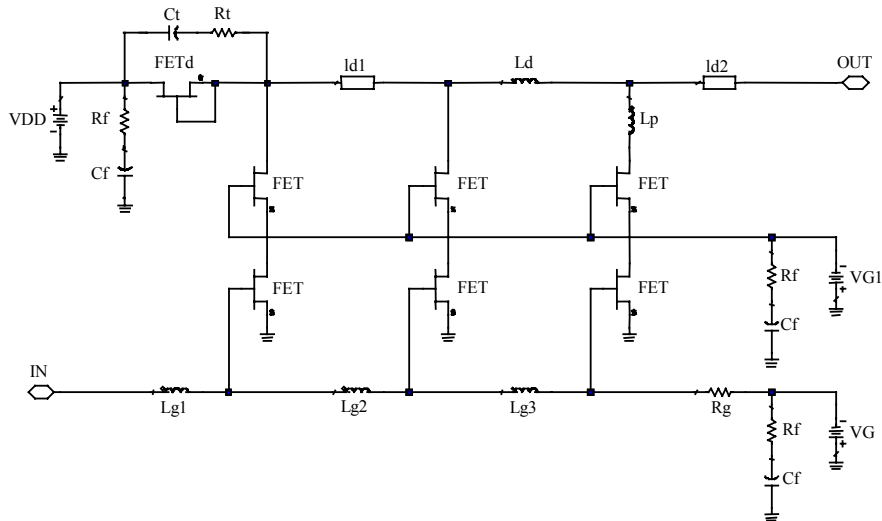


Figure 1. Distributed amplifier circuit schematic

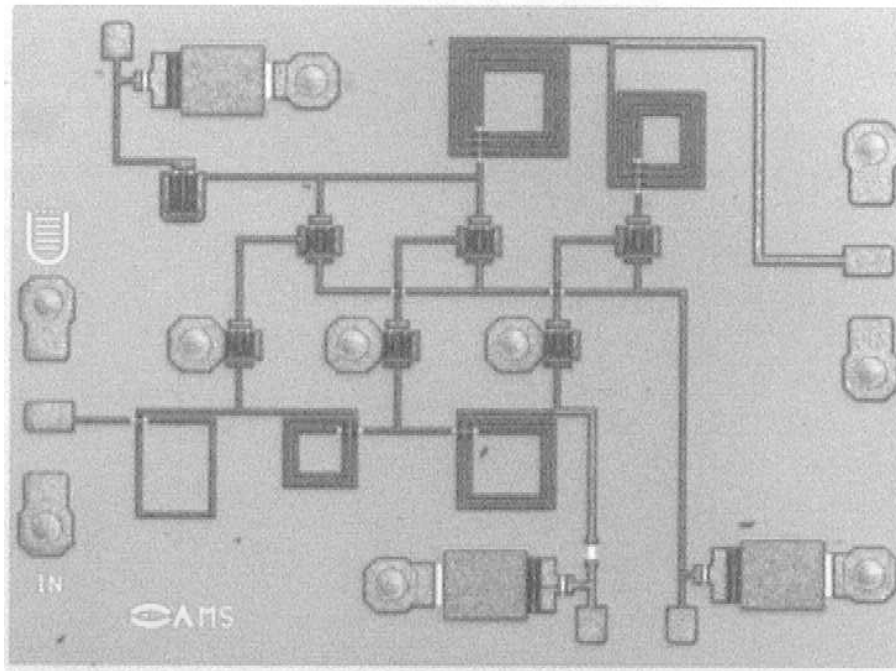


Figure 2. Distributed amplifier monolithic layout (1.7x2.5 mm<sup>2</sup> die size)

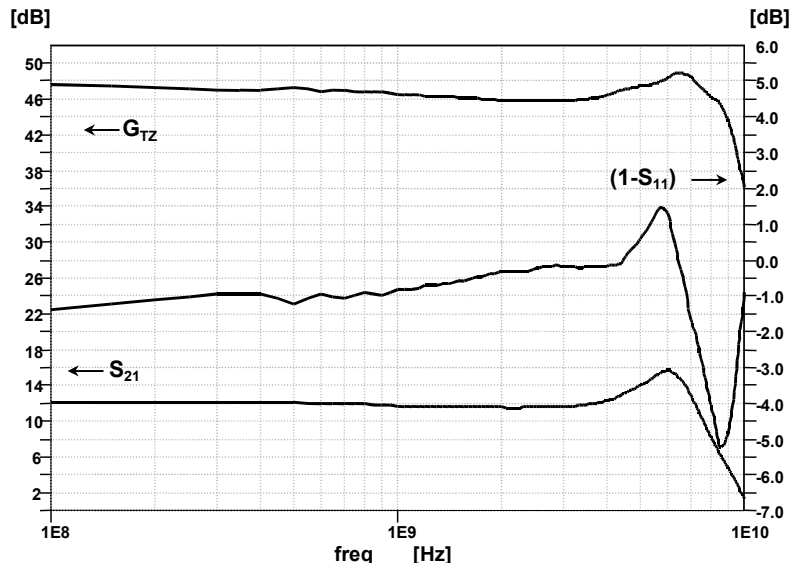


Figure 3. S-parameters and open input transimpedance gain.

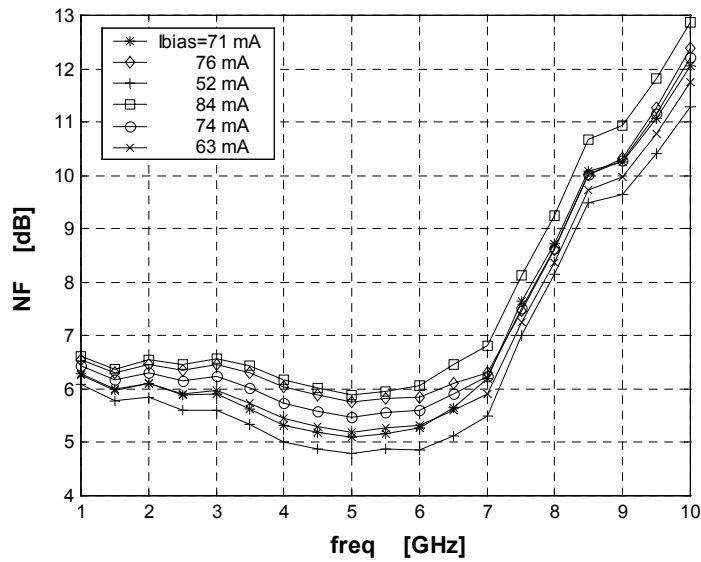


Figure 4. Measured Noise Figure for different circuit current absorption ( $I_{bias}$ ).

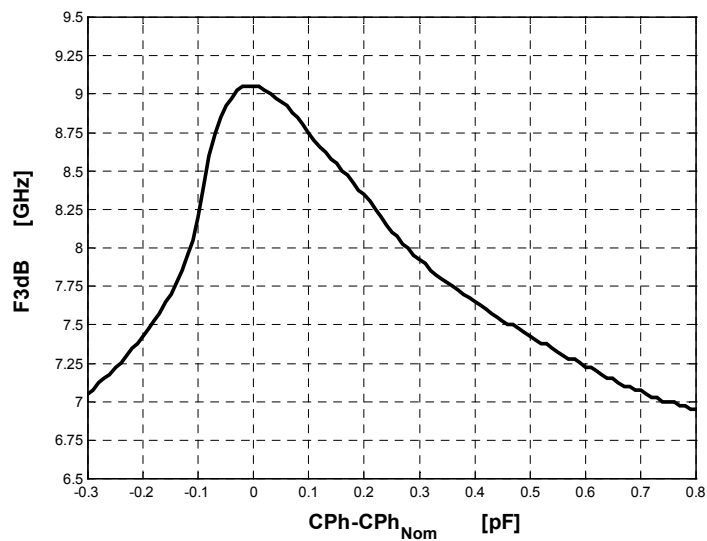


Figure 5. 3-dB transimpedance bandwidth against input photodiode capacitance variation.