Evidence of surface trap effects on pseudomorphic HEMT submitted to impact ionisation stresses

N. Malbert, N. Labat, B. Lambert*, A. Touboul, G. Pataut**

IXL(UMR CNRS 5818), Université Bordeaux 1, 351 cours de la Libération,
33405 Talence Cedex, France, e-mail:malbert@ixl.u-bordeaux.fr
*ESTEC/ESA, Keplerlaan 1 P.O. Box 299 , 2200 AG Noordwijk ZH, The Netherlands
**United Monolothic Semiconductors, Route Départementale 128, BP 46, 91401 Orsay Cedex, France

In this paper, AlGaAs/InGaAs pseudomorphic HEMTs have been submitted to DC life-tests in impact ionisation regime with and without thermal stress. Control devices present an identical and steep shape of the on-state breakdown locus while aged devices present a large dispersion of this characteristic. It seems that some slight modification of the surface properties and/or micro-defects located in the gate-drain region affect the on-state breakdown voltage loci measured with a gate current of 0.13mA/mm. After the two life-tests, the temperature evolution of the surface leakage contribution to the reverse gate current has increased while impact ionisation current remains unchanged. This result is confirmed by a weak temperature dependence of the on-state breakdown voltage measured with a gate current of 1mA/mm. These slight modifications of the surface properties do not affect the reliability of this technology.

INTRODUCTION

Pseudomorphic GaAs HEMTs are widely used in medium power applications. Users are concerned by the reliability of P-HEMT-based technologies submitted to RF overdrive. During RF operation, large electric field takes place in the channel inducing impact ionisation mechanisms. Therefore, III-V FETs may suffer from impact ionisation effect and surface related mechanisms (1, 2). The small-signal response of interface states at passivated III-V semiconductor surfaces has been measured over a wide frequency range from 1 Hz to microwave frequencies (3). Their influence on the performances of devices is very dependent on the technologies. Hot carriers mainly interact with deep levels or surface states located in the gate-drain region and the impact of such charge modification on device reliability is not so clear (4).
In this work, the effect of life-tests performed on P-HEMTs biased in impact ionisation regime with or without thermal stress has been analysed from the evolution of DC electrical characteristics and their temperature dependence. Drain current transients have also been measured to assess surface state effects after the ageing tests.

DEVICES UNDER TEST AND AGEING CONDITIONS

The P-HEMT technology under test is used for telecommunication applications from Ku to Ka-band as medium power amplification. The technological characterisation vehicle is based on an AlGaAs/InGaAs P-HEMT with a delta - doped layer and a single gate recess. The Ti/Al T-shaped gate is 0.25 µm long with a total width of (2 x 75) µm. The typical electrical performances are a drain saturation current Idss of 340mA/mm, a tranconductance of 500 mS/mm @Vds=2.5V, Vgs = 0 V, and an output power of 250mW/mm @1dB gain compression.
Different stress conditions are considered to separate degradation induced by thermal effects or by impact ionisation. Two sets of devices have sustained DC bias life-tests during 4000 hours in impact ionisation regime at Vds = 3.5 V and Ids = 35 mA, and at the maximum of the bell shape Ig-Vgs characteristics. In this technology, impact ionisation occurs for open channel bias conditions.
Devices of set 1 (DC1, DC2 and DC3) have been aged at room temperature corresponding to a channel temperature T_{ch1} of 90°C (5) and devices of set 2 (DC10, DC11 and DC12) at an ambient temperature of 140°C corresponding to a channel temperature T_{ch2} of 235°C (5). Four control devices, (T1, T2, T12 and T16), are used as reference parts to observe measurement errors or deviation. They are issued from a different wafer and present a lower threshold voltage V_T than aged devices, i. e. -0.80 V compared to -0.55 V, but a very similar transconductance value in the range of 85 mS.
Devices under test are issued from a reliability evaluation program that has lead to the qualification of this technology for space applications (5). Devices have been characterised during the ageing tests and the relative

parameter drifts remain clearly below the failure criteria that is a variation of ± 20% of the initial value for the saturation drain current, the transconductance and the threshold voltage. In particular, the transconductance evolution during the life-tests is in the range of –4% for devices of set 1 and –6% for devices of set 2.

ON – STATE BREAKDOWN VOLTAGE LOCI AT ROOM TEMPERATURE

The drain-source on-state breakdown voltage is measured by the gate current extraction technique (6). In this measurement, Ig is held constant at 0.13 mA/mm and Id is ramped from |Ig| to some reasonable value (7). The value of Ig is chosen to observe detailed mechanisms implied in the device breakdown (figures 1 and 2). The off-state breakdown voltage determined by the Id=|Ig| condition corresponds to the gate-drain diode breakdown. Therefore, the origin of the breakdown mechanism is first related to thermoionic field emission (TFE) and tunneling (probably assisted by interface traps) currents flowing through the reverse biased gate-drain diode. For all devices, it is verified that the higher the TFE-tunneling gate current, the lower the drain-source off-state breakdown voltage values.
When the drain current increases, the opening of the channel begins and as the gate current is maintained at a fixed value, the drain-source voltage first increases then decreases. The breakdown mechanism is correlated with the impact ionisation onset in the channel. Therefore, the shape of the BVon characteristics is very dependent on the relative importance of each mechanism i.e. TFE - tunneling gate currents and onset conditions of impact ionisation in the channel.
Control and aged devices present identical bell-shape curves Ig-Vgs at high Vds, except DC3 and DC12 that present a lower gate current contribution due to impact ionisation. For all aged devices in figures 1 and 2, the dispersion of the BVon locus shape is large while the BVon locus of control ones (T1, T2) presents a steep transition from the off-state to the on-state breakdown regime. As a consequence, control devices present a very similar value of the BVon voltage around 4.7V. The shape of the BVon locus of aged devices is either hyperbolic (as for DC3 and DC12) or soft (as for DC1 and DC11) resulting in a large range of BVoff values from 2.9V to 6.6V. As the impact ionisation is an intrinsic and specific mechanism related to a given technology, a similar contribution of this mechanism can be assumed in control devices. Therefore, a soft shape of the on-state breakdown locus corresponds to a higher leakage gate current while a hyperbolic shape is related to a lower leakage gate current.
As a dispersion of DC parameters is observed after the two life-tests and as the ageing temperature is different, the life-test ambient temperature is not considered as an accelerating factor of degradation.

EVOLUTION WITH TEMPERATURE OF GATE CURRENT AND BREAKDOWN VOLTAGE OF CONTROL AND AGED DEVICES

To complete the comparison on the effects of the two different life-tests, DC characteristics have been measured in the temperature range of 125K to 350K.
The figures 3 and 4 show the evolution with temperature of the reverse gate current, Ig-Vgs at high Vds.
It is composed of a hole component due to impact ionisation occurring in the channel and a leakage current component. The bell-shape of these characteristics reflects the preponderance of the impact ionisation contribution at high drain-source bias over the leakage gate current. Control devices present a slight increase of the leakage current component when increasing the temperature (figure 3). Compared to control devices, a drastic evolution of the gate current is observed for aged devices of each set between 280K to 350K (figure 4).

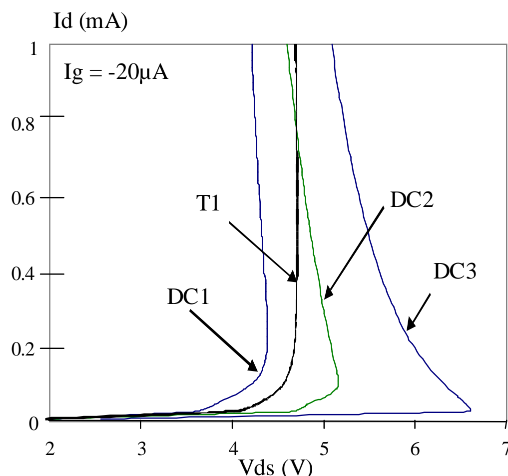

Figure 1 : On-state breakdown voltage locus for one control device (T1) and for set 1 (DC1, DC2 and DC3) at 300K

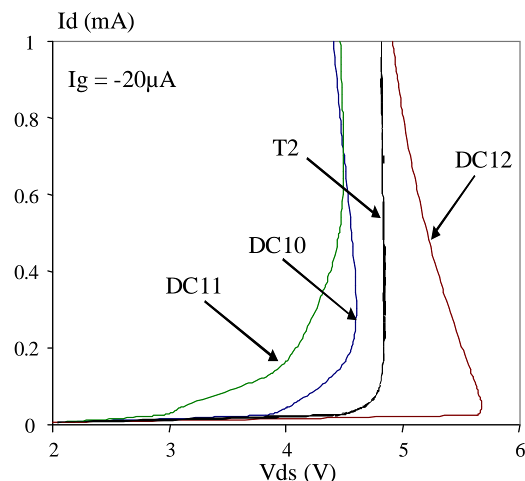

Figure 2 : On-state breakdown voltage locus for one control device (T2) and for set 2 (DC10, DC11 and DC12) at 300K

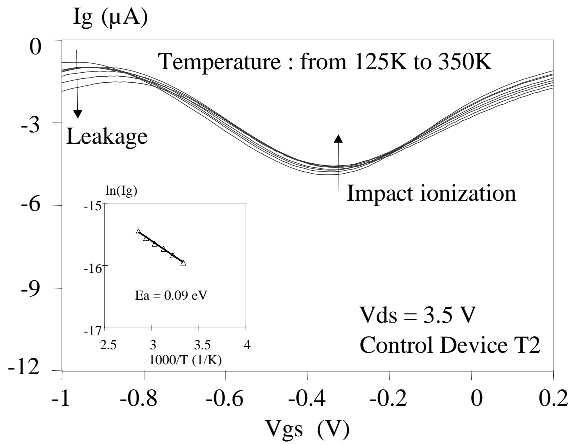

Figure 3 : Evolution of a bell-shape curve with the temperature from 125K to 350K at Vds = 3.5 V for a control device (T2)

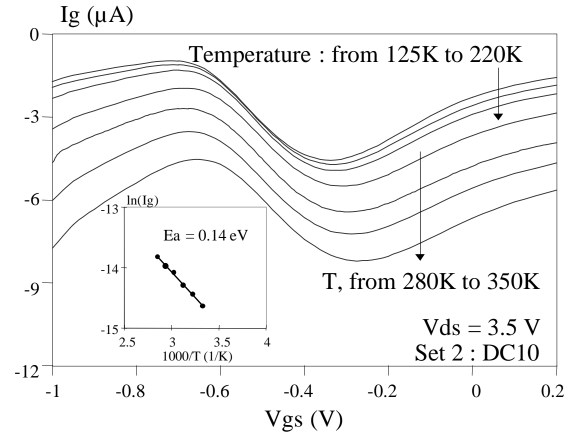

Figure 4 : Evolution of a bell-shape curve with the temperature from 125K to 350K at Vds = 3.5 V for one aged device of set 2 (DC10)

The bell-shape curve amplitude remains constant indicating that the impact ionisation effect is not dependent on temperature for this technology. Hence, the temperature evolution of the reverse gate current is attributed to a surface leakage current (8) controlled by surface states which kinetics has changed after ageing. The temperature variation of this surface current has been quantified through an activation energy that is 0.09 eV for control devices and 0.14 eV for aged devices in the 280 K-350K temperature range.
The evolution with temperature of the on-state breakdown voltage BVon measured with an injected gate current of 1mA/mm is plotted in figure 5 for one aged device of set 2. After the two types of life-tests, the on-state breakdown voltage presents a similar and weak decrease with increasing the temperature from 125K to 360K.
This result is consistent with a positive temperature coefficient of the electron ionisation rate in InGaAs material (1). For open-channel bias conditions, the breakdown voltage locus reflects the impact ionisation influence occurring in the channel. Therefore, the weak evolution of this locus is consistent with the weak temperature evolution of the bell-shape curves.

DRAIN CURRENT TRANSIENT AFTER AGEING

Drain current transient measurements have been performed in the saturation regime at V_{DS} = 3 V. As the contribution of, either the surface and access regions or deep layers and interfaces, are analysed, different voltage pulses are applied to the gate. For aged devices, the gate pulse is drifted towards negative values to reach a similar value of the final drain current at equilibrium for control and aged devices and to take into account the difference in V_T.

When the gate voltage is pulsed to analyse the deep region of the devices through the modulation of the space charge layer thickness, the drain current transient amplitude appears as a very weak capture component in all control and aged devices. Hence, it is assessed that there are no active traps in the deep layers of the devices. On the contrary, when the gate voltage is pulsed to track traps located in the upper zone of the active layer, an electron emission component is observed for both control and aged devices (figure 6).
The transient amplitude is at least twice higher for aged devices than for control ones while the transient time constant is in the range of several hundred milliseconds for all devices. This reveals that surface traps are responsible for the emission process in control and aged devices. The increase of the emission transient amplitude suggests either a higher active trap density in aged devices than in control ones or the contribution of additional traps in aged devices.

CONCLUSIONS

All control devices present an identical and steep shape of the on-state breakdown locus while all aged devices present a large dispersion of this characteristic. It seems that some slight modification of the surface properties and/or micro-defects located in the gate-drain region affect the on-state breakdown voltage loci measured with a gate current of 0.13mA/mm.
The breakdown voltage measured for open-channel bias conditions (Ig = 1 mA/mm), presents a weak evolution with the temperature that is consistent with the weak temperature dependence of the impact ionisation contribution to the reverse gate current at high drain-source voltage.
After the two life-tests, the temperature evolution of the surface leakage contribution to the reverse gate current has increased.

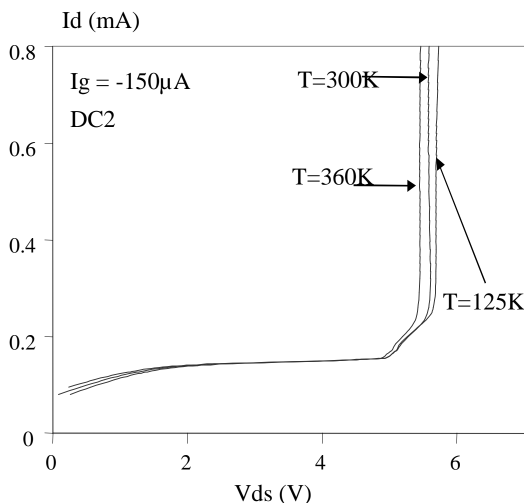

Figure 5 : Evolution of the breakdown voltage locus with the temperature from 125K to 360K, measured at Ig=1mA/mm for one aged device of set 2 (DC2)

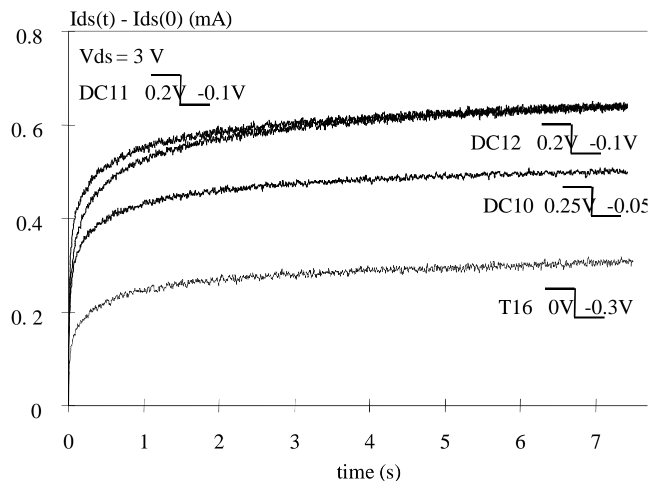

Figure 6 : Drain current transient measured at 300K for a control device (T16) and aged devices of set 2 (DC10, DC11, DC12) showing an electron emission contribution

Isothermal transients of the drain current measured in response to a gate pulse have demonstrated that the technology is not affected by deep levels located in the active layers.
This result is confirmed after the two life-tests. Only an increase of the electron emission contribution from surface traps is identified after ageing.
Electron conduction might enhance during ageing at the surface and in access regions. The contribution of additional surface traps or surface micro-defects are assumed to explain the evolution observed in aged devices (8).
Therefore, the two stress tests performed in impact ionisation regime have demonstrated the influence of this mechanism. Also, as the ageing temperature is different for the two life-tests, this thermal stress is not an accelerating factor of electrical parameter degradation. Slight modification of the surface properties affects the on-state breakdown voltage locus and the reverse gate current without affecting the reliability of this technology.

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