7 V_{PP} Modulator-Driver for 40 Gbit/s Optical Communications

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The high frequency, high power performance of a modulator driver based on a dual input travelling wave amplifier (combiner) is reported. Measured output terminal voltages greater than 7 V_{pp} have been achieved. Although the results are intermediate in some respect, the simulated as well as the measured data indicate that the driver circuit is suitable for a bit rate of 40 Gbit/s. Simulation results obtained for an improved circuit which contains an active divider also indicate even better performance at operation with single input voltage.

INTRODUCTION

To operate Mach-Zehnder modulators, output voltages higher than 6 V_{pp} are necessary. Si and SiGe bipolar technologies have reached 3.5 V at 23 Gbit/s and 1.25 V at 40 Gbit/s (1,2). Based on GaAs P-HEMT technology higher voltages have been reported in (3,4). However, this state-of-the art is still not sufficient for driving a Mach-Zehnder modulator. Our goal was to develop a modulator driver capable to generate the required minimum output voltage of 6 V_{pp} at a data rate of 40 Gbit/s. We briefly explain the design and the main technological aspects of the modulator driver, the original simulation results, and electrical measurements. Resimulation results and very promising simulation results of a new circuit that contains an active divider are also included .

DESIGN AND REALISATION OF THE MODULATOR DRIVER CIRCUIT

The modulator driver is fully monolithic and has been fabricated using the OMMIC D01PH process, i.e. a pseudomorphic AlGaAs/InGaAs HEMT technology. The mushroom gates have a length of 0.13 µm. The process exhibits excellent electrical characteristics such as a transit frequency of 105 GHz and a gate drain breakdown voltage of -11 V. The DFET characteristic allows operation without a gate bias voltage. A drain bias voltage of 6 V is applied through an external bias tee. This voltage is also used on chip for the drainline termination resistor, avoiding the DC losses that would result from a simple termination to ground. Resistors were realised using a thin film n+ active layer with a sheet resistance of 100 $\Omega_{\square}$. Capacitors with a 150nm SiN dielectric were employed to supress noise on the two required DC voltages,i. e. the drain line termination voltage mentioned above and a cascode reference voltage of 3 V. The buffer capacitors were integrated into the grounded areas of the coplanar structures.

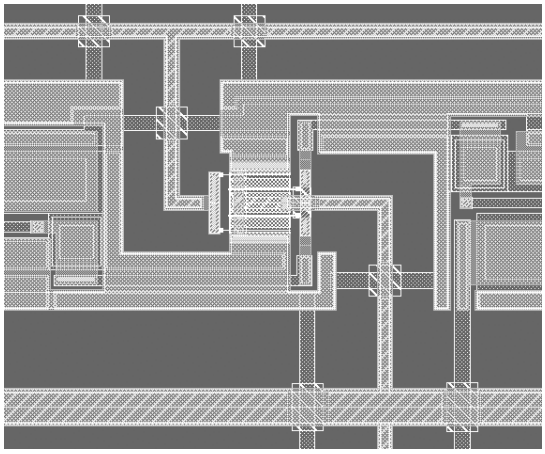

Fig. 1: Layout Detail of Combiner with common gate line (upper part) and common drain line (lower part)

The design concept of the modulator driver is based on two identical travelling wave amplifiers sharing a common drain line on which their output power is combined. The additional capacitive loading of this common drain line causes a lower phase velocity and thus enables a design with similar length of the gate and the drain line between two stages. Therefore, a simple layout without meander lines was possible. Each half of the combiner consists of 5 stages in coplanar wave guide technology. A single stage contains a two finger HEMT cascode consisting of two FETs.

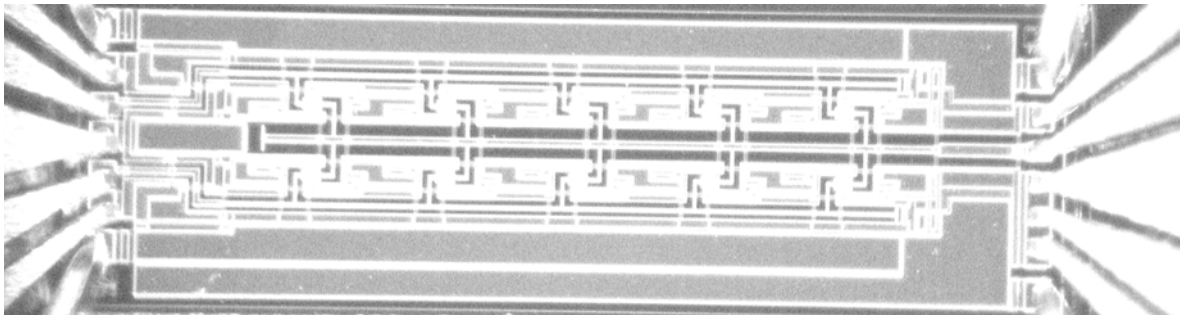

Fig. 2: Chip micrograph of the modulator driver under test

Each transistor of the cascode has a gate width of 30µm The cascode is designed as a single cell in order to save space and reduce parasitics.The combiner circuit was fabricated in a multi-user run. Therefore, the chip size and orientation had to comply with a general pattern, a set of common rules for all users. On the other hand, only one gate orientation for all transistors on the wafer is possible because of the electron beam writing technique and the gate fabrication process. As a result of these two constraints, the gates of the cascode cells had to be parallel to the common gate and drain line, as depicted in Fig. 1. A major disadvantage of this design is that bended lines at the gate and drain contact of each cascode cell became necessary after circuit optimisation. With gate orientation perpendicular to the common gate and drain lines, these interconnections could be realised as short straight lines.

SIMULATION AND MEASUREMENT RESULTS

Small signal measurements were carried out to determine S-parameters and group delay. Fig. 2 shows a chip micrograph of the combiner under test, with a 100 µm P-G-S-G-S-G-P probe on each side. On the left hand side, the two input signals are fed into the modulator driver, while the right probe contacts the output from the common drain line. Fig. 3 shows the simulated, measured, and resimulated absolute value of S_{21} and the group delay, the latter being calculated from the phase of S_{21} by approximation of its differential quotient by the difference quotient of two neighbouring measurement points. This method would be numerically critical for small distances between the measured points, but because only a small number of values were available anyway, the result turned out to be a reasonable replacement for direct measurement of the group delay that was not available. In the resimulation the best and very convincing fit could be obtained for all four S-parameters and the phase delay by incorporating an additional bend with a parasitic capacitance of 25 fF at the input and output of each stage into the simulation model. This bend correlates the real layout of the circuit shown in Fig. 1. In respect of redesign, the results clearly indicate, that these bends have to be avoided because they reduce the gain at higher frequencies remarkably. For the layout of the improved circuit with the active divider, it will be possible to avoid the bends by using a non-standard chip size.

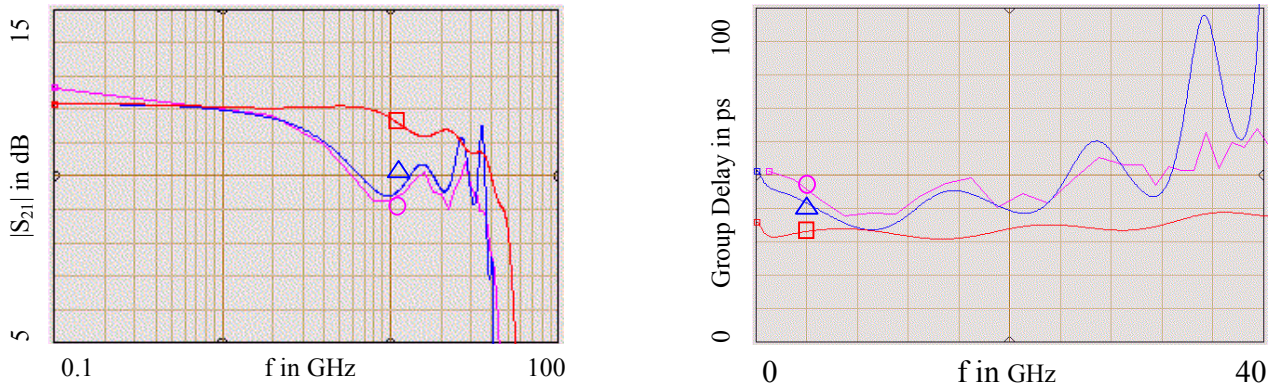

Fig. 3: Comparison of simulated (□), measured (○) and re-simulated (Δ) data for the magnitude of S_{21} (left) and group delay (right)

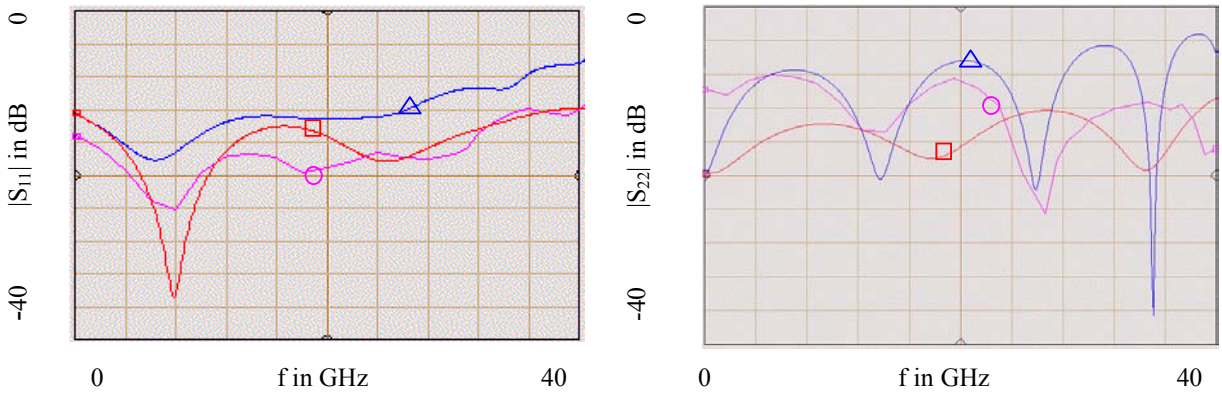

Fig. 4: Comparison of simulated (□), measured (○) and re-simulated (Δ) data for the magnitude of S_{11} (left) and S_{22} (right)

Fig. 4 shows the magnitude of S_{11} and S_{22}, again with a comparison of the simulated, measured and resimulated curves. In general, the very small magnitudes differ only slightly, and the frequency dependency is modelled quite well in the resimulation. It should be emphasized that measurement and simulation agree very well, giving good prospect to a successful redesign.

LARGE SIGNAL MEASUREMENT

Because the circuit is designed to drive a Mach-Zehnder modulator, it is desirable to measure its large signal output with a PRBS input signal of appropriate voltage level and to generate an eye pattern. But a 40 Gbit/s PRBS generator was not yet available, so large signal 20 GHz sine wave measurements were carried out. All losses due to the measurement setup were measured at 20 GHz and were subsequently compensated either by applying additional power at the input or by setting the attenuation parameter of the oscilloscope. Moreover, only the 10 MHz reference could be used as trigger signal for the scope, requiring averaging to get a clear signal. A passive power divider was employed to deliver two equal input signals. The term input voltage is always used for the voltage applied to the chip. Fig. 5 shows the output waveforms of the large signal measurement: an input voltage of 1 V_{pp} leads to an output voltage of 6 V_{pp}. Increasing the input voltage to the limit defined by the Schottky diodes, i.e. approximately 1.5 V_{pp}, results in a maximum output voltage well above 7 V_{pp}.

ACTIVE DIVIDER

The need of two identical input signals is a major drawback of the combiner concept. The required passive divider consumes half of the input power. The use of an active divider based on two TWAs but sharing a common gate line as proposed in (5) approximately doubles the chip area and requires broadband DC decoupling. Our new approach is to use a source follower based active divider circuit. Similar to the cascode cells of the TWA, transistor pairs, i.e. the follower transistor itself and the active current source, can be integrated into a single cell which fits into the coplanar environment.

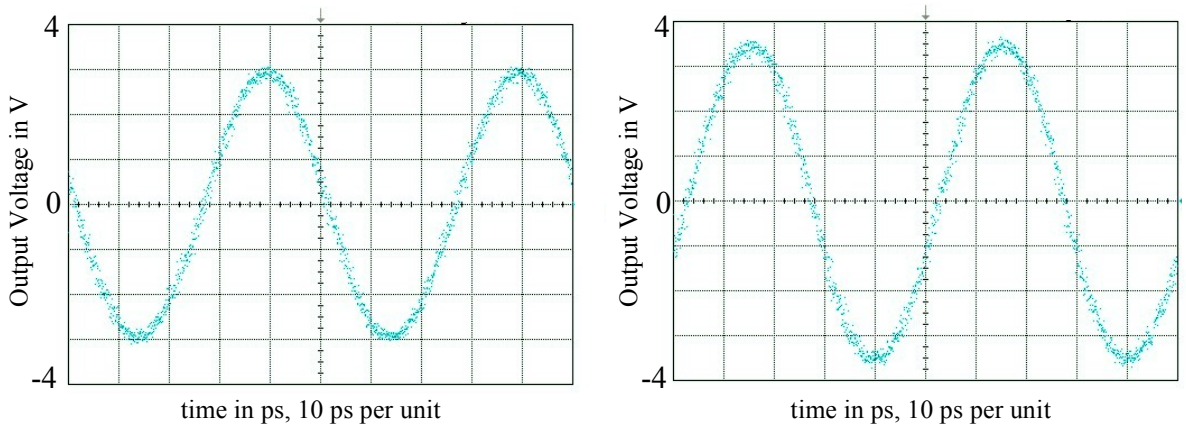

Fig. 5: Output voltage of combiner for input voltages of 1 V_{PP} (left) and 1.5 V_{PP} (right)

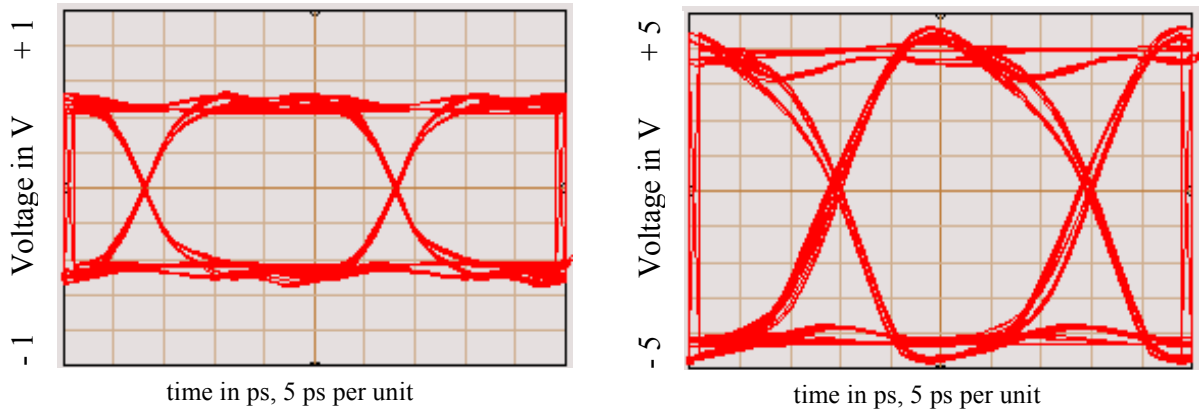

Fig. 6: Simulated eye diagrams at 1.5 V_{PP} input voltage for internal active divider (left) and modulator driver (right)

Thus, the active divider can be implemented with almost no additional chip area needs. Although the source follower also introduces losses, the higher losses of off-chip components and the DC decoupling problem are avoided. Another advantage of the source follower based active divider is its capability to operate with higher input voltages than the cascode cell. Because the HEMT of the first stage has no grounded source contact, the Schottky diode is no longer a limiting factor for the input voltage. The gate-source voltage (identical with the diode voltage) is kept small by the source follower principle. Output voltages close to 8 V can be produced at input voltage levels of 1.5 V_{PP} according to simulation results presented. The complete chip, i.e. from single input port to single output port, has a small signal gain of 16 dB. Fig. 6 shows the large signal waveform at one of the active divider outputs (an internal node) and the output waveform of the whole chip, both at 1.5 V_{PP} input voltage. The depicted output signal of the active divider is identical with the combiner input signal and therefore restrictions from the Schottky diodes apply, but Fig. 6 shows that this internal voltage is not critical. Further simulations indicate that input voltages of 2 V_{pp} could be used, leading to ouput voltages as high as 9 V_{pp}.

CONCLUSION

Output voltages above 7 V_{pp} at 40 Gbit/s could be experimentally obtained by a combiner concept based on two TWAs sharing a common drain line. The integration of an active divider based on source follower structures has proved to be very promising in simulations.

ACKNOWLEDGEMENT

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