Development of Complete On-Wafer Cryogenic Characterization: S-parameter, Noise-Parameter and Load-Pull

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ABSTRACT

In this paper, we review recent progress at Georgia Tech's Microwave Application Group towards the development of complete cryogenic analysis techniques. This includes development of on-wafer cryogenic (15K to 300K) S-parameter, Noise Parameter, and Load-Pull measurement techniques. These data are then used for detailed analysis of various device technologies for development of improved small and large signal models. Applications include optimization of transistor device technology for reduced temperature operation, development of cryogenic low-noise amplifiers, and reduced temperature power amplifier operation.

INTRODUCTION

Results of cryogenic on-wafer noise-parameter measurements are presented for the first time on $In_{0.8}Ga_{0.2}As$ channel High Electron Mobility Transistors (HEMTs) grown on InP. The Noise resistance (R_n) and optimum reflection coefficient for minimum noise (Γ_{opt}) are obtained applying Modified-Lane's algorithm directly to the experimental data. A procedure is developed to extract the minimum noise temperature, T_{min} from the measured R_n, Γ_{opt} and utilizing the Pospieszalski Noise model. Good agreement between the measured and extracted values of T_{min} is obtained at room temperature. At cryogenic temperatures the extracted T_{min} shows excellent agreement with that obtained on a low-noise amplifier built using this HEMT.

On-wafer load-pull measurements at cryogenic temperatures are made for the first time on FET power amplifier structures to demonstrate the improved performance when operated at reduced temperatures. Measurements from 300K to 17K demonstrate improvements in both efficiency (40-80 %) and output power (1.0-2.7 dB). These results demonstrate that advanced device technologies that are optimized for cooled operation may provide significantly enhanced system performance and reliability with a minimal increase in prime power.

EXPERIMENT AND RESULTS

In this section we investigate the accuracy of the determination of T_{min} at cryogenic temperatures. We utilize the values of R_n, Γ_{opt} and the small-signal model (derived from on-wafer S-parameters) in conjunction with the Pospieszalski model [1] to determine T_{min}. In Fig 1 we show the noise conductance at the two temperatures of measurement from 10-26 GHz. The magnitude and phase of Γ_{opt} are shown in Fig 2. The measurements are done at a V_{ds} of 0.75V and an I_{ds} of about 7mA, which was found to be the optimal bias for low noise.

The flowchart in Fig 3 describes the procedure adopted for the determination of the T_{min}. First, an accurate small-signal model is obtained from the measured S-parameter data of the device based on the method described by Shirakawa et.al. [2]. The measured noise parameters F'_{min}, R_n, Γ_{opt} are converted to T'_{min}, g_n, Z_{opt}. The drain equivalent temperature, T_d is calculated from the following equation [1].

$$g_n = \left(\frac{f}{f_t}\right)^2 \frac{g_{ds}T_d}{T_0} \qquad (1)$$

where f is the frequency of measurement, f_t is the cut-off frequency obtained from the S-parameter data, g_{ds} is the drain-source conductance and T_0=290K. At room temperature T_d is obtained to be 9,000 K ± 750 K while at 27 K T_d is 3,750K ± 750K. Finally, T_{min} is calculated from the following relation [1],

$$T_{min} = 2\frac{f}{ft}\sqrt{g_{ds}T_d r_{gs}T_g} \qquad \mathbf{(2)}$$

where r_{gs} is the gate-source resistance and T_g is the gate equivalent temperature which is assumed to be the ambient temperature.

In Fig. 4 we show the T_{min} extracted at 290 K and 27 K. It indicates that T_{min} shows nearly a ten fold decrease by cryogenic operation. Hybrid low-noise amplifiers built out of these devices showed a T_{min} of 10 K at a physical temperature of 16 K validating the results presented here.

We have also adapted the on-wafer cryogenic measurement technique[3] to an ATN load-pull system. This new system allows temperature (300-20 K) and bias dependent power measurements for complete load-pull analysis. The measurement reference planes are established directly at the device under test (DUT). This condition is achieved through a set of user calibrations: Short-Open-Load (SOL), Power Transfer, 2 port S-parameter and Thru delay. The calibration was validated by measuring a 50-ohm Thru. Additionally, for measurement accuracy, the calibrations are performed at each temperature of interest: 300K, 200K and 20K[3]. This measurement approach provides the foundation for developing microwave large signal models over a wide temperature range and represents a significant contribution to recently reported approaches for temperature dependent large signal models [4,5].

In figures 5 and 6, we show the effect of temperature (290-17 K) on Contour Circles of Constant Efficiency and Output Power for the GaAs MESFET (W=300µm) sample. The input impedance was set for maximum small signal gain and the input power was set at the 1dB compression point. The decrease in temperature results in larger contour circles for that same condition of constant Efficiency and Output Power at room temperature. An improvement in the Efficiency and the Output Power with the physical decrease in the temperature of the device will result independently of the termination due to the fact that the same termination is now on a different contour circle with a higher Efficiency or Output Power. Figure 4 shows that result into 50-ohm termination for that same device.

In Figure 7, we show the effect of temperature (300-17 K) on power measurements into 50-ohm termination for GaAs MESFET devices. A large signal model for the GaAs MESFET (W=200µm) was implemented in MDS for both 300K and 20K operation.

CONCLUSION

In summary, we have developed both cryogenic on-wafer load-pull and noise parameter measurement systems. These systems have been employed to study the effect of temperature on several amplifier device technologies: GaAs MESFET, GaAs PHEMT and InP HEMT. For noise parameter operation, we develop a procedure using the Lane algorithm and the Pospiesalski noise model to determine T_{min} from the measured R_n and Γ_{opt} . We demonstrate significant improvement in reduced temperature large signal operation of a GaAs MESFET and develop an initial temperature dependent large signal model .

ACKNOWLEDGEMENTS

This work was supported in part by NSF CAREER Award ECS-9623964 and NASA/JPL/ The authors would also like to acknowledge ATN Microwave, Cascade Microtech, Hewlett-Packard, Raytheon, TriQuint Semiconductor, and TRW.

REFERENCES

[1] M. W. Pospieszalski, “Modeling of Noise parameters of MESFETs and MODFETs and their Frequency and temperature dependence”, IEEE Trans. On Microwave Theory and Techniques, 37, 1340 (1989).

[2] K. Shirakawa, H. Oikawa, T. Shimura, Y. Kawasaki, Y. Ohashi, T. Saito, Y. Daido, "An approach to determining an equivalent circuit for HEMTs", IEEE Trans. On Microwave Theory and Techniques, 43,499 (1995)

[3] J. Laskar, M. Feng "An On-Wafer Cryogenic Microwave Probing System for Advanced Transistor and Superconductor Applications" Microwave Journal Vol. 36 pp. 104-114, February 1993.

[4] J. Laskar, J. Bautista, M. Nishimoto, M. Hamai, and R. Lai, "Development of Accurate On-Wafer, Cryogenic Characterization Techniques," IEEE Transactions on Microwave Theory and Techniques. Vol. 44, pp. 1178-1183, July 1996.

[5] S. Munoz and J. Gallego, ”Modeling the Bias and Temperature Dependence of a C-Class MESFET Amplifier” IEEE Transaction On Microwave Theory And Techniques. Vol. 25 pp. 527-533 April 1997.

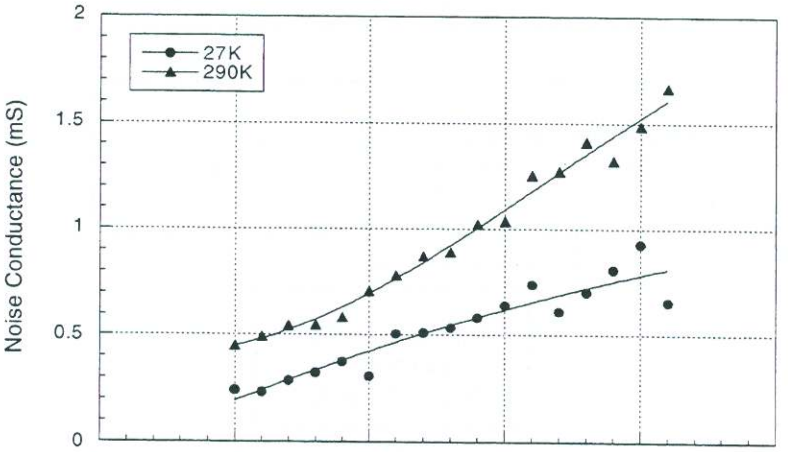

Fig1 Noise conductance of 0.1x40μm InGaAs/InP HEMT at 27 K and 290 K

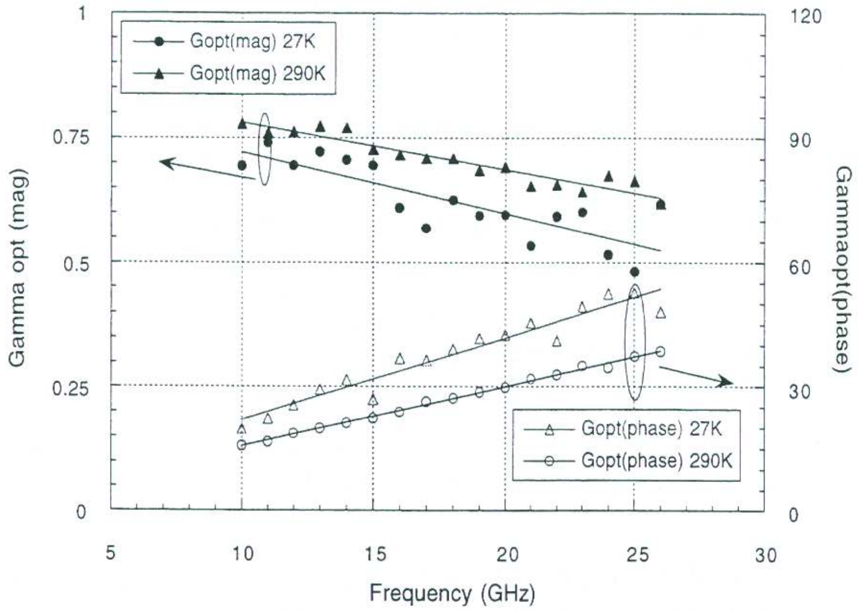

Fig 2 Magnitude and phase of the optimum reflection coefficient for minimum noise InP HEMT at 27 K and 290 K

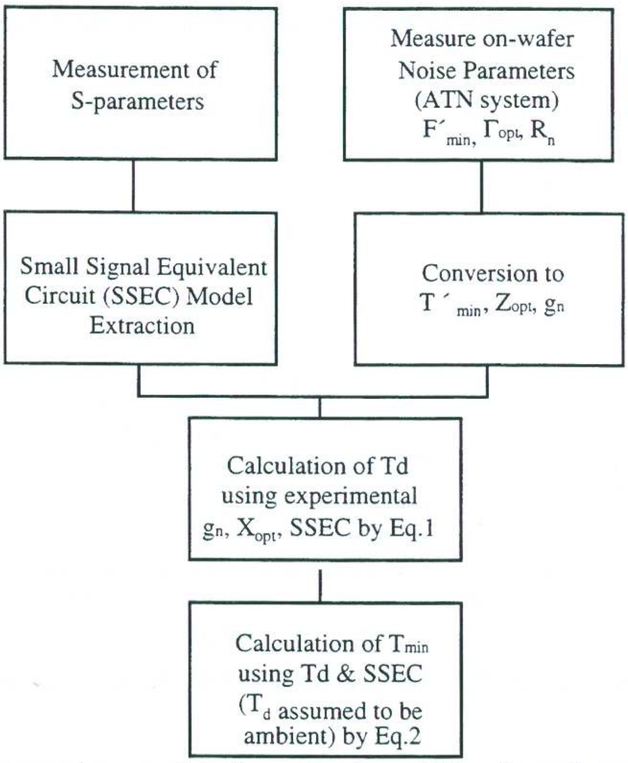

Fig 3 Flowchart of the procedure used in the extraction of T_{min} from the measured data

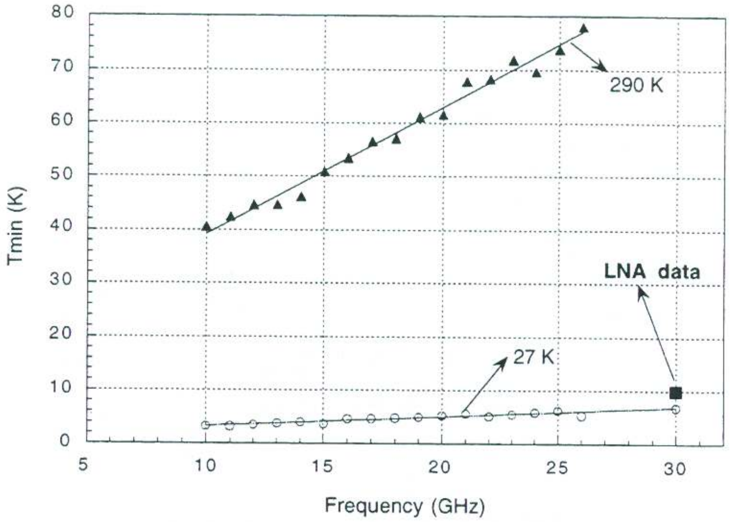

Fig4 T_{min} for 27K(O) and 290K (▲) on the discrete HEMT and Noise Figure measured on a hybrid Low Noise Amplifier (■).

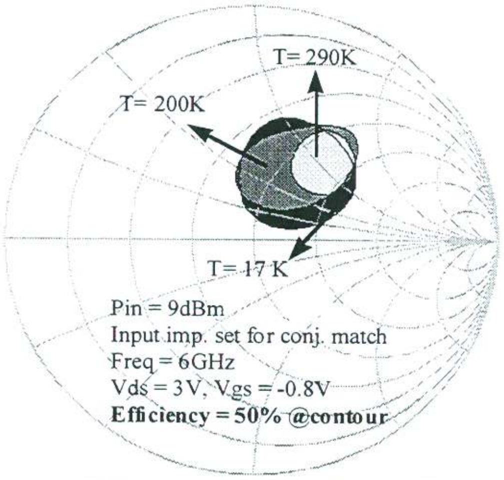

Figure 5: GaAs MESFET constant Efficiency Contour Circles for three different temperatures

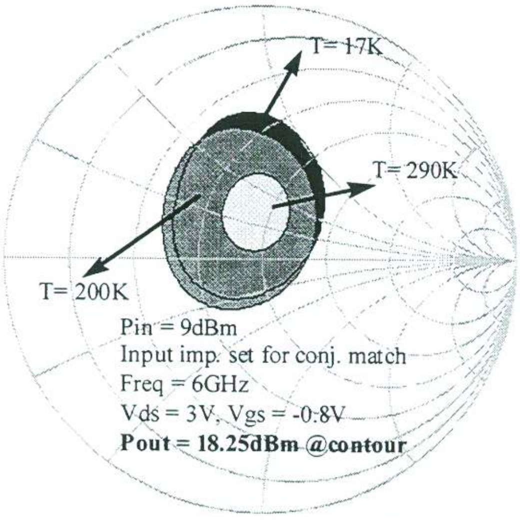

Figure 6: GaAs MESFET Constant Output Power Contour Circles for three different temperatures

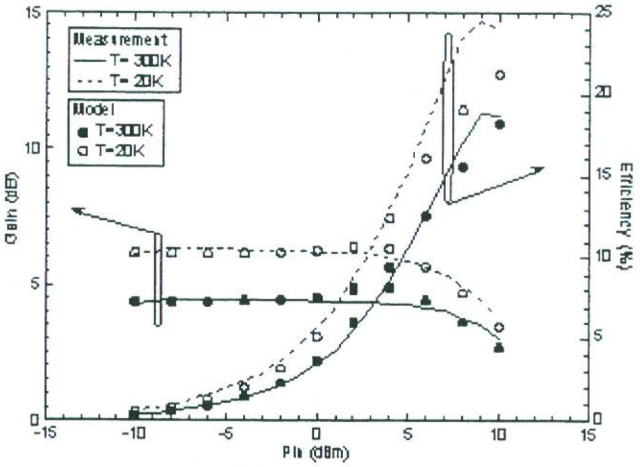

Figure 7: GaAs MESFET 10GHz measured, modeled Gain and Efficiency versus input power levels at 300K and 20K into 50 ohm termination at Vds=2V, Vgs=-0.8V