Dynamic, self consistent electro-thermal simulation of power microwave devices including the effect of surface metallizations

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We present an efficient simulation technique to account for the thermal spreading effects of surface metallizations in the self-consistent dynamic electro-thermal analysis of power microwave devices. Electro-thermal self-consistency is achieved by solving the coupled nonlinear system made of a temperature dependent device electrical model, and of an approximate description of the device thermal behavior through a thermal impedance matrix. The numerical solution is pursued in the frequency domain by the Harmonic Balance technique. The approach is applied to the thermal stability analysis of power AlGaAs/GaAs HBTs and the results show that metallizations have a significant impact on the occurrence of the device thermal collapse.

INTRODUCTION

Electro-thermal modeling of III-V based power devices is a critical task for reliable transistor and circuit design. In fact, the high power densities involved, coupled with the low thermal conductivity of the GaAs or InP substrates, can cause significant self-heating, whose effects lead either to catastrophic failure or thermal instability, or to device performance degradation. In particular, high power multifinger heterojunction bipolar transistors (HBTs) are susceptible to thermal instabilities leading to the occurrence of the so called gain collapse. This phenomenon occurs when one emitter heats up more than the others and draws all the device current turning off the other emitter fingers, thus causing a remarkable drop of gain [1]. Even in thermally stable devices, however, high junction temperatures lower the DC gain and the overall microwave performances, besides reducing the device reliability. To overcome these challenges various thermal management techniques can be adopted, such as wafer thinning, top-side heat removal through thick metallizations, or thermal shunt [2]. Indeed, reliable and efficient electro-thermal simulation tools able to include all of these issues are needed to drive the designer towards more effective layouts to obtain significant improvements of the device performance.
In a previous work we have proposed an original approach to HBT simulation, exploiting a self-consistent dynamic electrothermal power device analysis [3]. The device electrical behavior is simulated through a circuit-oriented large-signal model with temperature-dependent parameters, while the thermal device behaviour is evaluated through a quasi-analytic 3D technique based on [4], allowing for a closed form estimation of the frequency-dependent, dynamic thermal impedance. This hybrid approach is numerically efficient since the thermal impedance matrix, depending on the layout characteristics only, can be computed only once before carrying out the electro-thermal simulation. In this work we present a further development of our thermal analysis tool allowing to account for surface metallizations, thermal shunts, and via holes. The technique we adopt preserves the numerical efficiency of the overall electro-thermal CAD tool described in [3], since surface metallizations are conveniently described through an approximate thermal conductance matrix, depending on the metal thermal conductivity, thickness and layout [5].
In the following we briefly describe our approach and report some electro-thermal simulation results of power GaAs/AlGaAs HBTs [3], stressing the relevance of surface metallizations induced heat removal onto the device thermal stability.

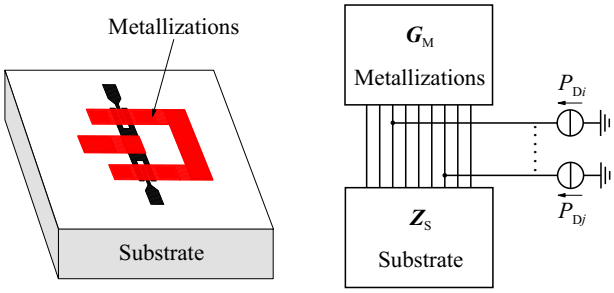

Figure 1: Layout of the 2 finger HBT (left) and equivalent thermal circuit representation (right).

THE THERMAL MODELING APPROACH

In a typical power transistor layout, metallic layers are deposited on the top surface and likely connected to the mounting (heat sink) through via holes. As an example, Fig. 1 (left) reports a layout of the 2-finger power HBT we have simulated. The thermal spreading effects due to the high thermal-conductivity metallic layers can be included in the model by means of the technique proposed in [5]: as a first step, surface metallizations are discretized into small areas (patches), thus enabling to define the thermal conductance matrix $\mathbf{G}_m$ of the metallic layers, which depends on the metal thermal properties and thickness; notice that, as a simplifying assumption, the dynamic response of the metal layers is supposed to be much faster than the substrate, and is

therefore considered as instantaneous at this stage of the thermal model development: this means that $\mathbf{G}_{\mathrm{m}}$ is real and frequency-independent. It is also worth pointing out that multi-layer metallizations (this is, for example, the case if air-bridges are exploited either for electrical connectivity or thermal shunt purposes) can also be described by this approach, provided that the layers, each described by a thermal conductance matrix, are thermally connected through proper ports.
Secondly, the device substrate is described by means of a (substrate) thermal impedance matrix $\mathbf{Z}_{\mathrm{s}}$, whose input-output ports correspond to the patches defined by the surface metallization's discretization (this means that the two square matrices have the same dimension). From a modelling standpoint, the frequency-dependent substrate thermal impedance matrix is efficiently evaluated according to the method proposed in [4], i.e. by approximating each thermal source (patch) through a superposition of spherical sources complemented by the application of the images method in order to recover the substrate thermal boundary conditions, see e.g. [6]. As far as via holes are concerned, they can be modeled through additional thermal conductances connecting the metallizations to the heat sink. This equivalent circuit interpretation of the heat flows in the device structure is represented in the right part of Fig. 1, where the current generators represent power sources due to dissipation in the active device regions: in an HBT, these are connected to the patches pertaining to the device emitters.
By solving the circuit, the resulting equivalent thermal impedance matrix of the device, including the effect of metallizations, can be calculated as:

$$\mathbf{Z}_{\mathrm{T}} = \mathbf{Z}_{\mathrm{s}} \cdot [\mathbf{G}_{\mathrm{m}} \cdot \mathbf{Z}_{\mathrm{s}} + \mathbf{I}]^{-1} \qquad (1)$$

where $\mathbf{I}$ denotes the identity matrix, and the (i, j) element of $\mathbf{Z}_{\mathrm{T}}$ represents the average temperature increase ΔT_i in patch i due to the thermal power $P_{\mathrm{D}j}$ injected in patch j: $(\mathbf{Z}_{\mathrm{T}})_{i,j} = \Delta T_i / P_{\mathrm{D}j}$.
To perform the electro-thermal simulation, $\mathbf{Z}_{\mathrm{T}}$ needs to be reduced, since we are interested in computing the temperature values only in the nodes corresponding to the thermal sources, i.e. the emitter fingers. By properly averaging the temperature on the emitter patches, one can extract such a reduced device thermal impedance matrix $\mathbf{Z}$ (see Fig. 2), whose dimension, for an HBT, equals the number of emitter finger patches. Notice that if any emitter is further divided into smaller patches, a distributed description becomes available for the temperature profile along the emitter finger itself, thus making possible to include, e.g., emitter crowding effects in the model.

ELECTRO-THERMAL ANALYSIS

The device thermal model described by the reduced thermal impedance matrix $\mathbf{Z}$ is then coupled to the electrical temperature-dependent model to obtain an equivalent self-consistent electro-thermal circuit representing the multifinger device. For the case of HBTs, the model is, in DC operation, a standard

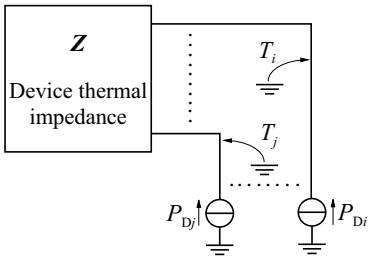

Figure 2: Reduced device thermal circuit.

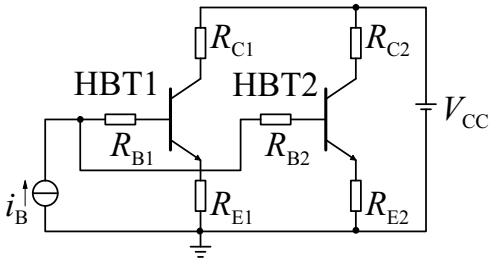

Figure 3: Electrical circuit for a two-finger HBT.

Gummel-Poon model for the forward operation of each device finger:

$$i_{\mathrm{B}k} = \frac{I_{\mathrm{C0}}}{\beta_{\mathrm{F}k}} \exp\left[-\frac{E_{\mathrm{g}}(T_k)}{k_{\mathrm{B}} T_k}\right] \left[\exp\left(\frac{v_{\mathrm{BE}k}}{\eta_{\mathrm{F}} k_{\mathrm{B}} T_k}\right) - 1\right] + I_{\mathrm{B0}} \left[\exp\left(\frac{v_{\mathrm{BE}k}}{\eta_{\mathrm{E}} k_{\mathrm{B}} T_k}\right) - 1\right] \qquad (2)$$

where k is the finger index, E_{g} is the base material energy gap, η_{F} the ideality factor of the base-emitter junction, $I_{\mathrm{C0s}} = I_{\mathrm{C0}} \exp[-E_{\mathrm{g}}(T_k)/(k_{\mathrm{B}}\, T_k)]$ is the base-emitter reverse saturation current, η_{E} the ideality factor for the parasitic base current, I_{B0} represents such parasitic current in reverse saturation and $\beta_{\mathrm{F}k}(T_k) = \beta_0 \exp[\Delta E_{\mathrm{v}}/(k_{\mathrm{B}} T_k)]$ is the finger gain excluding parasitic base current. ΔE_{v} is the valence band discontinuity of the base-emitter junction. For time-dependent analysis, this DC model is complemented by a dynamic part represented through (generally) nonlinear capacitances and a time delay between emitter and collector currents [3].
The electrical and thermal device models are finally combined in order to derive a set of nonlinear differential equations describing the multifinger device layout. For the sake of simplicity, Fig. 3 represents the equivalent electro-thermal circuit for the two-finger case only. The resulting dynamic system is solved directly in the frequency domain by means of the Harmonic Balance (HB) method [7, 3], thereby obtaining a self-consistent electro-thermal working point.

RESULTS

In order to apply the electro-thermal analysis methodology with the aim of investigating the effects of surface metallizations on the onset of the current collapse, we have simulated the two-finger HBT layout shown in the left part of Fig. 1: the two fingers are

identical and simmetrically placed so that the device should not exhibit gain collapse. Due to small mismatch of the two emitters characteristics, gain collapse can actually occur. From a simulation standpoint the collapse is introduced into the model by means of a small difference in the emitter resistance of the biasing network.

The fabrication process is characterized by a substrate thickness of 120 μm and a metal thickness of 0.6 μm for the emitter and base, and 3.3 μm for the collector and the other cold metallizations. The electro-thermal device simulation was performed by considering a single, averaged temperature for each of the two emitters (this means that the reduced thermal impedance matrix has dimension 2×2), though for the thermal impedance evaluation the emitter fingers, as well as the other metallizations, were discretized into several patches. Fig. 4 shows the section of the surface temperature across the emitter fingers calculated (in static conditions) with and without the effect of surface metallizations, and for a dissipated power of 100 mW for each finger. Due to heath spreading by metal layers, the simulation including the metallizations exhibits a noticeable (around 28 K) reduction of the peak temperature on the emitters: this is expected to significantly improve the device thermal stability.

In order to highlight the importance of thermal spreading effects due to metal layers, different thicknesses for the emitter and base metal layers have been also considered. The corresponding reduced thermal impedance matrix elements are reported in Tab. 1; we considered also a reduced thickness for the substrate in order to investigate whether this could further ameliorate device stability.

Simulated structure	$Z_{11} = Z_{22}$	$Z_{12} = Z_{21}$
No met., 120 μm	1642 K/W	55 K/W
0.6 μm E/B met., 120 μm	1435 K/W	54 K/W
2 μm E/B met., 120 μm	1247 K/W	55 K/W
0.6 μm E/B met., 60 μm	1411 K/W	34 K/W

Table 1: Static components of the reduced thermal impedance matrix for the different simulated structures.

We have first performed static simulations, in order to evaluate the output characteristics of the HBT biased with a fixed total base current I_{B} and a collector bias V_{CC} fed through an emitter and collector resistance (see Fig. 3). The DC output characteristics (i.e., the total collector current) computed without the metallizations are shown in Fig. 5 and can be compared to the ones evaluated in the case where the metal layers have the thickness as described in the nominal process (see Fig. 6). As expected the gain collapse occurs for higher collector bias in the second case: for the 400 μA characteristic, the onset of collapse is moved from $V_{\mathrm{CC}} = 7.5$ V to $V_{\mathrm{CC}} = 9$ V.

As a further investigation we consider a possible process where the base and emitter metal thickness is increased to 2 μm (see Tab. 1 for the thermal impedance values). The three cases are compared in Fig. 7 (symbols), where $I_{\mathrm{B}} = 400$ μA, showing that gain collapse is shifted towards even higher collector bias. The full line in Fig. 7 refers to dynamic simulations carried out with an input tone on the base current at 1 GHz, with amplitude 400 μA, superimposed to the 400 μA DC component so as to fully quench the device. The further shift of gain collapse towards higher bias could be partly related to the conversion of DC power towards higher harmonics. Finally, we have investigated the effect of substrate thinning on the device performance, with nominal process metallizations. Reducing the substrate thickness from 120 to 60 μm causes a reduction of the thermal coupling between the fingers, and gives a marginal improvement to the self-heating of the individual finger (see Tab. 1). Thus, as shown in Fig. 8, the gain in the stable operation region is slightly higher, while the current collapse occurrence becomes a little bit worse. A more significant effect of substrate thinning can be expected for layouts wherein the thermal coupling of the fingers is more pronounced.

CONCLUSIONS

In this contribution we have reported a development of our self-consistent electro-thermal simulation tool for the analysis of power microwave devices. The description of the thermal layout properties has been complemented by the inclusion of the thermal spreading effect due to the presence of surface metallizations. By coupling the thermal model to a temperature-dependent large-signal device model, a fully dynamic model, solved in the frequency domain with the harmonic balance method, has been implemented, and applied to the simulation of multifinger power GaAs/AlGaAs HBTs. The metallizations have been shown to significantly improve the device thermal stability, by moving the onset of gain collapse towards higher collector bias.

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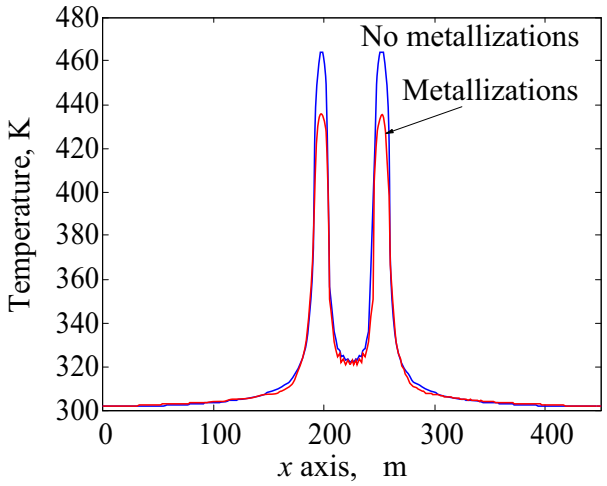

Figure 4: Temperature profile across the emitters without metallizations and with nominal thickness metal.

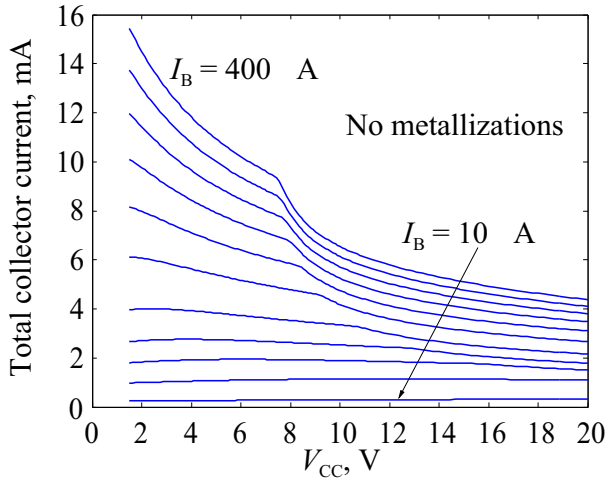

Figure 5: DC output characteristics without metallizations.

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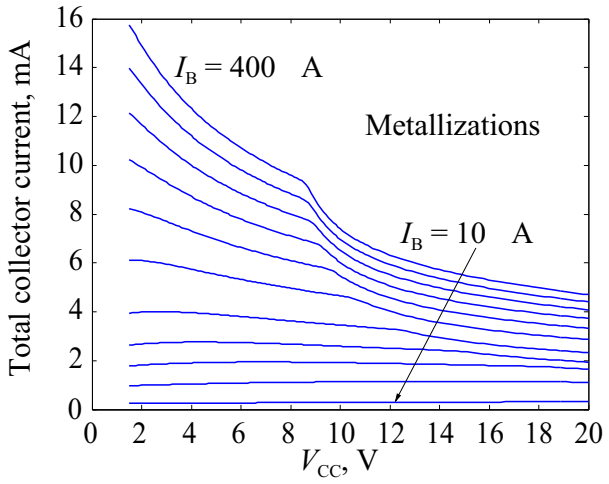

Figure 6: DC output characteristics with nominal metallizations.

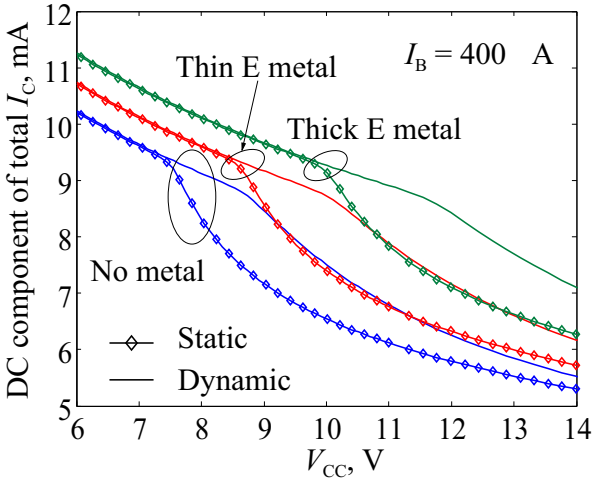

Figure 7: DC component of the total collector current for a DC base current $I_B = 400$ μA. Static simulations are denoted by symbols, the full line refers to the dynamic case (with a 400 μA input tone at 1 GHz superimposed to the 400 μA base bias). Three different metal layer thicknesses are considered.

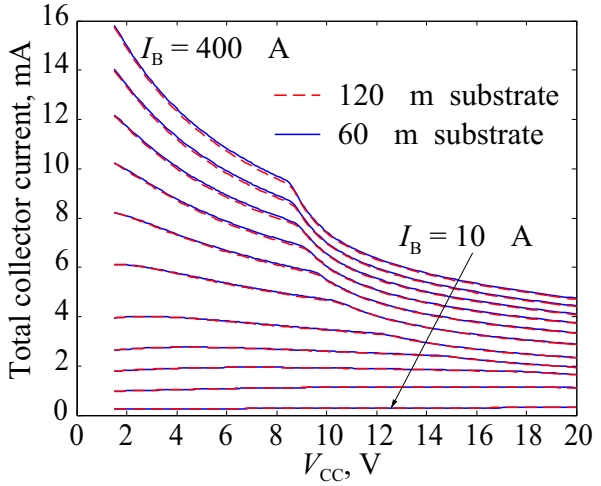

Figure 8: DC output characteristics for substrate thickness of 120 and 60 μm.