TECHNOLOGICAL TRENDS FOR T/R MODULES

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ABSTRACT

The concept of advanced phased array antennas, based on the combination of a large number of active elements, is critically dependant on the availability of compact and minimum weight, low consumption and high-reliability microwave T/R modules. The main guideline for the design is to achieve the best trade-off between performance, reliability and manufacturing cost.
THOMSON-CSF is leading phased array developments with T/R modules in S, C, X bands and also wideband for airborne, space and ground-based radars. Examples will be given.
The technological trends will be discussed, as following :

- Electrical architecture of the T/R module.
- Performance in relation with the GaAs processes : MESFET, pHEMT or HBT.
- Packaging in relation with the level of hermeticity :
  - . micro or macropackages,
  - . ceramic or printed circuit multilayer,
  - . silicon substrates,
  - . robotic manufacturing.
- Tests duration and number reduction..

Some different possible designs of T/R module for the future will be discussed.

INTRODUCTION

Space, airborne or ground-based active array radars in S, C, X bands or also wideband contain several hundreds or thousands of T/R modules. The cost, weight and volume of these modules make up a significant part of the radar. It is the reason why there are continuing developments in THOMSON-CSF in order to reduce these parameters, while increasing the transmitted power and reducing the noise figure. The T/R module packaging concept is critical to the reduction of the manufacturing cost. So all the constituents of a T/R module (MMIC, technologies, tests) have to be reviewed in relation to the design-to-cost.

ELECTRICAL ARCHITECTURE

Figure 1 shows some RF electrical block diagramms of T/R modules. The choice of the architecture, using or not a common part in both transmit and receive, is driven by the following considerations :

- Noise figure/TOI/power consumption trade-offs.
- Switching times.

So the position of the different functions (phase/shifter, attenuator, distributed gain and switches) is given by the result of calculations for all these parameters in accordance with the requirements. For example for space applications, when no strong TOI specification is needed, the case (b) is often used.

Phase-shifter aspects :

Some comparisons have been done in the past between analog or digital versions. Definitively, whatever can be the bandwidth, the digital solution is preferred. So often is used a MMIC phase-shifter which is designed to procure a phase-shift constant on the overall frequency range. Another possibility which can offer different advantages is to use the "delay" principle, and not the phase-shift. Figure 2 presents a 6 bits Delay Line Phase-Shifter (DLPS) layout in wide band (from 2 to 20 GHz). Other larger bits can be built on hybrid circuits, with lines between switches.
The drawback can be the compensation of the losses variation versus frequency.

Front end aspects :

The receiver protection has to take into account the radiating element behavior : a significant power can be reflected to the receiver. So the receiver protection must be selected in relation with the needed specification for losses, switching time, leakage and isolation. The choice has often to be done between a 3-port or 4-port circulator, a reflectiv or non-reflectiv limitor, including or not a high power switch.

LNA AND MULTIFUNCTION CHIP

Reduction in size of the module can be obtained by the integration of the low power RF functions into a single multifunction chip.

Multi Function Chip concept :

Advantages :

- better performance, better reproductibility and increase of the reliability, thanks to the interconnection integration,
- decrease of the total MMIC area,
- decrease, at the MMIC level, of the test cost (1 function instead of n),
- decrease of the assembly cost (lower chips number),
- decrease of the cost relating to the components supply, storage and management,
- decrease of the T/R module size and weight.

Drawback :

- decrease of the MMIC yield, regards to the bigger size : typically less than 10 %.

pHEMT Technology for Low Power Circuits :

- maturity of 0.25 µm pHEMT Technology with high reliability (UMS PH25),
- improved noise figure compared with MESFET (≈ 1 dB noise figure in X band, 0,8 dB in S band for examples).
- possible integration of LNA and MFC (including digital phase shifter, digital attenuator, amplifiers as well as switches) on a single chip.
- yield is comparable to MESFET technology,
- chip area : examples between 15 and 25 mm^2.

HPA

HBT and HFET MMIC's performance shows today a significant improvement compared to the MESFET technology : power density, power added efficiency, capability of higher output power on a single chip.

Figure 3 gives as illustration the PAE of discrete devices at 10 GHz in CW operation, as a function of the output power.

For the comparison between HBT and HFET or PHEMT, the results for narrow-band amplifiers are similar (in X-band especially). These technologies are today still under development in Europ and in the USA, but need further development work and support to translate them into fully characterised mature foundry processes. Performance in bandwidth are given in figures 4 and 5.

PACKAGING SURVEY

The first item to be discussed, in relation with the complete antenna requirements, is the T/R module grouping network : a monopack, a bipack, a quadpack,... a Npack ?
A lot of considerations has to be taken into account for the final choice.

- Thermal aspects :
  - . maximum heat exchange area,
  - . thermal contact,
  - . coolant or not.
- Mechanical aspects, dimensions, interconnection.
- Weight per module, level of integration.
- Environment : level of hermeticity (1 module, n packs, modules network, antenna ?).
- Antenna RF performance : relative position of the T/R module and the radiating element.
- T/R module performance.
- T/R module cost, alone.
- T/R module cost, inserted with support.

For a precise project, an analysis of the best trade-off is necessary, for each of these aspects, and for all these aspects together.
After this step, the figure 6 gives an overview of the different technological capabilities for a T/R module packaging.
The first decision to be taken is, at which level of integration will be made the hermeticity, with a drastic impact on the physical architecture :

- Micropackages with MMIC inside, and then the possibility to test some functions before final assembly. Interconnection can be provided by a multilayer PCB like presented in figure 7 - a).

- Macropackages with MMIC glued or brazed on a carrier, or directly mounted on a multilayer substrate (figure 7 - b).
  . If the interconnection substrate is a PCB or a TFML (Thick Film MultiLayer) ceramic, the hermeticity can be ensured by the lid (laser welding for example). In this case, where the assembly is planar, the housing is a metallic or MMC one, and the external interconnection can be realized by classical connectors or ceramic inserts.
  . If the interconnection substrate is constituted with LTCC or HTCC technology, housing and substrate are only one entity with an hermeticity given often by construction.

- Resine encapsulation for MMIC and ASIC is a way to be improved for localized hermeticity , and then cost reduction.

The figure 6 shows a classification of all these available or under development technologies, which can be choosen to satisfy the different requirements, in relation with the design-to-cost for a T/R module.

A special accent must be given to the development of very interesting packaging items :
- plastic housings,
- solderless vertical interconnections, for example with elastomers or fuzz-buttons (Cin : apse).
- 3-Dimensional assembly.

One of the THOMSON approach for technology has been demonstrated with microstrip MMICs, though it could be adapted to coplanar chips.
The principles of the technology are shown in figure 8. The basics are the following :
- T/R modules are composed of 3 MMICs : HPA, LNA and multifunctional carrier (total GaAs area : 0,35 cm2) and one control circuit (BiCMOS chip, 1 cm2) : figure 9.
- Large capacitances and circulator are outside the module.
- The level of integration is reached by assembling MMICs directly onto the silicon control circuit.

A 6 inches Si wafer is used as an active substrate where about 150 control circuits are integrated at a 1 cm pitch. The wafer is metallized and the metallization is etched in order to insulate decoupling capacitors, resistors and microwave ground plane. A 100 µm polyimide film is glued onto the wafer, and is locally removed where the MMICs are to be placed and above the pad of the control circuits, using a ablation process. The polyimide is then metallized and the metallization is locally etched. MMICs are glued or brazed into the cavities, directly on the silicon : a 10 µm positioning accuracy is necessery in the three axis. A second polymer film is glued onto the wafer, so the MMICs are totally surrounded by organic materials. This second layer will support 50 Ω connections between MMICs and low frequency connections to the control circuit. Finally a third polymer layer will give a final protection to the module and will support SNPb. After testing and dicing, the module will be mounted onto a multilayer PCB by solder reflow. Thermal management will be provided by gluing the silicon onto a heat sink (figure 10).

Assembly of MMICs digital phase shifters (X-band) onto their control has been realised to demonstrate the active silicon carrier concept (figure 11). Assembly of HPA onto silicon using Ausn brazing has also been demonstrated. Silicon offers a good thermal substrate for medium range HPA. When high power devices are to be used, reducing the thermal resistance will require substrates with larger thermal conductivity such as AlN or SiC. In this case, the module will be split in two parts : the LNA and multifunction MMICs hybridised onto the control unit, and the HPA in a separate package, the whole T/R module remaining smaller than 2 cm^2.

CONCLUSION

This paper has outlined some requirements for T/R modules for phased array antennas and has described the technological developments required for the future systems, in relation as for as possible with the design-to-cost.

ACKNOWLEDGEMENTS :

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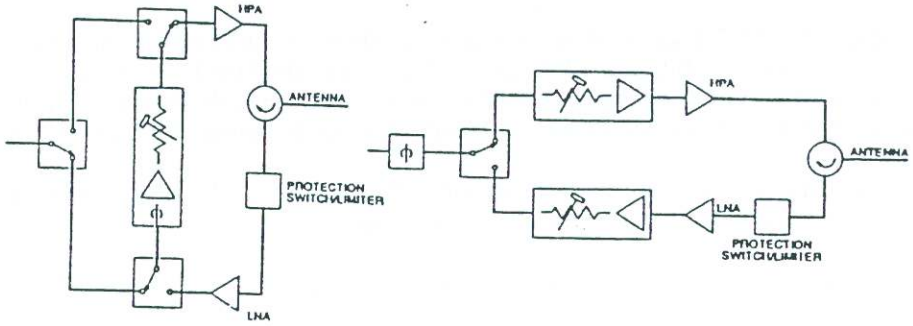

a) COMMON ARCHITECTURE b) SEPARATE ARCHITECTURE

Figure 1 : T/R module Architecture

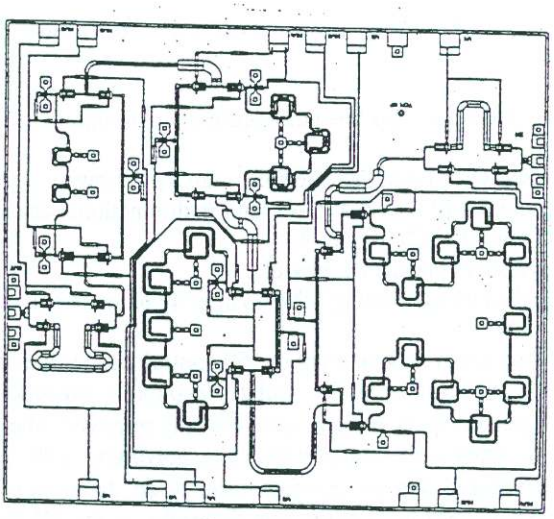

Figure 2 : DLPS Layout

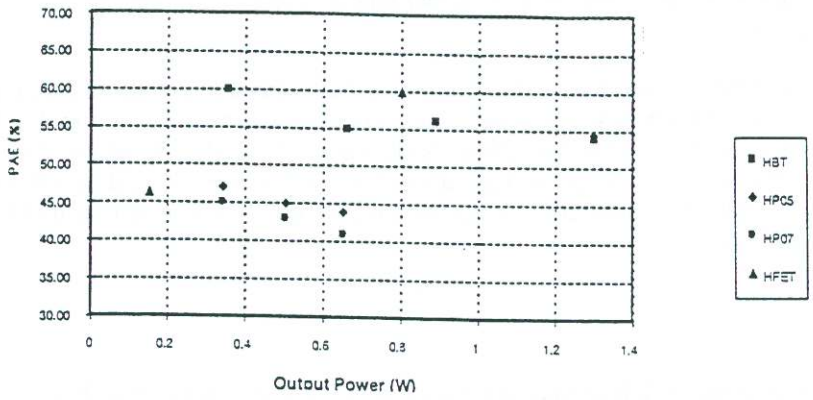

Figure 3 : PAE versus output power @10 GHz in CW of discrete devices

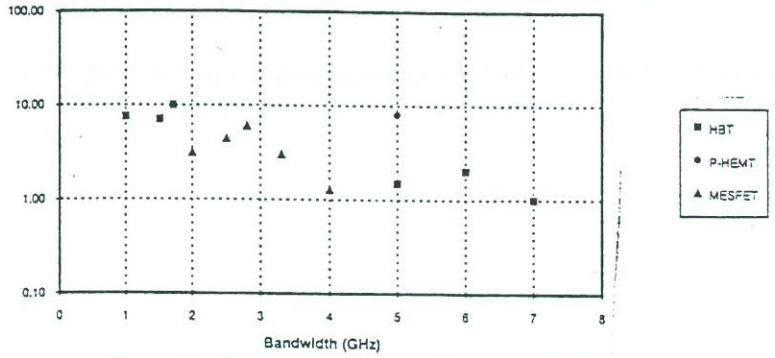

Figure 4 : Output power versus bandwidth of X-Band MMIC's

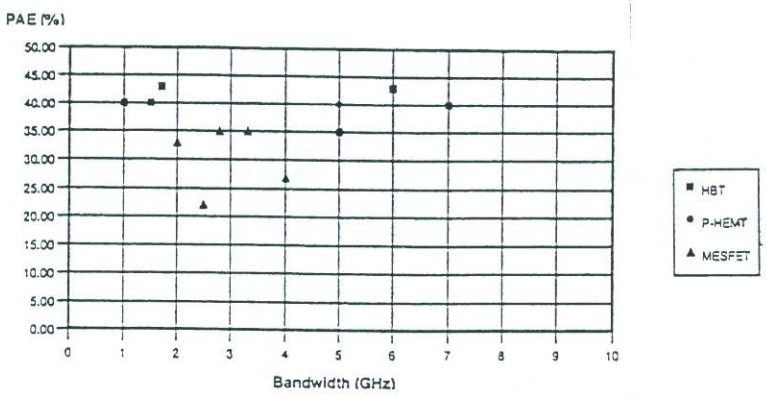

Figure 5 : PAE versus bandwidth of various X-Band MMIC's

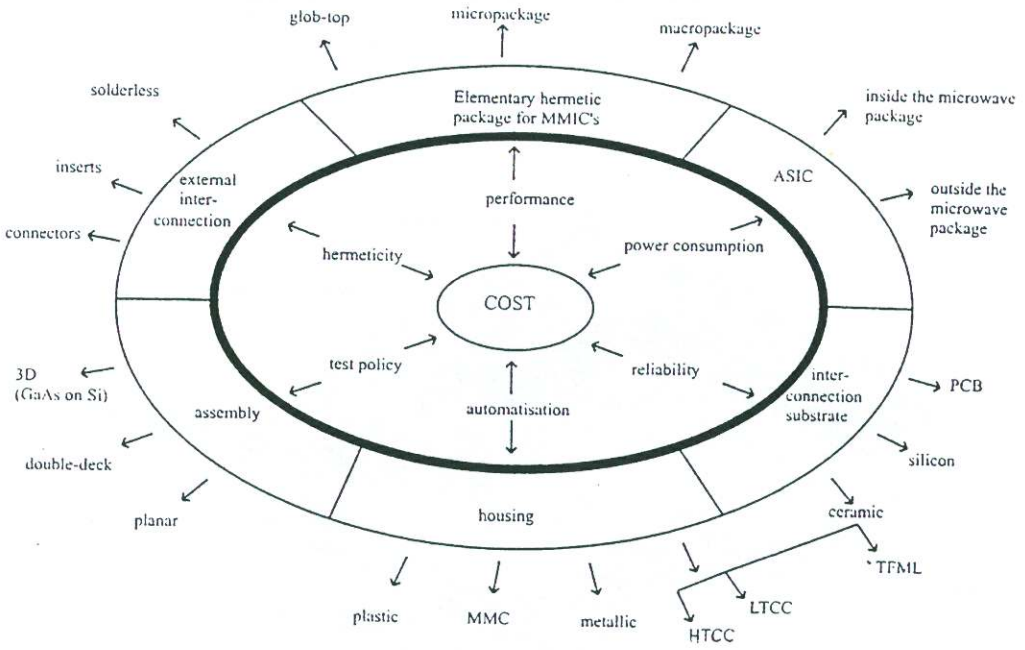

Figure 6 :Packaging survey

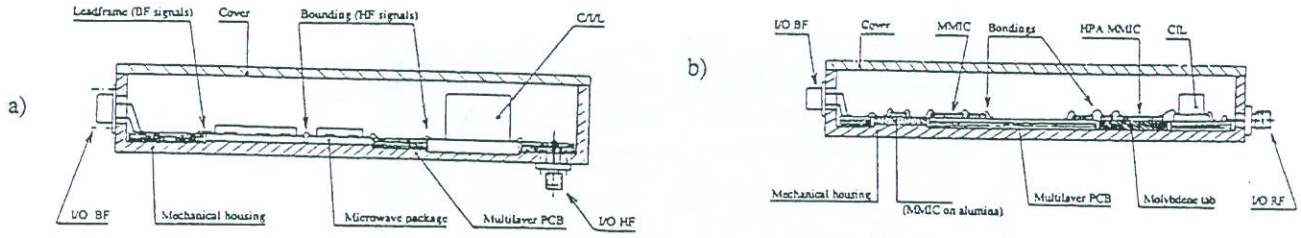

Figure 7 : Packaging

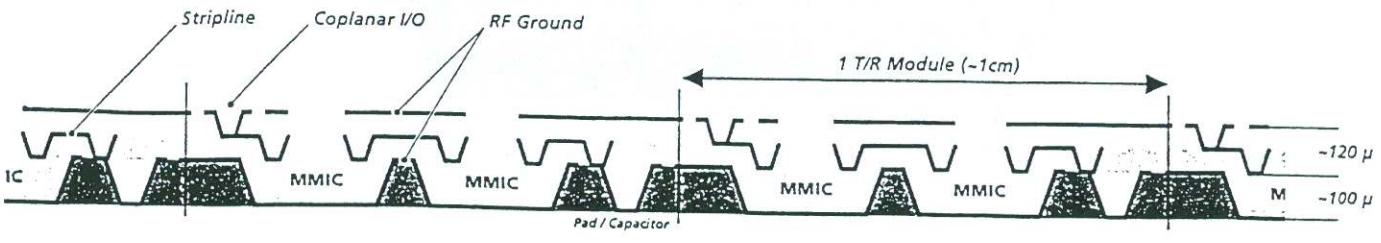

Figure 8 : Collective Wiring Technology

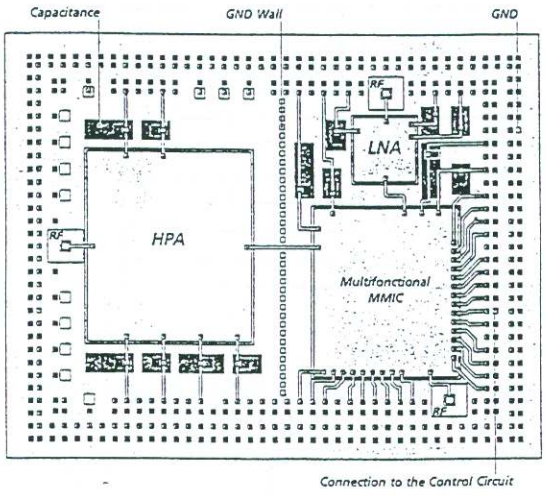

Figure 9 : T/R Module Design with 3 MMICs

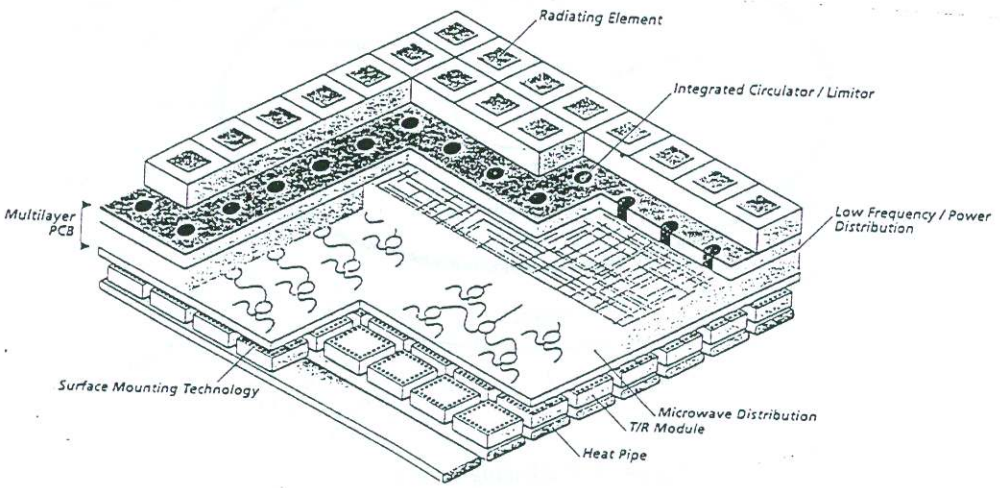

Figure 10 : Integration of Tile modules into a Smart Skin

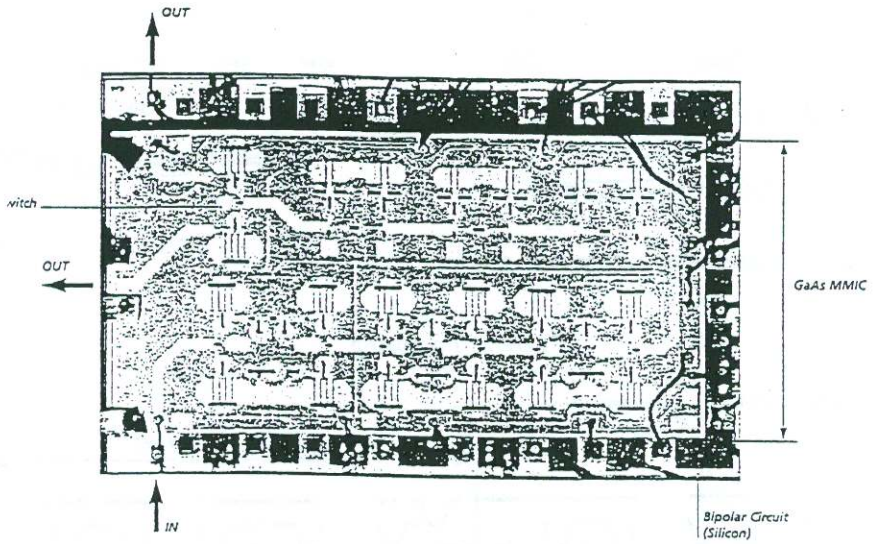

Figure 11 : MMIC Phase Shifter Hybridized on its Control Circuit