Modeling and Investigation of Instabilities in Heterojunction Interband Tunnel FET for Microwave Applications

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An analytical treatment for the stability of Resonant Tunneling devices is proposed. It exploits a previously proposed approach for Resonant Tunneling Diodes with the aim of deriving an effective guideline for the use of such class of devices in MMIC applications. The discussion is carried out on a class of devices deriving from the integration of Heterojunction Interband Tunneling Diodes (HITD) with HEMTs on an InP substrate, for different cases of device parameters uncertainty and circuit topologies. Preliminary simulations and experimental validation results are provided in the paper.

INTRODUCTION

Recently tunnel diodes have received a lot of attention in the microwave and analog high-speed field, see G. Manes et al (1). The enhancement in the semiconductor growth techniques, in particular MBE, has lead to improved device quality and performance and has also introduced new families of tunnel diodes. One family is based on intra-band resonant tunneling in semiconductor conduction band (RTD). Another family consists of Heterojunction Interband Tunneling Diodes (HITDs).

Table I: HITD's layer structure

P^+ - InGaAs	Top contact layer
nid – InAlAs	Barrier
nid – InGaAs	Well
N^{++} - InAlAs	Ohmic contact
N^+ InGaAs	Bottom contact layer
InP	Substrate

These HITDs are interesting because of the high peak-to-valley current ratios and the large span of the negative differential resistance region. Tunnel diodes have been used to demonstrate numerous applications and potential markets including digital to analog converters, clock quantisers, shift registers and ultra low power SRAMs, see Sebaugh and Lake (2). All these applications take benefit from the bi-stable inherent diode behavior and utilize the negative differential resistance (NDR) to increase the transition speed between the two stable states. A recent advancement in this class of devices is the monolithic integration of the tunnel diode into the structure of a three terminal device, resulting in a novel NDR device having three terminals. This new device is called Heterojunction Interband Tunneling FET (HITFET) and its third terminal can be used as gate control, see Nair et al (3).

Although tunnel devices in theory promise medium noise amplifiers, low noise converters, and low-cost oscillators in the microwave range, these circuits have never achieved the high volume of usage, which one would have expected on the basis of the claims being made. Primarily this is due to the low power handling capability of the tunnel diode and the stability issues, however in spite of these difficulties a number of significant applications of tunneling device based MMICs has been demonstrated, see A. Cidronali et al (4), (5), (6) and Auer and al (7). The paper gives an effective insight on the mechanism generating instability or unwanted oscillation on the basis of a simple equivalent circuit model and gives the guidelines for the proper use of such devices in microwave oscillators and other negative resistance circuits.

DEVICE STRUCTURE AND MODEL

The semiconductor structure of the HITD adopted here is shown in Table I; the HFET is a conventional In-P HEMT. These tunnel diodes have shown very high current densities (50-60KA/cm^2) and peak to valley ratios between 10 and 15, see El-Zein et al (8). Analysis of microwave performance shows a maximum frequency of oscillation to be around 60GHz for a 2.5x2.5μm^2 diode. The current–voltage, characteristics of a HITFET is shown in Fig. 1. The bias (drain) voltage spans from 0 V to 1 V while the gate control voltage spans from 0V to –0.8V (at step 100mV). The shift of the NDR region towards higher drain bias voltage is observed as gate bias magnitude is increased. For gate voltage close to 0V an increase in the magnitude of the NDR region is also observed. This results in a decrease in the cut-off frequency as the gate bias changes from 0V to pinch-off voltage due to the increase in drain-source resistance of the HEMT that is in series with the HITD.

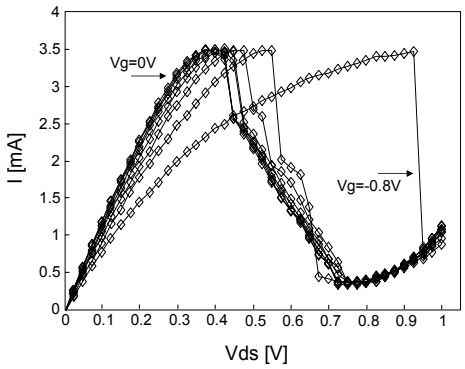

Fig. 1: I\V characteristic of the HITFET, Gate bias V_g spanning from 0 to -0.8V, step 100mV.

The HEMT also introduces a reactive component that modifies the self-resonant frequency slightly. For a HITFET the key property is the negative resistance, which can be tuned in amplitude and phase by the gate voltage that acts as a control voltage. Although, in principle, the interconnection between the HFET and the HITD can be obtained through any of the three terminals of the HFET, the most suitable configuration is the one with the HITD placed on the top of the drain electrode, namely a drain-HITFET, see Fig. 2a. Some technological solutions integrates RTD directly on the drain ohmic contact of the HFET obtaining a vertical monolithically integrated transistor, see Stock et al (9).

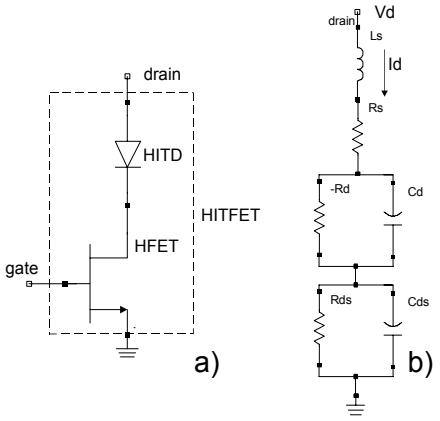

Fig. 2: (a) schematic representation of the HITFET, (b) equivalent circuit model adopted for the analytical treatment of the stability.

The solution adopted in this work consists in interconnecting the two devices as it is conventionally made for two or more elements of the same circuit. The performance in terms of S22 coefficient is reported in Fig. 3 between 100MHz to 20GHz for a bias voltage of 500mV and a control voltage spanning from 0V to –400mV. The schematic representation of the measurement set-up is in the inset of the same figure. In Fig. 3 it is also shown the maximum reflection coefficient magnitude, which spans from 8dB to 10dB depending on the control voltage, and the phase change according to the gate voltage. For the purpose of the discussion on the HITFET stability, a simple but effective model has been derived, see Fig. 2b. The model has been derived under the assumption that the HFET within the HITFET is biased at a drain-source voltage of few tens of mV; this makes the transconductance negligible with respect to the HFET output conductance. The drain-gate capacitance is also neglected.

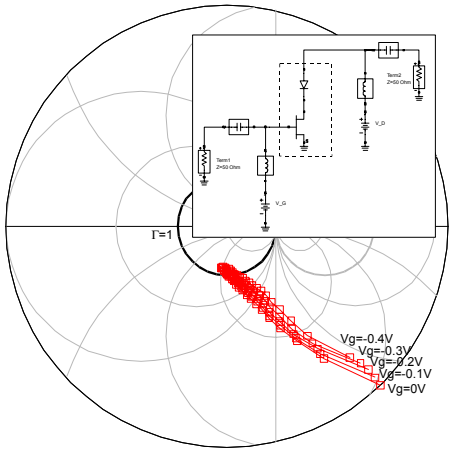

Fig. 3: Drain - HITFET's reflection coefficient as seen from the source terminal at 6.2 GHz, V_d=500mV as a function of the gate control voltages.

ANALYTICAL TREATMENT

In the Laplace domain the voltage-Kirchoff-law of the circuit in Fig. 2b is $V_d(s) = Z_H(s) \cdot I_d(s)$, the HITFET is short-circuit stable if the impedance $Z_H(s)$ has no zeros in the right half of the s-plane. After mathematic manipulation the impedance is:

$$Z_H(s) = (-L_s R_d C_d R_{ds} C_{ds}) \frac{N(s)}{D(s)} \qquad (1)$$

it turns that the stability condition is now imposed on $N(s)$ which can be written in the form:

$$N(s) = s^3 + a_2 \cdot s^3 + a_1 \cdot s^2 + a_0 . \qquad (2)$$

The polynomial coefficients a_i, are evaluated by the inherent time-constants and the self-resonance frequencies of the devices as in the follow:

$$\begin{aligned} a_0 &= \frac{\omega_d^2}{\tau_{ds}} - \frac{\omega_{ds}^2}{\tau_d} - \frac{1}{\tau_s \tau_{ds} \tau_d} \\ a_1 &= \omega_d^2 + \omega_{ds}^2 + \frac{1}{\tau_s \tau_{ds}} - \frac{1}{\tau_s \tau_d} - \frac{1}{\tau_{ds} \tau_d} \\ a_2 &= \frac{1}{\tau_s} + \frac{1}{\tau_{ds}} - \frac{1}{\tau_d} \end{aligned} \qquad (3)$$

for which hold:

$$\begin{aligned} &\tau_s = \frac{L_s}{R_s}; \quad \tau_d = R_d C_d; \quad \tau_{ds} = R_{ds} C_{ds}; \\ &\omega_d^2 = \frac{1}{L_s \cdot C_d}; \quad \omega_{ds}^2 = \frac{1}{L_s \cdot C_{ds}} \end{aligned} \qquad (4)$$

From the analysis of (2) it is possible to write the necessary and sufficient condition for the HITFET short-circuit asymptotical stability as:

$$a_2 > 0; \quad a_1 - \frac{a_0}{a_2} > 0; \quad a_0 > 0 \tag{5}$$

Once evaluated the equivalent circuit parameters, the (5) determine whether the stability of a particular device is critical or not. Conditions (5) are also useful if we want to investigate the stability issues with respect to variations of the equivalent circuit parameters or when a particular network is added to the circuit.

Effect of series inductor

In circuits of practical interest it is significant to assess the influence of a series choke inductor which is normally required to bias the device. It can be easily taken into account by substituting L_s with $\hat{L}_s = L_s + L_c$ in the above treatment, where L_c is the additional series inductor. In a state-of-the-art InGaAs–InAlAs HITFET the capacitors C_d and C_{ds} have very close values, moreover R_d for well designed devices has to be much higher than R_{ds} and R_s, therefore the following further conditions are usually fulfilled:

$$R_d C_d - R_{ds} C_{ds} > 0 \; ; \quad R_d > R_s + R_{ds} \tag{6}$$

In the hypothesis that the HITFET itself (i.e. with $L_c = 0$) is short-circuit stable, only the second condition of (5) can by changed by the presence of an additional series inductor. The critical value of $\hat{L}_s$ is given by that equation, if L_c is further increased the circuit becomes unstable and the frequency of oscillation decreases for increasing values of L_c.

Effect of series resistor

This case represents the practical situation of an unsure ohmic loss evaluation. Equivalently to the previous case, R_s is replaced with $\hat{R}_s = R_s + R_1$, where R_1 represent the additional loss in the network. If the first condition of (6) is verified, the insertion of the serial resistance increases both a_2 and a_1 while decreases a_0. The circuit is then stable until a_0 becomes negative; this occurs when $R_1 > R_d - R_{ds} - R_s$. This possibility leads to growing exponential functions solution for (1) which is a kind of instability like the one discussed in Kinder et al (10) and Cidronali (11). It can also be demonstrated that, if we add both a serial resistance R_1 and a serial inductor L_c, the circuit is stable for higher values of L_c than those obtained when only the inductance is added, but when the circuit becomes unstable the oscillation frequency is not affected by the resistance R_1.

Effect of a parallel capacitance with the HITD

This case represents the incorrect evaluation of the diode junction capacitance. Adding a parasitic contribution C_p we obtain: $\hat{C}_d = C_d + C_p$. In this case the stability is critical only for very low values of $\hat{C}_d$, therefore if the HITFET itself is stable (i.e. conditions (5) are verified for $C_p = 0$), it can be demonstrated that stability conditions are not changed by C_p. The most relevant effect associated to this case is a reduction of the diode negative resistance cut-off.

Effect of a parallel capacitance with the HFET

As the previous one, this case considers a wrong estimation of the drain-source capacitance; moreover it gives also a guideline for the correct choice of the HFET size. Introducing $\hat{C}_{ds} = C_{ds} + C_d$ and supposing that the condition $R_d > R_{ds} + R_s$ is always true, it is possible to identify three different situations on the basis of the value of R_d. Defining C_{z1}, C_{z2} as the zeros of $a_1 - \frac{a_0}{a_2} = 0$ we obtain the following situation:

1. $R_d < \frac{L_s}{C_d (R_{ds} + R_s)}$: the circuit is stable only if there are real zeros for $a_1 - \frac{a_0}{a_2} = 0$ and $C_{z1} < \hat{C}_{ds} < C_{z2}$
2. $\frac{L_s}{C_d (R_{ds} + R_s)} < R_d < \frac{L_s}{C_d R_s}$: the circuit is stable only if $\hat{C}_{ds} < C_{z2}$, being $C_{z1} < 0$
3. $\frac{L_s}{C_d R_s} < R_d$: the circuit is always stable.

MODEL VALIDATION

The experimental validation of the procedure described above has been carried out in the first two cases, inductor and resistor in series. As a first step the equivalent circuit represented in Fig. 2b for a sample fabricated on a In-P substrate has been extracted. The complete set of parameters is the following: $R_s = 6.4\Omega$, $L_s = 0.187\text{nH}$, $R_{ds} = 17.3\Omega$, $C_{ds} = 0.2\text{pF}$, $R_d = 190\Omega$, $C_d = 0.11\text{pF}$. These values lead to a critical inductance of $L_c = 1.39\text{nH}$ (with a 50Ω RF load) and to a critical resistance of $R_1 = 166\Omega$. The output spectrums reported in Fig. 4 are obtained through CAD simulations, using previously developed non-linear models of the HITD and HFET, see Cidronali et al (4) and El-Zein et al (8), and adding a series inductor of $L_c^{(1)} = 1.2\text{nH}$,

$L_c^{(2)} = 1.5\text{nH}$, $L_c^{(3)} = 1.8\text{nH}$ respectively. The absence of a spectral content, different from the background noise, obtained in the first case, demonstrates the accuracy of the analysis.

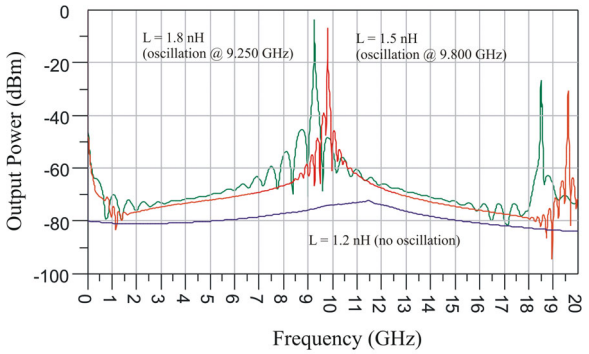

Fig. 4: Simulated output spectrum for L_c=1.2 nH (stable), L_c=1.5 nH and L_c=1.8 nH (both unstable).

In Fig. 5 the result of a time-domain simulation with a series resistor of $R_l = 180\Omega$ is reported. As it can clearly be seen the circuit is unstable but no sine-wave oscillation is observed.

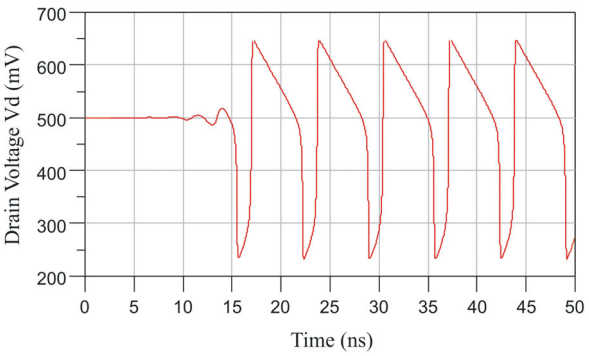

Fig. 5: Drain Voltage vs. time plot, R_l=180 Ω.

In Fig. 6 the measured output spectrum of the same HITFET with an external series inductor of $L_c = 2.7\text{nH}$ is reported.

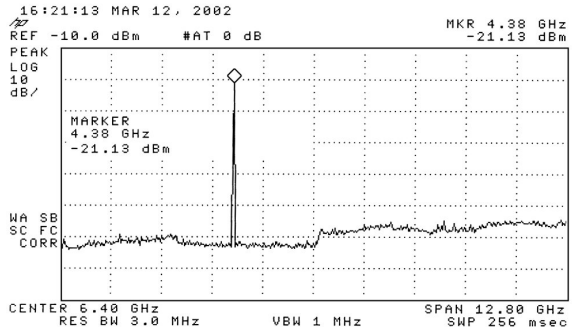

Fig. 6: Measured spectrum for L=2.7 nH; the circuit oscillates @ 4.38 GHz with an output power of –21.13 dBm.

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