

AlGaAs/GaAs HFET Power Devices for J-Band Applications: Performance Dependence on Gate Recess Geometry

C. Lanzieri[°], R. Menozzi*, D. Dieci[#], M. Peroni[°], A. Cetronio[°], C. Canali[#]

[°]Alenia Difesa, Un'Azienda Finmeccanica S.p.A.
Via Tiburtina Km. 12.400, 00131 Roma, Italy.

* Dipartimento di Ingegneria dell'Informazione, University of Parma
Viale delle Scienze, 43100 Parma, Italy

[#]Dipartimento di Scienze dell'Ingegneria and INFN, University of Modena
Via Campi 213/B, 41100 Modena, Italy

ABSTRACT

We show in this work that Al_{0.25}Ga_{0.75}/GaAs power HFET's can offer substantial performance improvement at J-Band over conventional GaAs power MESFET's with the same geometry. Further performance enhancement is offered by a non-lithographic gate etching technique able to downscale the gate length to 0.3 μm . The paper will discuss the advantages and possible limitations of this gate scaling process; in addition, evidence will be given of the good hot-electron reliability of these devices.

1. INTRODUCTION

Heterostructure FET's (HFET's), where a large-bandgap n-AlGaAs layer is grown on top of a relatively high-doping n-GaAs channel, currently represent a good compromise for the industrial production of high performance devices covering the upper end of the microwave spectrum. In comparison with GaAs MESFET's, HFET's offer a larger input voltage swing due to higher Schottky barrier, and a better trade-off between channel conductance (and consequently, output power) and drain-gate breakdown voltage (BV_{DG}), due to lower doping of the AlGaAs barrier layer [1]. Over GaAs pseudomorphic HEMT's, they feature, in addition to much easier epitaxial growth, improved linearity, due to low AlGaAs doping and the absence of parasitic conduction therein, and larger current capability, since the channel thickness is not limited by the critical value for pseudomorphic growth. The distinctive features of HFET's are particularly attractive for microwave power applications; therefore, the device design is mainly aimed at achieving large channel conductance, high BV_{DG} , large input voltage swing, good linearity over a wide gate bias range, and at reducing hot electron effects, or confining them to bias conditions where they do not limit the power handling capability nor pose reliability concerns [2].

In this work we report on the performance superiority of power HFET's, as compared to power MESFET's, in the frequency range up to J-Band. We will also demonstrate that performance enhancement, in terms of device gain and bandwidth capability per output power, can be achieved by controlled gate-length reduction down to 0.3 μm obtained by simple processing techniques.

The most stringent reliability issues for power FET's are typically related to hot electron and impact ionization conditions, i.e. to on-state and off-state breakdown (the latter being the gate-drain breakdown occurring with the channel completely pinched-off). The design strategy adopted for our power HFET's leads to minimizing hot electron and impact ionization effects, and to confining them at bias conditions very close to the device threshold, i.e., far from the operating bias points for class A operation [2]. Figure 1 shows the output characteristics of an AlGaAs/GaAs HFET. The shadowed area represents the most critical region for impact ionization. Figure 2 shows the typical impact ionization-dominated bell-shaped I_G - V_{GS} curves and the off-state breakdown gate currents for different drain-source bias voltages (V_{DS}). In the shadowed region of Fig. 2, the device works under pronounced impact ionization regime, with possible deleterious reliability effects. Since, in order to maximize the output swing, it could be useful to operate the HFET along a load line that reaches high V_{DS} , as show in Fig. 1, we investigated how these devices react to hot carrier effects. As documented in Section 3, our results have shown that these devices feature a very good hot carrier reliability.

2. SAMPLES AND EXPERIMENTS

The devices studied in this work derive from Alenia's standard double-recess process for power HFET's (AL07EP). They feature n-GaAs channel, Si-doped at $4 \times 10^{17} \text{ cm}^{-3}$ and $\text{Al}_{0.25} \text{Ga}_{0.75} \text{As}$ barrier layer, Si-doped at $2 \times 10^{17} \text{ cm}^{-3}$. After recess formation by wet etching, $1 \mu\text{m}$ Ti/Al gates are deposited, and subsequently gate-length reduction is carried out by selective lateral dry-etching of the Ti layer, to form a T-shaped gate with the desired footprint length (L_g). With this technique, HFET's with L_g ranging from 1 to $0.3 \mu\text{m}$ can be routinely fabricated. As shown schematically in Fig. 3, the gate recess is $1 \mu\text{m}$ wide, and the source-drain spacing is $5 \mu\text{m}$. The HFETs are passivated by a plasma-deposited SiN layer. The DC electrical measurements and stress cycles were carried out using an HP-4145 semiconductor parameter analyzer. For the transconductance dispersion, we used a setup based on a Schlumberger 1255 HF Frequency Response Analyzer. A small signal voltage wave of frequency f is superimposed to the DC bias applied to the gate of the transistor under test (used as an inverter and biased within the linear region); then the small signal voltage on the drain is measured. The amplitude of the output wave divided by that of the input one gives a number proportional to $g_m(f)$.

In order to inspect the robustness of devices under hot electron conditions, two methods of step-stress tests have been performed: HES (Hot Electron Stress) and HRC (High Reverse Current) [3]. All tests were carried out at room temperature on devices with $L_g = 0.6 \mu\text{m}$ and $W_g = 200 \mu\text{m}$. At each step, the devices were stressed for 25 hours.

In the HES, V_{GS} is fixed at the maximum of the I_G - V_{GS} bell-shaped curve [4] of the virgin device ($V_{GS} \approx -2.5 \text{ V}$), while V_{DS} is increased by 0.25 V at each step, starting from 5.5 V .

The HRC stress was instead carried out with source floating, and driving the gate-drain diode with a reverse current equal to the I_G measured, at the corresponding step, during the HES.

Figure 4 shows the gate current (I_G) at each step, together with the dissipated power, both for the HES and the HRC step-stress tests. In the upper horizontal axis we reported the applied V_{DS} and the measured V_{DG} for the HES and the HRC, respectively. It is worth noting that the voltage between the gate and the drain was much higher, at each step, in the HRC stress than in the HES, therefore causing larger electric field and carrier heating (see paragraph 3.2). The HES was stopped after 700 hours, when the dissipated power P_D reached 180 mW . At this power level, it becomes questionable to neglect thermal-induced degradation. The HRC test was stopped after 600 hours, since it had reached a very high V_{DG} (20.4 V).

3. RESULTS AND DISCUSSION

3.1 Performance

Figures 5 and 6 show the class A output power and power added efficiency (PAE), respectively, measured at 10 GHz , as a function of the input power, for 1 mm -wide MESFET and HFET devices. The HFET's are clearly superior to conventional power MESFET's (fabricated at Alenia laboratories, and independently optimised for power performance at J-Band) with the same gate length. Furthermore, additional performance improvement can be achieved through gate-length reduction using the side etching process outlined above. The small signal power gain (MSG/MAG) of the devices, reported in Fig. 7, clearly indicates the capability of HFET's to operate at J-Band: in particular, at 24 GHz the $0.4 \mu\text{m}$ gate length device has a MAG larger than 6 dB .

Although the lateral dry-etching process for gate footprint reduction has proved to yield highly reproducible, high performance power devices without resorting to e-beam or other sophisticated photolithography techniques, work is in progress to tune a suitable passivation process capable to suppress the surface state density generated in the gate recess region by the dry-etching [2]. The influence of the surface states is illustrated by Fig. 8, where we plot the frequency dependence of the transconductance of two HFET's, one that did not undergo the gate side-etching (non-etched) and one whose L_g was reduced to $0.6 \mu\text{m}$ by side-etching (etched). While the non-etched device does not show any relevant g_m dispersion up to 100 KHz , a small g_m decrease with increasing frequency is observed on the etched device, a typical signature of surface states [3,5]. It should also be noticed that the g_m dispersion is smaller for more negative gate bias, where the current conduction is pushed away from the surface. A consequence of this low-frequency reduction of the device gain is shown in Fig. 9, where we plot the magnitude of S_{21} for 3 HFET's, with $L_g = 1, 0.7, \text{ and } 0.35 \mu\text{m}$, respectively. Due to the surface state effects described above, at low frequencies (from 100 MHz to a few GHz) $|S_{21}|$ is smaller for

shorter devices; as the frequency increases, instead, the reduction of the gate capacitance caused by L_g scaling prevails, and the device gain ends up showing the proper scaling behaviour (with larger $|S_{21}|$ for shorter gates) in the upper frequency range ($f \geq 5$ GHz). The small-signal data are consistent with the power performance improvement at 10 GHz presented in Figs. 5 and 6 for the scaled device. Although the effect of surface states is quite limited and does not represent a serious concern, some enhancement of the HFET performance can be expected once the surface-state-induced g_m decrease will be completely eliminated by a suitable passivation technique.

It is finally worth pointing out that, despite these surface-state effects, the influence of gate side-etching on the gate leakage and on the BV_{DG} is largely beneficial, consistently with the results of [6]: as L_g is scaled from 1 μm to 0.3 μm , BV_{DG} increases from 11-13 V to 17-18 V.

3.2 Hot electron reliability evaluation

Several device electrical parameters have been regularly measured at the end of each HES and HRC step.

The threshold voltage V_T did not show to be affected by either HES or HRC, even in the presence of substantial electron heating and impact ionization (see Fig.4: during the 700 hours step the HES reached an I_G of -3.1 mA/mm, and a V_{DG} of 20.4 V was measured during the 600 hours step of the HRC stress).

We measured an increase of the drain parasitic resistance R_D by 8% and 22% at the end of the HES and HRC stress, respectively. This phenomenon has to be attributed to an accumulation of negative charge, possibly associated with an increase of the concentration of surface states in the gate-drain access region, caused by impact ionisation [7-9]. The negative charge extends the surface depletion over the gate-drain access region, causing a more resistive path for the electrons travelling toward the drain.

We observed no change of the source parasitic resistance R_S , because the electric field peaks under the drain end of the gate, leaving the source-gate access region unaffected.

A relatively small reduction of I_{DSS} (measured at $V_{DS} = 2$ V) has been observed, which has to be related to the R_D increase. The relative change of I_{DSS} was 5.5 % and 15 % at the end of the HES and HRC stress, respectively.

Creation of new surface states after the stresses is confirmed by the observed increase of the transconductance frequency dispersion. Figure 10 shows the transconductance vs. frequency dependence (at $V_{DS} = 300$ mV, $V_{GS} = 0$ V), as measured after several steps of the HES (a similar behavior has been observed during the HRC stress). The increased surface state concentration allows the gate input signal to modulate a larger depletion region, i.e., which enhances the g_m dispersion [3,5].

The phenomenon of surface state creation due to impact ionisation leads also to a beneficial effect on the gate-drain breakdown voltage (BV_{DG}), measured leaving the source floating and forcing a reverse current of 1 mA/mm through the gate-drain diode (very similar results are obtained by considering the off-state breakdown voltage, measured with the procedure described by del Alamo [10]). The negatively charged surface states extend the depletion layer under the gate-drain access region, causing a lower peak electric field, hence reducing carrier heating and the impact ionization rate. As reported in Fig. 11, we observed a BV_{GD} change of 5 V (from -13.5 V to -18.5 V) after 700 hours of HES and of 6.4 V (from -14.6 V to -21 V) after 600 hours of HRC. Figure 12 shows the gate-drain diode reverse characteristics, measured after different HES steps (again, the HRC stress presented a similar behavior). The so-called "breakdown walkout" [7-9] is clearly visible. No significant change has been observed on the gate-source breakdown voltage BV_{SG} , as also shown in Fig. 11, confirming that surface states are created and electrons are trapped only over the gate-drain access region, where electrons are hottest.

From the stress results we can conclude that HES and HRC tests induce the same degradation phenomena on our devices. The degradation rate in the HRC stress was higher, though, because of the very high electric fields reached between gate and drain. R_D and I_{DSS} degradation only occurred at quite extreme stressing conditions, with extremely high electric fields involved. One can therefore aspect a good device hot electron robustness during usual working conditions (typically involving V_{DG} values not larger than 10 V). In addition, the breakdown performance is improved by the stress.

4. CONCLUSIONS

We have shown that good performance at J-Band can be obtained with AlGaAs/GaAs HFET's. These devices out-perform GaAs MESFET's with the same geometry, and further benefit from the use of a lateral gate dry-etching process for length reduction down to 0.3 μm . This non-lithographic gate scaling technique was shown to consistently yield high-performance, reliable HFET's for power applications at J-Band. Some issues related to the creation of surface states on the etched areas beside the T-gate footprint will be tackled by proper tuning of the passivation process.

We have also tested the hot carrier reliability of our devices. Both open-channel and two-terminal drain-gate step stress tests were carried out bringing the device to extreme bias conditions, far from the usual working state. Considering this, the observed degradation of the main electrical parameters was minor and the device showed a good overall reliability. Furthermore the gate-drain junction breakdown voltage improved, due to surface states generation and increased depletion over the gate-drain access region.

REFERENCES

- [1] J. L. B. Walker, Ed., *High-Power GaAs FET Amplifiers*, Artech House, 1993.
- [2] R. Menozzi, M. Pavesi, M. Manfredi, C. Ghezzi, C. Lanzieri, M. Peroni, and C. Canali, "Hot Electron and DX Center Insensitivity of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}/\text{GaAs}$ HFET's Designed for Microwave Power Applications," to be published on the *IEEE Trans. Electron Devices*.
- [3] G. Meneghesso, Y. Haddab, N. Perrino, C. Canali, E. Zanoni "Drain Current DLTS analysis of recoverable and permanent degradation effects in AlGaAs/GaAs HEMT's," 1996 *Microelectronics and Reliability*, vol. 36, pp. 1895-1898.
- [4] C. Tedesco, C. Canali, A. Neviani, E. Zanoni, A. Cetronio, C. Lanzieri, "Dependence of Ionization Current on Gate Bias in GaAs MESFET's," 1993, *IEEE Trans. Electron Devices*, vol. ED-40, pp. 498-501.
- [5] P. H. Ladbroke and S.R. Blight, "Low-field low-frequency dispersion of transconductance in GaAs MESFET's with implications for other rate-dependent anomalies," 1988, *IEEE Trans. Electron Devices*, vol. 35, pp. 257-267.
- [6] D. Geiger, J. Dickmann, C. Wolk, E. Kohn, "Recess Dependent Breakdown Behavior of GaAs-HFET's," 1995, *IEEE Electron Device Lett.*, vol. 16, pp. 30-32.
- [7] A. Christou, Ed., *Reliability of Gallium Arsenide MMICs*, John Wiley & Sons, New York, 1992, pp. 143-148.
- [8] R. Menozzi, P. Cova, C. Canali and F. Fantini, "Breakdown Walkout in Pseudomorphic HEMT's," 1996, *IEEE Trans. Electron Devices*, vol. 43, p. 543-546.
- [9] P.C. Chao, M. Shur, M. Y. Kao, B.R. Lee, "Breakdown Walkout in AlGaAs/GaAs HEMT's," 1992, *IEEE Trans. Electron Devices*, vol. ED-39, pp. 738-740.
- [10] S. R. Bahl, J. A. del Alamo, J. Dickmann, and S. Schildberg, "Off-State Breakdown in InAlAs/InGaAs MODFET's," 1995, *IEEE Trans. Electron Devices*, vol. 42, pp. 15-22.

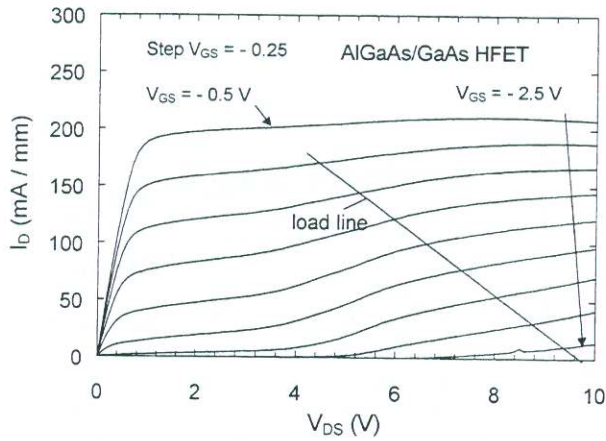


Fig. 1- HFET output characteristic and load line.

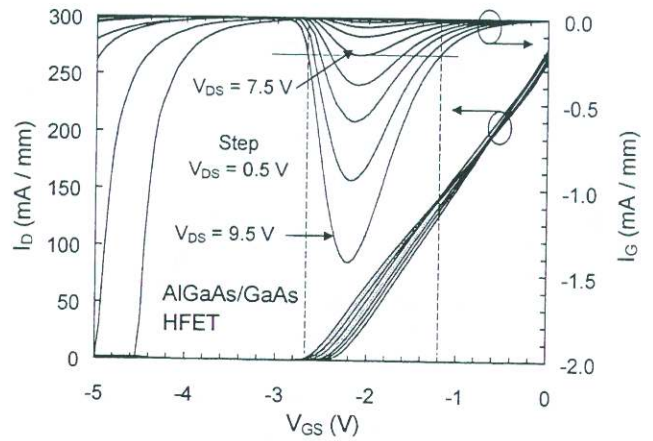


Fig. 2- Impact ionization region of an HFET.

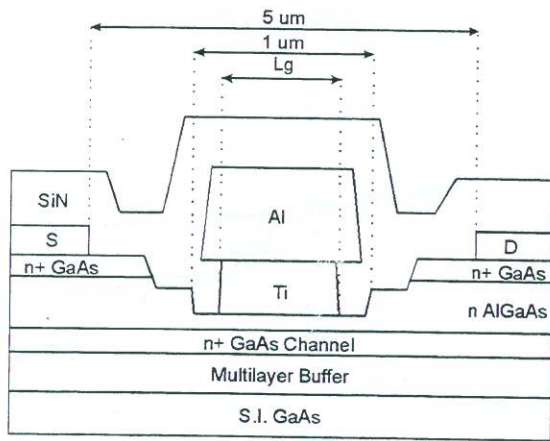


Fig. 3- Schematic cross section of the HFET's.

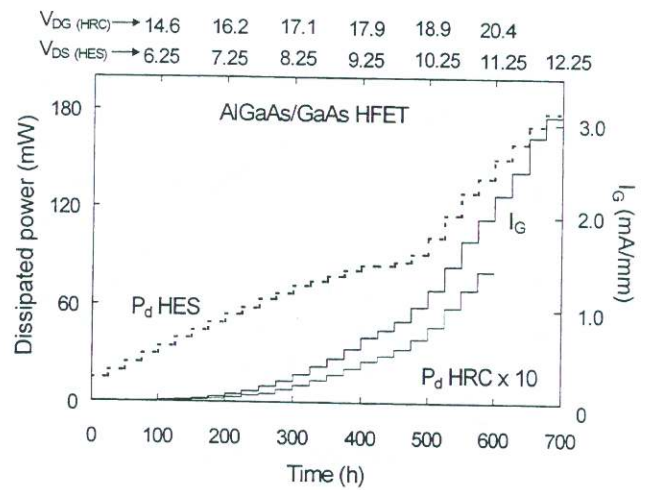


Fig. 4- Dissipated power and measured I_G during HES and HRC step stress tests.

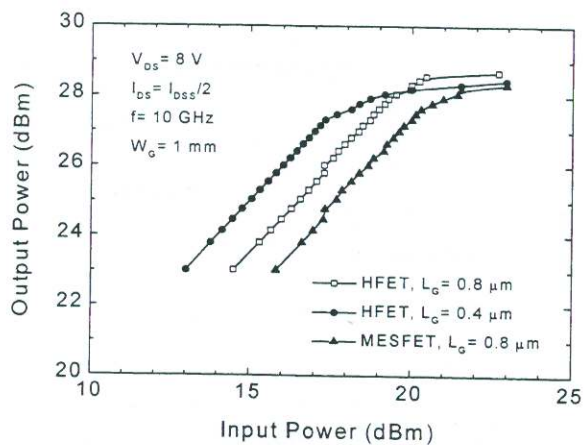


Fig. 5- Output power vs. input power.

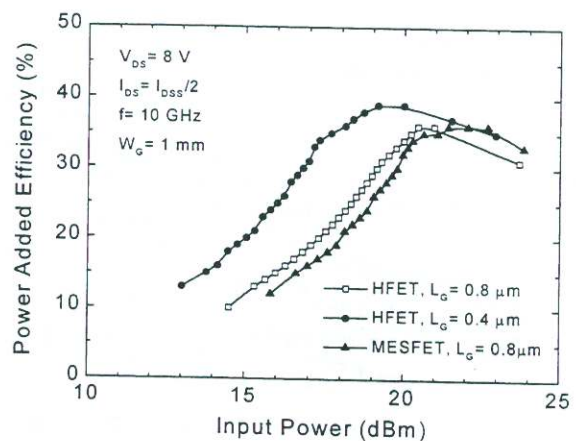


Fig. 6- Power added efficiency vs. input power.

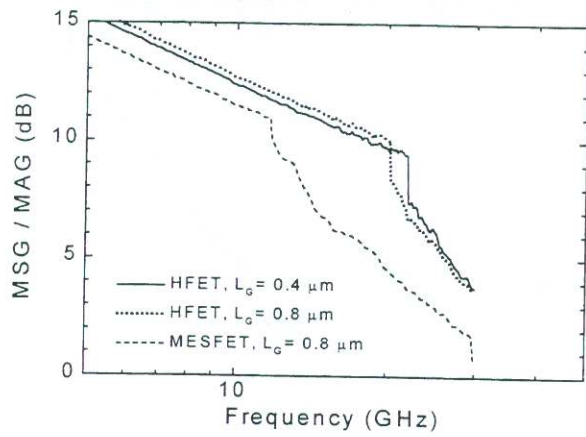


Fig 7- Small-signal power gain vs. frequency.

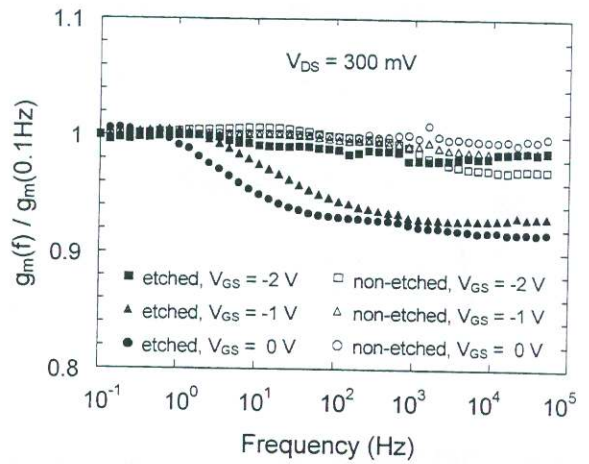


Fig. 8- Transconductance frequency dispersion in the linear region.

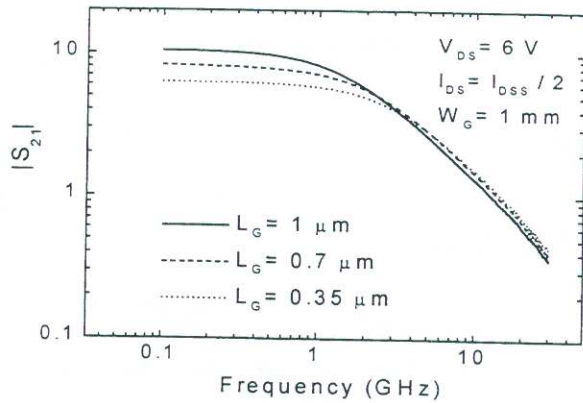


Fig 9- Magnitude of S_{21} vs. frequency.

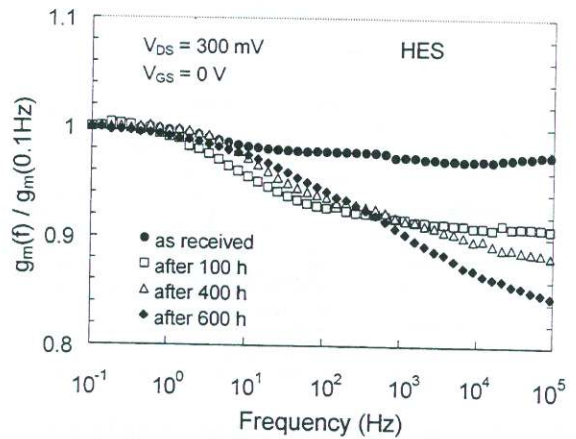


Fig. 10- Rise of g_m frequency dispersion at increasing steps of HES stress.

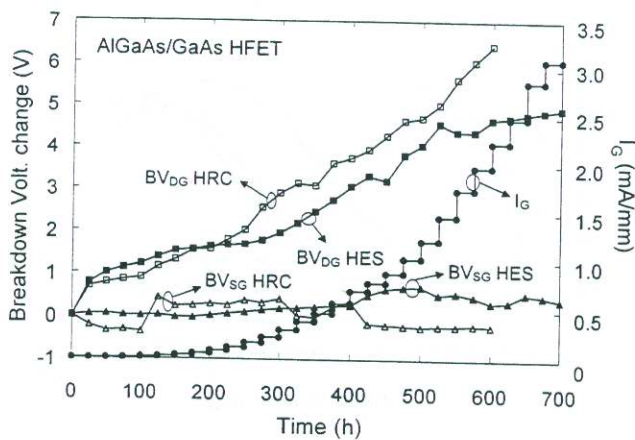


Fig 11- Change of the drain-gate and source-gate breakdown voltage vs. stress time.

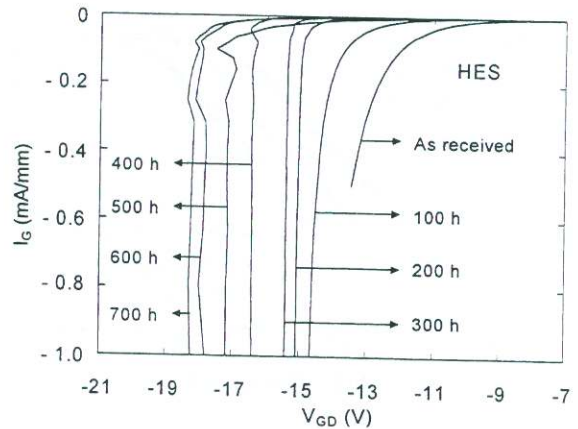


Fig. 12- Drain-gate breakdown walkout during HES step stress test.