A single relaxation-time non-quasi-static model for monolithic MESFET devices

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In this contribution a MESFET equivalent circuit that takes into account the device's non-quasi-static (NQS) effects is presented. The model topology is deduced directly from the small-signal measurement analysis and consists of a small-signal equivalent circuit that can be obtained from the linearization of a non-linear NQS model with non-linear state-functions (terminal charges and currents) that include a single relaxation-time. Results confirm that just one relaxation-time for all components is needed. The proposed model provides small-signal simulation performance similar to conventional models, but incorporating NQS effects in a consistent way and using just a reduced number of non-linear functions.

INTRODUCTION

Most applications of MESFET devices require a small-signal equivalent circuit, and many also demand a large-signal model. It is desirable that both models are consistent, i.e. to be able to deduce one from the other. Measurements are the main source of information for the simulation process regardless of the model topology or the parameter extraction technique used to determine the model element values. Small-signal measurements at different bias conditions are widely used to obtain the non-linear model from the bias dependence of the small-signal parameters. In this case, consistency between linear and non-linear models is a must.

In this contribution the development of a non-linear NQS equivalent circuit is presented. Initially, the small-signal equivalent circuit topology is deduced from just the information provided by the small-signal measurements of the device. In fact, the model for the device under cold-FET bias conditions is firstly deduced. The topology of this small-signal equivalent circuit suggests the definition of the non-linear state functions (terminal charges and currents) that describe the non-linear model. These functions include a relaxation-time that happens to be the same for all of them. The small-signal equivalent circuit for the device under any bias conditions (hot- or cold-FET) is then deduced from the linear approximation of the non-linear model. Finally, the bias dependence of the element values of this small-signal equivalent circuit could be integrated and, thus, the non-linear state functions could be calculated.

The resultant model includes some novel aspects. The first distinctive feature is the presence of NQS effects in the non-linear current sources. Most conventional large-signal FET models account for NQS behaviour in charge sources but assume quasi-static conduction currents [1]. The second main feature of the model is to use the same relaxation-time for all charge and current sources. A large-signal FET model that accounts for NQS effects in both components has been also proposed in [2], but using two different relaxation-times and different dynamics for the state functions.

NQS EFFECTS IN THE SMALL-SIGNAL EQUIVALENT CIRCUIT

The proposed process has been applied to a 4x100 μm monolithic MESFET device, measured from 1 to 40 GHz, at different bias conditions.

The starting point is the analysis of the small-signal device measurements biased under cold-FET conditions (V_{DS}=0). Using Bode diagrams (see Fig.1), the open-circuit Z-parameters can be analysed and a simplified 'T' topology equivalent circuit can be obtained for the device under normal gate bias conditions.

The resultant 'T' topology equivalent circuit, shown in Fig. 2a, provides quite good prediction of the small-signal measurements (see Fig.3) under cold-FET bias conditions. This model is particularly interesting because it contains the minimum number of elements that must be used in the simulation of the device under small-signal conditions and cold-FET bias. The 'T' equivalent circuit can be easily converted into a 'Π' equivalent circuit, with the same relaxation-time in all branches (see Fig. 2b). The 'Π' topology is closer to the ones typically employed in FET-type device simulation. This equivalent circuit is similar to that obtained by Hauser [3] after performing a small-signal analysis of a simplified FET structure. The model is also able to provide a consistent explanation for observed negative drain-to-source capacitance values [4].

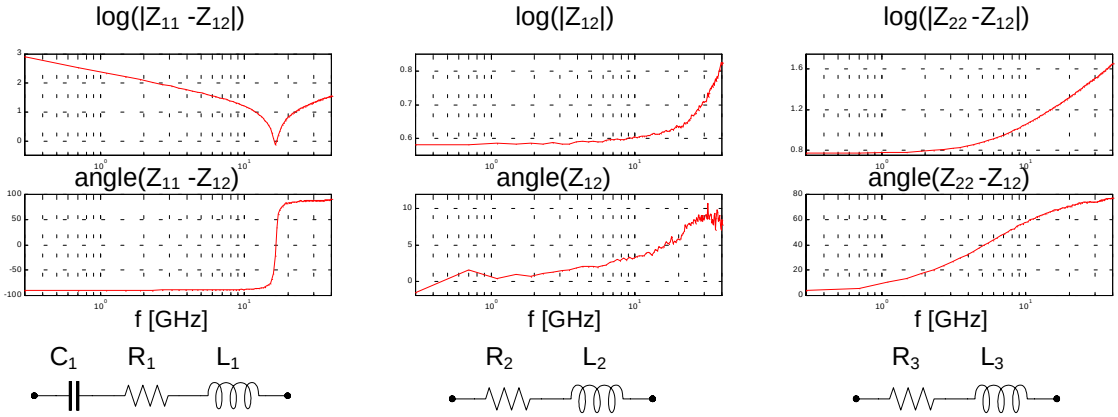

Fig.1.-Analysis of the frequency dependence of the measured Z-parameters for V_{GS}=0, V_{DS}=0, using Bode diagrams, and identification of the equivalent circuit elements that display this frequency performance.

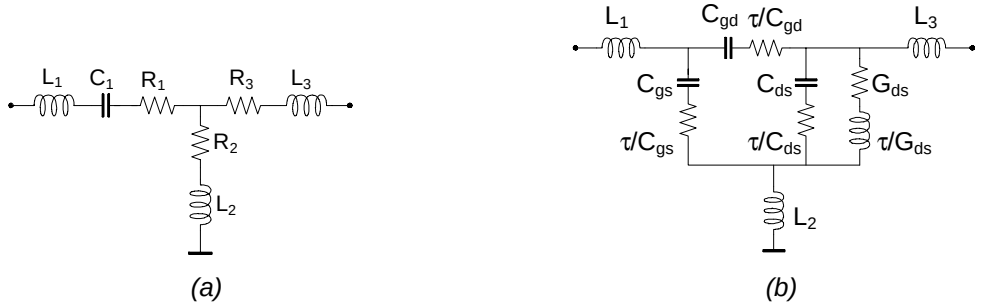

Fig.2.- Equivalent circuit for the 'cold-FET' under normal gate bias conditions. (a) 'T' topology, (b) 'Π' topology.

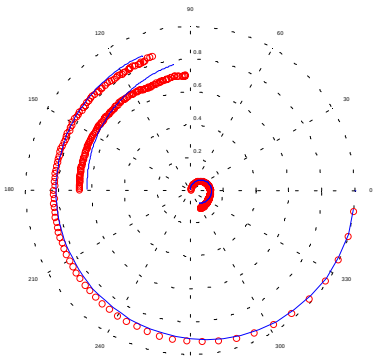

Fig.3.- Comparison between measured (°°°) and simulated (—) small-signal S-parameters (V_{GS}=0 V, V_{DS}=0 V) for a 4x100 µm MESFET device (1-40 GHz) using the equivalent circuit shown in Fig. 2a. (L_1=159 pH, C_1=618 fF, R_1=0.9 Ω, R_2=4.5 Ω, L_2=4.3 pH, R_3=7 Ω, L_3=164 pH).

NQS LARGE-SIGNAL MODEL

Equations 1-3 represent the charge and current non-linear functions for both gate and drain terminals. Total currents are considered to be the superposition of two components: one associated to capacitive effects (charge storage), the 'displacement' component, and the other associated to conduction phenomena in the device, the 'conduction' component. The time-constant τ is the relaxation-time that describes the non-quasi-static dynamics of the functions.

$$Q^{nqs}(t) = Q^{qs}[v_1(t), v_2(t)] - \tau \frac{d}{dt}[Q^{nqs}(t)] \quad (1)$$

$$i_{cond}^{nqs}(t) = I^{qs}[v_1(t), v_2(t)] - \tau \frac{d}{dt}[i_{cond}^{nqs}(t)] \quad (2)$$

$$i(t) = i_{cond}^{nqs}(t) + i_{disp}^{nqs}(t);\ i_{disp}^{nqs}(t) = \frac{dQ^{nqs}(t)}{dt} \quad (3)$$

It can be easily proved that, under small-signal conditions and for low gate voltages, this large-signal model reduces to the equivalent circuit shown in Fig.4. Notice that, for nonlinear consistency purposes, NQS effects have been also included in the definition of the transadmittance, $Y_{me} = (G_{me} - j\omega C_{me})/(1 + j\omega\tau)$. The suitability of a single relaxation-constant for use in all branches of the model, including the transadmittance, is confirmed by the fact that experiments with different relaxation-times happen to take similar values for these parameters in the analysed devices. It is evident from this figure that the equivalent circuit for cold-FET bias simulation must be the one previously deduced from the measurements (see Fig. 2.b).

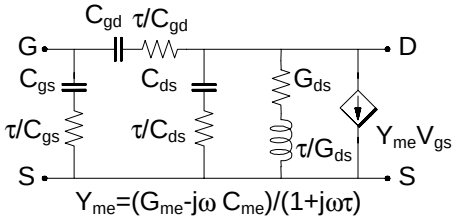

Fig.4.- Derived small-signal equivalent circuit.

If an optimal fitting for all bias conditions is required a more complete equivalent circuit must be used, where element values are obtained by means of an optimisation process, properly initialised with the available information from the former measurement analysis.

The process to reach the complete model is:

- Inclusion of propagation effects along the gate.

By using a distributed model, transverse propagation phenomena in the device can be evaluated. However, in the device under study these effects can be properly simulated by means of just a series resistor in the gate terminal. It represents one third of the total resistance along the gate electrode and it has been found to be needed for the correct device simulation [5].

- Addition of parasitic elements.

Taking into account the equivalence between the 'T' and the 'Π' topologies shown in Fig. 2, inductance values obtained from the previous measurement analysis can be considered as parasitic inductances. To improve the simulation performance at high frequencies (see Fig. 3), a more precise transmission line model for simulating the microstrip line environment has to be used in the definitive equivalent circuit. The values obtained for the total line inductances with this model are very close to those of the simplified 'T' model. Transmission line characteristic impedances are calculated by using an optimisation process for V_{GS}=0 V and V_{DS}=0 V. The values obtained for all parasitic elements at these bias conditions are kept fixed during the final optimisation process that provides the intrinsic element values for all bias conditions.

The resultant equivalent circuit is shown in Fig. 5. It is composed of the intrinsic model, incorporating propagation effects (R_{tg}), and the extrinsic model, which incorporates parasitic lossless transmission lines and the source inductance, related to the via hole connecting the source terminal to ground.

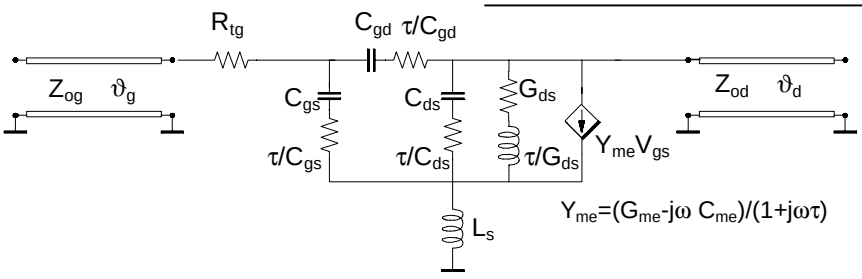

Fig.5.- Complete model including propagation and parasitic effects.

RESULTS

Results obtained for a 4x100 μm monolithic MESFET device, measured from 1 to 40 GHz, at different bias conditions, confirm the quality of the proposed extraction process and the small-signal NQS equivalent circuit. As parasitic elements are bias independent, only eight non-linear elements have to be considered in the final model. Fig. 6 illustrates the good fitting achieved with this model for normal operating bias conditions. Table I shows parasitic element values. Fig.7 presents the bias dependence of the intrinsic elements. The state functions that constitute the large-signal model can be later obtained from this bias dependence by taking into account that the small-signal capacitances and conductances are the partial derivatives of the quasi-static components of the charge and current functions described by Eq.1-2.

CONCLUSIONS

In this contribution a new non-quasi-static large-signal FET model, which introduces only one relaxation-time for both displacement and conduction current components, has been presented. The topology of the small-signal equivalent circuit has been obtained from the analysis of device measurements under cold-FET bias conditions, without any assumption regarding the non-linear model. It is considered that the proposed model provides simulation performance similar to conventional models, for both linear and non-linear working conditions, with a reduced number of non-linear elements. The proposed model can also explain certain anomalous phenomena such as negative values in the drain to source capacitance.

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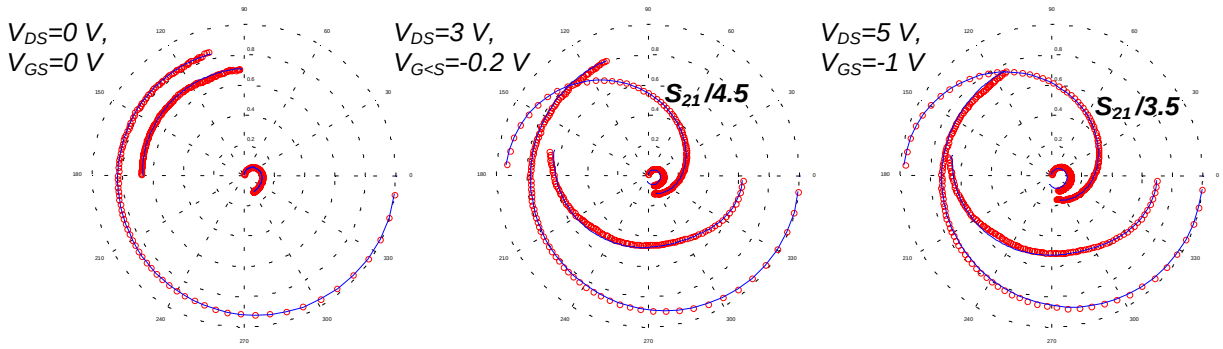

Fig.6.- Comparison between measured (°°°) and simulated (—) small-signal S-parameters for a 4x100 µm MESFET device (1-40 GHz).

Table I. Parasitic element values

Lg	Ld	Ls	Zog	Zod
154 pH	152 pH	6 pH	60 Ω	57 Ω

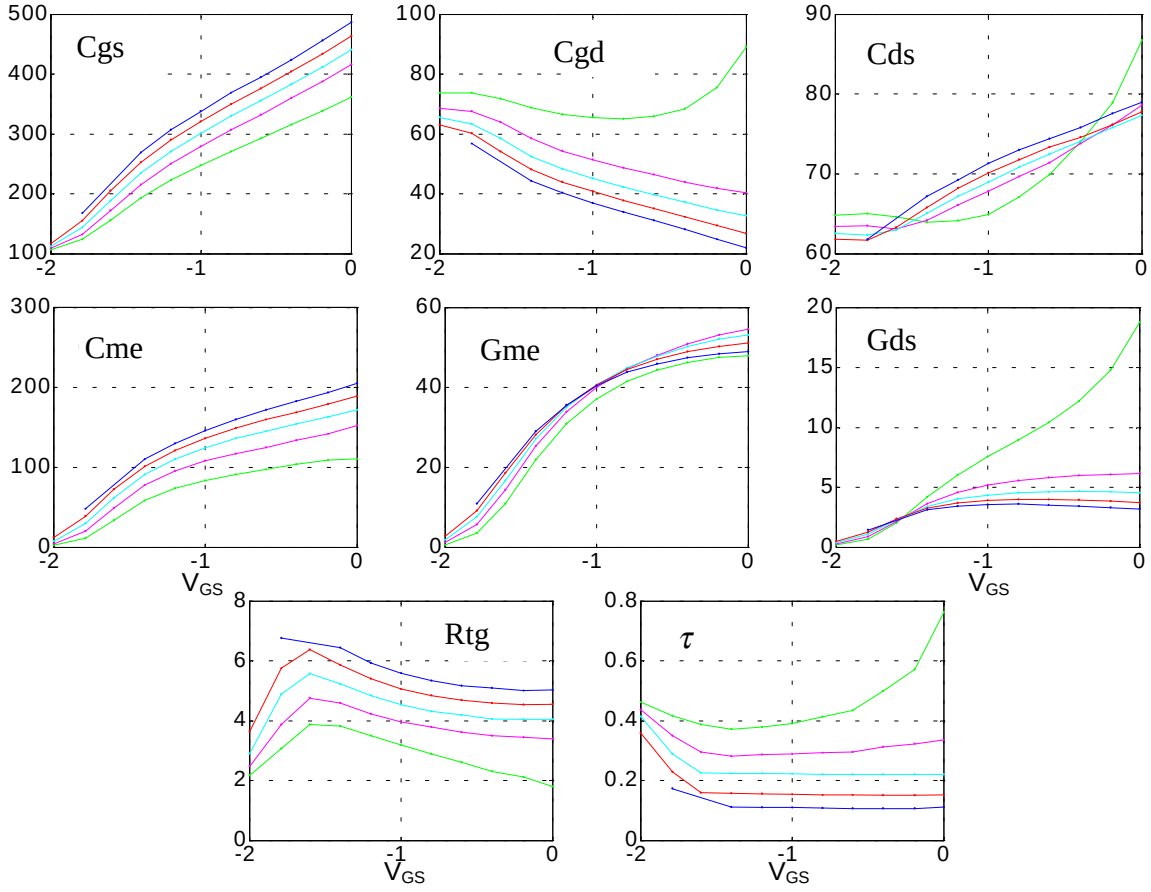

Fig.7.- Bias dependence of several model elements (V_{DS}= 1, 2, 3, 4, 5V).