COPLANAR MMICS - THE FUTURE FOR MASS PRODUCTION!

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INTRODUCTION

Coplanar line technology is now almost 30 years old and only these days, due to increasing volumes, it becomes more attractive for many MIC or MMIC designers. All the obvious advantages such as

- lower dispersion,
- lower coupling between adjacent lines
- reduced parasitic effects,
- compatibility with flip-chip
- potential low cost

have not convinced engineers to utilize this technique up to now. However, with increasing volumes and the availability of flip-chip, technology cost reduction has become such a major factor in MMICs, that during the MTT-S 98 managers from M/A-Com or other leading foundries have called coplanar MMICs the technology for the future. In the meantime it is clear that at least 20%, in some cases up to 40%, cost reduction can be achieved by using coplanar technology instead of microstrip line technology. Bumping technologies are available which even allow the design of power amplifiers in coplanar environment.

Ignoring these developments some designers still try to find arguments against coplanar circuit design where all the arguments have already been proven wrong in the past. The reason for this behavior is not clear to us but it is a fact, that every MMIC designer will be able to design a coplanar MMIC which works after the first design if he utilizes today's software tools, especially the COPLAN software from IMST. Coplanar circuits are continuously being demonstrated by research labs, e.g. FhG-IAF in Germany, NTT in Japan or IMST in Germany. Up to now, only a few companies like M/A-Com, Hughes or Terratec showed a serious interest in coplanar circuits. At this time, there are various possibilities to design coplanar circuits. These design solutions can be divided in the following way:

- analytical models (various),
- measured data base models (FhG-IAF),
- EM-solvers (various),
- COPLAN (IMST).

The hesitation of today´s engineers may be attributed to some rumors about coplanar circuits and also to the fact that, up to now, only one company, the IMST in this case, has developed a suitable library for CAD of coplanar MICs and MMICs. Various attempts of coplanar circuit designs were not successful but during the past years, more and more coplanar applications have been demonstrated. Thus, the interest in this technique is steadily increasing and there is a fair chance that coplanar circuit design will replace the common microstrip design during the next couple of years simply because coplanar circuits are cheaper, easier to design and today's state-of-the-art design tool COPLAN is by far superior in many aspects to comparable tools for microstrip design.

In this paper, a short overview of the evolution in coplanar line technique is given. Various rumors and facts on the coplanar line technique have been discussed in the past and will not be discussed here. The verification and capabilities of the software package COPLAN will be demonstrated together with a serious of application circuits, which range from simple functional blocks to complete systems, and which utilize the

coplanar line technique. Due to their very successful work and as a courtesy of FhG-IAF their method of modeling and designing coplanar circuits is being discussed as well.

EVOLUTION AND STATE-OF-THE-ART IN COPLANAR MMICS AND DESIGN TOOLS

Already in 1969, C.P Wen from David Sarnoff (today working at Hughes) proposed the application of Coplanar Lines (CPW) for MIC circuits [1]. In the 70s however, almost no publication on modeling coplanar elements or even circuit design utilizing such transmission lines can be found. Yet in the early 80th, some research groups e.g. Ghione et al [6] and Fouad-Hanna et al [3] started to develop models based on the conformal mapping technique for various types of coplanar lines. Almost at the same time, more rigorous numerical methods were developed by Itoh et al, Kathei et al or Jackson et al for the analysis of problems around coplanar lines. In 1986, CASCADE announced the first coplanar probe tips for On-Wafer measurements of MMICs and Riaziat et al from Varian [4] demonstrated a traveling wave amplifier from 2 GHz to 18 GHz which was designed utilizing CPW-lines. At that time, the modeling of microstrip elements was already quite sophisticated and MMIC designers started to become comfortable with the available models. More serious modeling of CPW-discontinuities started around 1988 and from the first published circuits and results it was soon believed that designing coplanar circuits is not a simple and straight forward task. The initial problems were caused by the fact that coplanar structures tend to generate the unwanted modes. At that time, tools and experience for suppressing these modes were not available and thus the designers of CPW circuits were not as successful as expected. In 1989, first investigations at the University of Duisburg demonstrated how to avoid such unwanted modes by applying an efficient air-bridge technology [8]. Various types of air-bridges were investigated and one of the key problems in designing CPW circuits is solved since then. However, even in 1990, the modeling of CPW elements had by far not reached the state-of-the-art compared to microstrip components. Most of the work on coplanar lines was on a very theoretical level and not suited for Computer Aided Circuit Design (CAD).

Especially the research labs NTT in Japan [7], FhG-IAF in Germany [15] and the IMST in Germany [16] successfully demonstrated many different applications utilizing coplanar line techniques. These applications range from broadband low frequency applications shown by NTT already in the 80s, over a commercially available CPW chip-set for 24 GHz applications introduced by the IMST to 77 GHz and 90 GHz demonstrators or total systems developed and manufactured by FhG-IAF in Freiburg. This shows that the coplanar line technique is well suited for low and high frequency applications as well. However, in the papers from MTT-S between 1992 and 1997 mostly high frequency, non volume oriented applications were presented.

Even though the bulk of the research on CPW is conducted in the USA, companies like Compact Software or HP-EEsof have not shown much interest in this development up to now. These companies totally failed with the introduction of a suitable design tool for coplanar circuits in their simulators up to now.

In 1987, Prof. Wolff from the University of Duisburg started his activities on coplanar lines [9], [10], [11]. Various activities were started one of which lead by the end of 1991, to a CAD oriented library for most coplanar structures. This comprehensive library is fast and accurate due to its 3D-Finite Difference kernel and the parametric description of each coplanar element. In the meantime, the original library was verified, enhanced and expanded at the IMST. Since the beginning of 1997 this library is available on the market and many applications from companies like Hughes, Alcatel, TRW, Dassault etc. have already proven the quality of this approach. During the last two years about 200 companies have approached IMST directly concerning coplanar lines and associated technologies.

TODAY'S DESIGN TOOLS FOR COPLANAR CIRCUITS

During the last years, a range of different design tools for coplanar circuits have been established. Some of the tools are dedicated to this problem others are general purpose solutions which have been applied to coplanar structures and designs. The types of available tools can be classified in the following groups:

- analytical models,
- measured data base models,
- EM-solvers,

- COPLAN.

The first three solutions are already well known from microstrip applications. Some of these tools are custom solutions and thus not suitable for commercialization. There are certainly advantages and disadvantages of each approach and a brief discussion will give an overview.

Analytical models:

There is only a limited number of models available at this time. The available models are not sufficient for complete, complex MMIC design. Air bridges or layouts are not supported by these models. The models are also limited in the range of application (e.g. substrate, dimensions, frequencies etc.). Analytical models are fast but don't consider mode conversions for instance. The accuracy of these models is only fair and can be problematic in critical cases.

Measured data base models:

These models are not commercially available and not technology independent. They are fast and accurate, but quite limited in geometry. Optimization is not possible and layout is typically not supported. This is a quite custom tailored solution which is very time consuming and expensive as well. However, the application of this technique has been demonstrated quite successfully by FhG-IAF and examples and some modeling background are shown below.

CPW MODELS BY FHG-IAF

For broadband circuits in microwave and optoelectronic communication systems as well as radar systems, models applicable from dc to over 100 GHz are required. Such broadband models have been developed at the IAF by extracting the data from coplanar test structures on GaAs [3]. The models are based on field-theoretical simulations of the basic coplanar transmission line properties as well as on on-wafer measurements, up to 120 GHz. For the characteristic impedances 30, 50 and 67 • , test structures of coplanar lines and elements like air bridges, corners, and probing pads were designed and processed. The test structure for coplanar corners is illustrated in Figure 2. A corner consists of two air bridges and a 90° bent section of transmission line. For the experimental analysis, 12, 24 and 36 corners as shown were connected in series.

The CPW elements are described by a physical transmission line model including frequency dependent values for the effective dielectric constant and the attenuation. The model parameters were extracted from measured S-parameters over the entire frequency range to 120 GHz. Thus, a CPW model library has been implemented in HP-MDS, which was the basis of various circuit designs. In Figure 3 and Figure 4, the performance of a W-band branch-line coupler is depicted, showing a good agreement between measured and simulated data from DC to 120 GHz.

In coplanar technology, small capacitances to ground can be realized without significant parasitic inductances, inherent to via holes in microstrip technology. By using capacitively loaded transmission lines, a chip size reduction of 60 % was achieved for a capacitively loaded branch-line coupler at 77 GHz, compared to a conventional branch-line coupler. This concept can also effectively be explored in matching networks for various circuit applications.

CIRCUIT EXAMPLES BY FHG-IAF

MMICs for FMCW systems require multiple active and passive circuits like oscillators, high gain and medium power amplifiers, mixers, and various couplers. For design verification of more complex chips, all crucial circuits were additionally realized as 2-port chips. Depending on the system specifications, bond wires of significant length, compared to the wavelength at the operating frequency, have to be accounted for on the chip design [20].

For a collision avoidance radar system at 77 GHz, an integrated transmitter and an integrated receiver front-end were developed and fabricated with the IAF PHEMT process on 3" s.i. GaAs wafers, where the T-shaped gatesof 0.15 µm length are defined by e-beam lithography [21], and with the Siemens HEMT process by use of optical stepper lithography [22].

A block diagram of the integrated transmitter is depicted in Figure 5. A total of 6 medium power amplifiers serve to deliver power from a coplanar VCO to the antenna (ANT), to the LO-port of the receiver (LO), and

to an oscillator control loop (LIN). A minimum RF-power of 10 mW has to be available at both the transmitter antenna port and the LO-port of the receiver. The power is split in two parts by means of a Wilkinson divider. Via a 10 dB coplanar coupled-line directional coupler, a small fraction of the input signal is fed to a linearizer loop for the frequency modulation of the RF-source. The measured output power at both the antenna- and LO-ports is 10 dBm, for an input power of 3 dBm, as can be seen in and saturates at 11 dBm for an input power of 6 dBm. The dissipated DC-power is 0.4 W. The chip, shown in the photograph of Figure 5, requires an area of only 3x2 mm².

The integrated receiver front-end incorporates a 4-stage LNA in the RF path, a balanced diode mixer, and a 2-stage LNA cascaded with a 2-stage MPA in the LO path. The gain in the RF path and in the LO path are 18 dB and 16 dB, respectively. The chip has a size of only 3 x 2 mm². For the diode mixer, an area saving reduced-size branch-line coupler with capacitively loaded l/8-lines is used to balance the LO- and RF-signals at the two diodes. The diodes are realized as HEMT-diodes. The conversion loss and the DSB noise figure of the mixer are 10 dB and 11 dB, respectively, for an LO-power of 8 dBm. The LO-to-RF-isolation is better than 16 dB. The overall conversion gain of the front-end is 9 dB for an LO-power of -10 dBm at 76.56 GHz and an RF-power of -40 dBm at 76.5 GHz. The total DC-power consumption is 0.4 W.

EM-solvers:

This solution is quite versatile and accurate. However, 2D simulations are not well suited and 3D simulations are typically too slow. Also, there is no efficient link between simulators and EM-solvers available which would allow circuit design and optimization. Automatic layout is also not possible. EM solvers can replace data base solutions and are process independent but they don't allow the efficient MMIC design. The design procedure is thus quite complex and very tedious.

COPLAN:

The COPLAN software from IMST combines accuracy, versatility, speed and CAD orientation in one tool. Automatic layout generation is also supported. Thus COPLAN is the only efficient alternative for designing high density coplanar circuits at this time which simply makes it to the state-of-the-art.

THEORETICAL BACKGROUND OF THE VERY EFFICIENT, 3D-FD SOFTWARE COPLAN

Coplanar lines and discontinuities show only marginal dispersion effects compared to microstrip lines e.g. Thus, a fast and accurate quasi-static 3D finite difference formulation is well suited to calculate three dimensional coplanar structures as depicted in Figure 8 for instance. In COPLAN, this approach is utilized and the boundary conditions are such that the top- bottom- and side walls are electrical walls, and the walls which are intersected by transmission lines are magnetic walls.

These assumptions seem to be restrictive, but they allow the calculation of almost all necessary structures since the ground dimensions are variable and even a finite metallisation thickness can be considered as well as various types of air bridges or package material on top of a MMIC for instance.

The procedure of calculating the electrical behavior of coplanar lines and discontinuities is as follows. The bounded region is first divided into elementary boxes using a three-dimensional non equidistant Cartesian grid. The electrical field (E) at any point **P** on the grid (see Figure 9) within the bounded region is calculated utilizing Laplace´s equation.

$$\left(\frac{\varepsilon_{r1}d+\varepsilon_{r2}c}{ab}+\frac{\varepsilon_{r1}}{d}+\frac{\varepsilon_{r2}}{c}+\frac{\varepsilon_{r1}d+\varepsilon_{r2}c}{ef}\right)+\Phi_P = \frac{\varepsilon_{r1}d+\varepsilon_{r2}c}{a+b}\cdot\left(\frac{\Phi_A}{a}+\frac{\Phi_B}{b}\right)+\frac{\varepsilon_{r2}}{c}\Phi_C+\frac{\varepsilon_{r1}}{d}\Phi_D+\frac{\varepsilon_{r1}d+\varepsilon_{r2}c}{e+f}+\left(\frac{\Phi_E}{e}+\frac{\Phi_F}{f}\right) \quad (1)$$

The "successive relaxation" method is used for solving the above given Laplace equation. In this method, the potential distribution inside the shielding can be determined starting with assumed potential values at all the grid points. After that, the new potential ϕ_{new} can be calculated by:

$$\Phi_{new} = \Phi_{old} - k * R \quad (2)$$

where R is the difference between ϕ_{old} and the value given in the first equation. The constant k, which determines the speed of convergence, must be chosen between $1<k<2$.

Calculating the electrical field at any grid point then leads to the charge distribution on conductors, which is used in order to determine the equivalent capacitance's. The equivalent inductance´s and calculated in a similar way using the surface current distribution on the conductors. Based on these results, the electromagnetic behavior of the structure is expressed in terms of equivalent circuits. Thus, the values of these equivalent circuit elements are the direct result of the numerical algorithms. Out of the equivalent circuits, the electrical behavior, e.g. the characteristic impedance Z_L, the effective dielectric constant ε_{reff}, or the S-parameters of these elements can be calculated. If we assume that the coplanar structures are lossless for the time being, the equivalent circuits consist only out of capacitance's and inductance's.

From the electrical field inside the shield, the total charge on the metallization (Q_{total}) and the charge per unit length on the connecting transmission lines (Q') are calculated. If the potential difference between the inner conductor and the ground plane is known to be V, the capacitance(s) (C_{eq}) associated to a given structure is then calculated as the difference between the total charge and the charge per unit length of the connecting transmission lines,

$$C_{eq} = (Q_{total} - l \cdot Q') / V, \tag{3}$$

where l is defined as the distance between the back-transformed reference planes of the discontinuity and the magnetic walls.

To determine the equivalent inductance's, a very efficient procedure was introduced by Naghed. The given geometry must be inverted, that means, the slots become metal and vice versa. Because of the fact that the slots in coplanar structures act as the magnetic wall, constant magnetic scalar potentials are assumed in the area of slots between the metallisation. After that, the magnetic scalar potential distribution can be calculated similar to the electrical potential given in the first equation. This is, once the magnetic field in the coplanar slots is known, the integral over the slot surface leads to the magnetic flux and the surface current distribution, which is then used for the calculation of the total inductance of the structure. The equivalent inductance (L_{eq}) is then calculated from the difference between the total inductance and the inductance per unit length multiplied by the geometrical length of the connected coplanar lines.

Conductor losses as well as dielectric losses are also considered in COPLAN. Dielectric losses are calculated from the comparison of the capacitance with and without the dielectric substrate. This way, the electrical field energy inside the substrate can be obtained. Under the assumption of low dielectric losses, an equivalent conductance will be calculated. The magnetic field distribution, which is calculated by the determination of equivalent inductance's, results in the surface current distribution on conductors. Under consideration of skin effect, the conductor losses are calculated from surface current distribution utilizing the disturbation method.

While Figure 10 shows the elements and air bridges of the smart library COPLAN, an overview of the today available elements is given in figure 20. At the current time, there are 16 standard elements and three types of air bridges in the COPLAN for Libra software available. Figure 26 shows the utilized element names, the physical geometry's and the applied electrical equivalent circuits as well. The complete 3D-simulation and foundry oriented layout for each structure is implemented in series IV from HP-EEsof. All of these elements were extensively verified by various companies and up to almost 70 GHz in the meantime. Some of the verification data is shown below.

Utilizing the smart library COPLAN, each dimension and other physical parameters can be varied within the software. Thus, circuit optimization utilizing field simulation becomes easily possible.

For different applications and various technologies there are three types of airbridges available. All bridges can automatically be applied to the discontinuities and are then included in the simulation and layout as well. Figure 1 shows the three air bridge types and the dimensions which can be modified. Any modification will automatically be considered in the simulation and related layouts. Two different metal layers are utilized for the air bridges. In the meantime it is also possible to allow dielectric material between the two metal layers. This is quite important for foundries like GEC-Marconi or Hughes for instance.

INTEGRATION OF THE SMART COPLAN FOR LIBRA LIBRARY INTO SERIES IV

The ***COPLAN for Libra*** consists of coplanar waveguide models and special data items. Each model represents a specific coplanar structure like a T-junction, bends etc. In order to reduce the number of input parameters for such a model, several data items were introduced. These data items have a similar function as the well known data items like **MSUB** item of the microstrip library or the general **UNIT** data-item. Many of the necessary input parameters are common for a lot of elements in a given design. Therefore, they are stored in dedicated data items. For example, a 50 Ohm line is defined by the line width w and the slot s. Normally all 50 Ohm lines in a design have the same values „w" and „s". This data is stored in the item C_LINTYP and can be referred by all modules without the need to enter the information again and again. The same is true for example for the bridge configurations and the grids.

In addition, the library supports process-related layout generation. This means, all necessary information (oversizes, layer configurations, etc.) are stored in two further data items. Technological data such as material constants of layers (dielectric constants, loss factors and resistivity) and layer height are maintained in the C_TECH data item. A second data item C_LAYER is intended for layer data such as layer number and oversize of each layer.

There is a standard foundry set-up available which allows the user to adjust several process specific parameters. Nevertheless, further adaptations to other foundries may be necessary and are also available as a special service. It is important to mention that *COPLAN for Libra* supports the use of several foundries and processes simultaneously. Using the quasi-static finite difference approach, an equivalent circuit is computed during a frequency independent pre-analysis. The number of iterations, the residual error and the name of the model are displayed inside the standard Libra *Status Window*. Input parameters and the results are stored in a data base file. During simulator startup, this file is loaded into memory and works then like a cache. Based on these previous results, a frequency dependent analysis is started and the S-parameters of all coplanar structures are calculated.

A smart cache memory management is implemented in order to speed up the statistical analysis and optimization process. The calculated parameters of coplanar elements are stored in this cache during the first analysis run and will then be updated, if the element data are changed.

The ***COPLAN for Libra*** comes along with the following data-items:

C_SUB	Substrate definition for coplanar structures
C_GRID	Definition of grid and shielding sizes for finite difference approach
C_LINTYP	Definition of cross-sectional dimensions of coplanar line
C_AIRTYP	Definition of air bridge parameters
C_PROCES	Foundry selection for layout generation and process-related simulation
C_TECH	Definition of technological data for selected Foundry
C_LAYER	Definition of layer data for selected Foundry

Table 2: Data items of COPLAN for integration within series IV from HP-EEsof

The calculated parameters are also stored in binary look up tables. These files contain the equivalent circuit parameters of all coplanar elements and characteristic line parameters of coplanar wave guides.

The *COPLAN for Libra* can simply be accessed by selecting the palette „Coplanar Elements" in the schematic and layout windows, as shown in Figure 26. In the case of defaults definitions there is a palette in the defaults window as well.

The complete schematic, simulation and layout library is thus seamlessly integrated into series IV and may be utilized as simple as resistors or other lumped elements. This approach offers certainly linear-, nonlinear simulations and circuit optimization as well.

Figure 12 depicts the schematic of a filter circuit which was designed utilizing COPLAN and Figure 13 shows the corresponding layout which is automatically extracted from the schematic. It is also possible however, that designers start from layouts or modify dimensions within the layout presentation.

VERIFICATION OF THE SMART LIBRARY COPLAN FOR LIBRA

The verification of COPLAN for Libra was started in 1992 by launching the ESPRIT-CLASSIC project. During this project, which lasted for three years, many passive coplanar structures were fabricated and measured up to 67 GHz. Finally the measurements were compared to simulations utilizing COPLAN for Libra. For all in Figure 26 depicted elements, these verifications showed superb results. Thus, the library was sufficiently verified already at this time. In the meantime however, many companies like Alcatel, Dassault, Hughes, Ricoh or research labs like IMEC or FhG-IAF have also produced test structures and verified measurements against simulations. Up to now there is not a single company which reported poor accuracy of the software. Since the library was also verified by extensive circuit designs, some results of this work will be shown as well.

The following examples give a flavor of some verification examples conducted at the IMST. All shown structures were realized on GaAs with a conventional MMIC technology. No extra layers or special design rules were required. First of all, loss simulations and characteristic line behavior was investigated. Various structures for impedance's between 30 Ω and 80 Ω were realized and evaluated.

Figure 14 shows results from a 25 mm long line on GaAs. Return loss and insertion loss were simulated almost in perfect agreement for magnitude and phase as well. Measurements and simulated data of a double step structure are depicted in Figure 15. A more complex structure, consisting out of 24 airbridges, 12 bends and the connecting lines is demonstrated in Figure 16. This structure generates resonance's already at low frequencies. A very strong resonance can be detected at 30 GHz. All resonance's are simulated perfectly in frequency, magnitudes and phases as well.

In the cases of tee's and crosses various structures were also evaluated. All these structures are two port structures as can bee seen in Figure 17

The remaining parts typically connect to transmission lines which terminate into opens or shorts. Thus, resonance's must occur as function of „n*λ/4" (n=1,2...) of these stubs.

Figure 17 depicts such data from measurements and corresponding simulations. Only at 50 GHz a small deviation between the two data sets can be found. This small discrepancy is due to increasing dispersion at such high frequencies. For the shown examples the dispersion was not considered in the simulation. It can be seen however, that even the phase behavior can be predicted with excellent accuracy.

Lumped elements like rectangular inductors, interdigital capacitors, thin film resistors of MIC-capacitors were also evaluated during ESPRIT-CLASSIC. In Figure 18, data from a 3.5 turn inductor is depicted. In this case, the simulation is very good up to 30 GHz and degrades only marginally at higher frequencies. As last example in this paper, data of an MIM-capacitor is shown in Figure 19. As in the other cases, the simulated data is in very good agreement with the measured data.

APPLICATIONS REALIZED BY UTILIZING COPLAN

In the meantime, COPLAN users can be found in almost every country. Thus, current applications cover almost every modern system. Unfortunately most of these applications are not accessible for public and will only find their way to publications after some time. At the IMST however, MMIC and MIC design activities are ongoing and some results of this work can be presented here.

The applications at the IMST range from 900 MHz highly linear base station components over a 2.4 GHz low power radio link for transponders, 5.8 GHz oscillators, various frequency up- and down-converters, 24 GHz radar sensors, TxRx-modules for satellite links at 20 GHz and 30 GHz, components for 38 point to point systems and finally, 77 GHz components for today's modern ACC-systems. All circuits for these applications were realized in coplanar technique utilizing HEMT or MESFET technologies: Some of the circuits designed with COPLAN are presented in this chapter. As first example, an oscillator for 29 GHz is presented. This circuit, shown in Figure 20, was realized with a conventional 0.5 µm MESFET process and features 5 dBm output power.

It is a two stage design with active loads and lumped inductors for biasing. The resonator is realized on-chip by a combination of inductors and a voltage dependent capacitor (diode). The chip size is 1.24 mm^2. The application for this 29 GHz oscillator is a satellite based communication systems. In the second example, Figure 21, an oscillator for 38 GHz is depicted.

This module is based on a 0.25 µm HEMT process and was designed in the frame of an ESPRIT project together with the Daimler Benz GaAs-foundry. This 1.23 mm by 0.75 mm single stage oscillator is utilizing an active load and an on-chip resonator.

The third example features a 5 GHz oscillator for a distance measurement system. In this case, a three stage design was required to reduce the load pulling of the oscillator. The output power is 10 dBm at the main port and 0 dBm at the PLL port. The Daimler Benz 0.5 µm MESFET process was utilized for this chip. Active biasing in combination with inductors and capacitors is utilized for this chip. This oscillator can be tuned over more than 4 GHz bandwidth and is available with on-chip and external varactor elements.

All presented oscillators were fully simulated by utilizing HP-EEsofs series IV in combination with COPLAN. Utilizing a nonlinear model for the active devices, the output power and oscillation frequency could accurately be predicted prior to fabrication. The fourth example in this little series shows a broadband SPDT switch with a TTL compatible driver (Figure 23).

The input and output of this switch is matched to 50 Ohm and the operating frequency band ranges from about 1 GHz to 12 GHz. Over the whole frequency band the return loss is better than 10 dB and the isolation of this switch is better than 25 dB (>40 dB @ 2 GHz) with about 1.5 dB insertion loss. This 0.2 mm^2 circuit was realized within a BMBF-Project utilizing a 0.5 µm MESFET process and the COPLAN software for simulation and prediction.

Within the ESPRIT-CLASSIC project, various MMICs were designed at the IMST. The applications for these circuits were ACC systems and MBS. These are high frequency applications well suited for coplanar technology. From the various components designed at the IMST during this project an up-converter from about 6 GHz to 63 GHz is shown in Figure 24. The LO-frequency is 56.8 GHz, achieved conversion gain is 11 dB and the chip size about 2.1 mm^2. This active two stage mixer, with adder stage at the input, was realized utilizing the Thomson and Daimler Benz 0.15 µm HEMT process. Both signals, the LO- and the input RF-signal are applied at the gate of the mixing device. All ports are matched to 50 Ohm at the corresponding frequency. At the RF-port (5.2 GHz to 7.2 GHz) the matching was achieved by a combination of lumped inductors and MIM-capacitors. This circuit was fully simulated within series IV utilizing COPLAN and a nonlinear model for the HEMTs.

In Figure 25, a 2.4 GHz amplifier with three output ports is depicted. This is a circuit with six integrated active devices featuring additional active loads, rectangular inductors and MIM-capacitors for matching purposes. This amplifier has a chip size of 5.23 mm^2 and offers two 10 dBm and one 0 dBm output ports. The input is matched to the corresponding oscillator with a low impedance. The devices in this circuit were selected for low power applications. Biasing is thus at low currents with about 10 dB gain per stage. A conventional 0.5 µm MESFET process was utilized for this circuit.

SUMMARY

In this paper, an overview of publications on coplanar technology over the last 30 years was given. The COPLAN software, based on an efficient 3D-FD calculation was introduced. The integration in series IV from HP-EEsof, a comprehensive verification procedure and various applications designed utilizing COPLAN are shown as well. The method of generating measurement based models was shown using data and very impressive results from FhG-IAF. This data was provided as a courtesy of FhG-IAF. All shown circuits were realized and measured data compares well with simulation.

In the past, coplanar circuit designs were applied to circuits for 1 GHz as well as 100 GHz. Many successful designs were presented and there is no valid reason against coplanar circuit design these days. Coplanar circuits can be interfaced with microstrip environments and co-integration of microstrip and coplanar MMICs is possible. Even high power applications, utilizing coplanar circuit techniques and flip-chip mounting have been demonstrated. Due to required price reduction in todays and tomorrows applications

CPW-MMICs will become one key technology. Chip cost reduction of up to 40% is possible by using coplanar technology.

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FIGURES

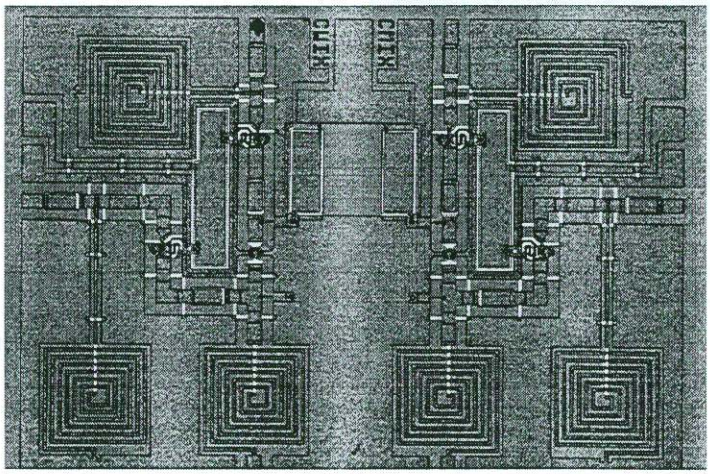


Figure 1: Coplanar IQ-demodulator for 2.4 GHz

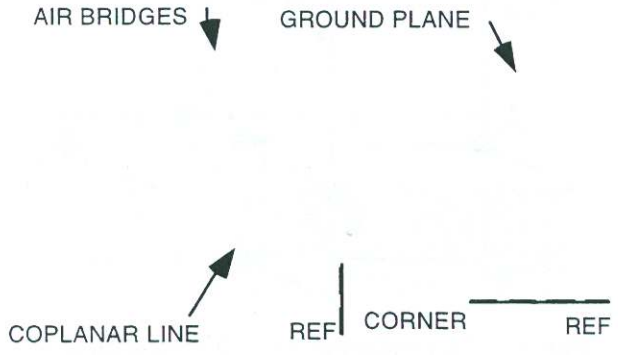


Figure 2: A section of the test structure for coplanar 90o corners.

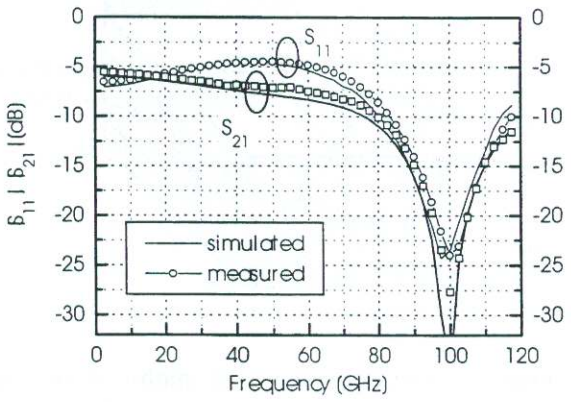


Figure 3: Measured and simulated return loss S_{11} and isolation S_{21} for a branch-line coupler

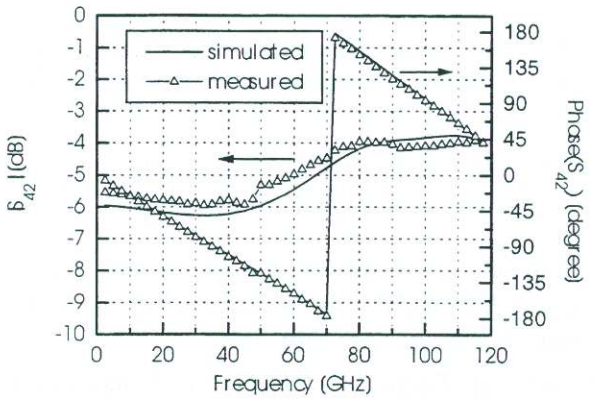


Figure 4: Measured and simulated insertion loss in amplitude and phase for branch-line coupler.

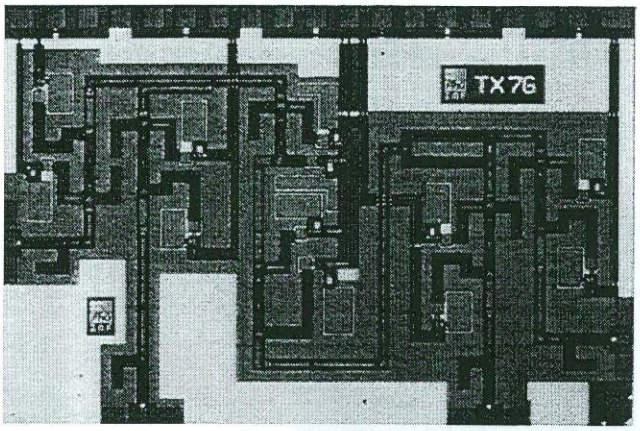


Figure 6: Chip photograph of coplanar 76 GHz transmitter MMIC (3x2 mm²).

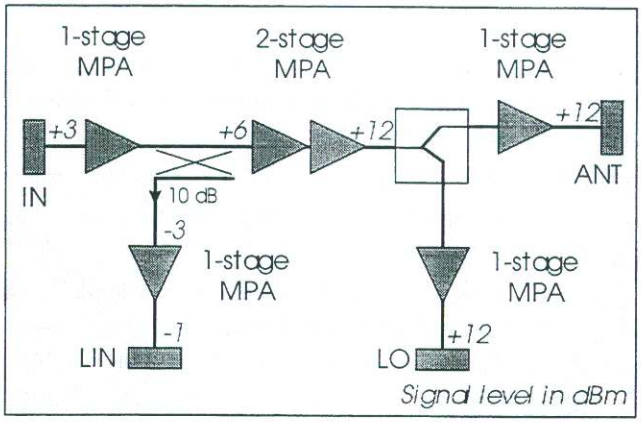


Figure 5: Block diagram of integrated 76 GHz transmitter MMIC.

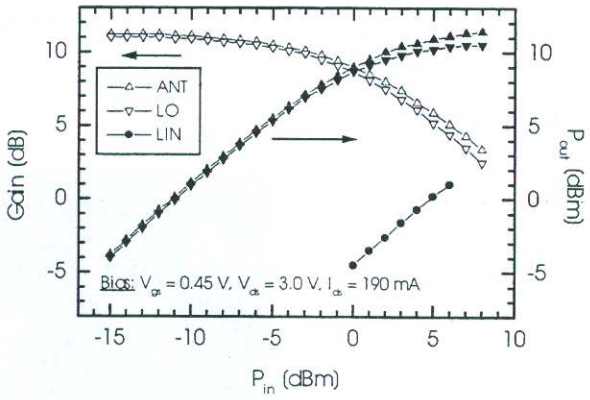


Figure 7: Output power of transmitter MMIC at the three output ports vs. input power

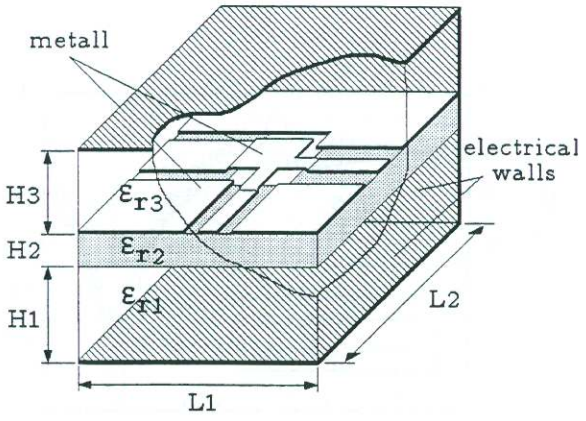


Figure 8: Three dimensional multi-layered and shielded structure containing coplanar T-junction.

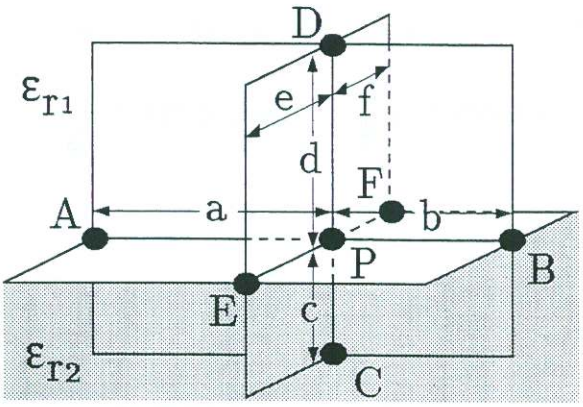


Figure 9: Elementary box for the calculation of the electrical field at point P.

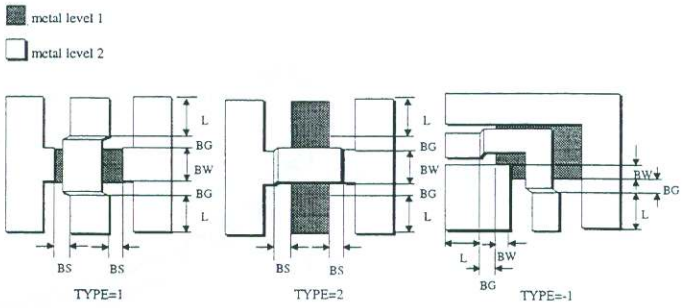


Figure 10: Types of air bridges in the COPLAN software

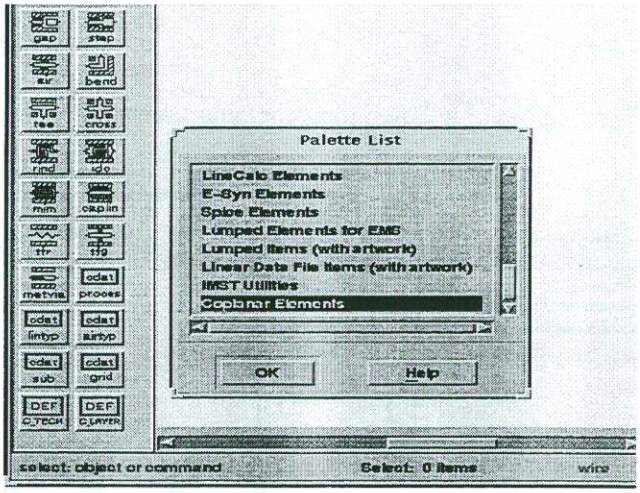


Figure 11: Selection of COPLAN for Libra library palette in schematic entry window

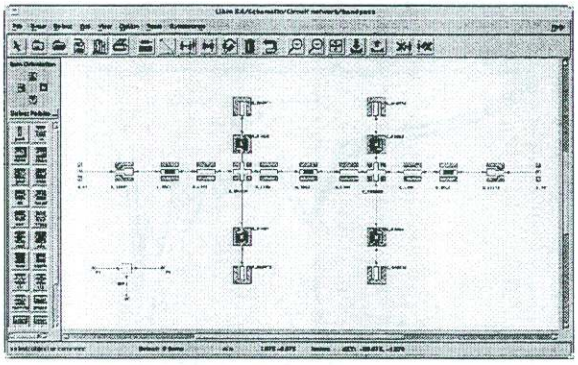


Figure 12: Schematic of a coplanar filter structure within series IV

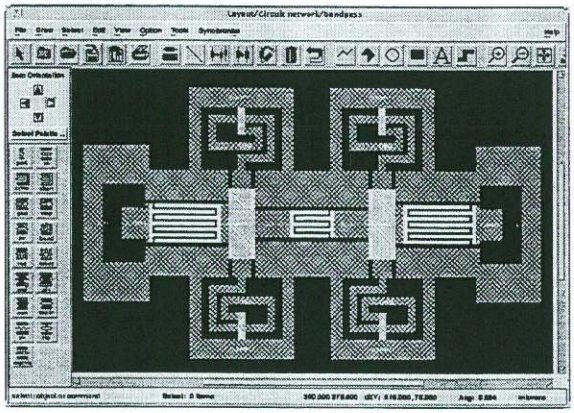
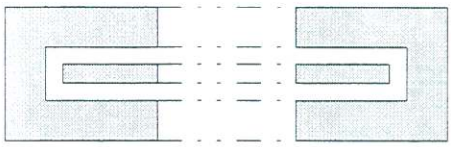


Figure 13: Layout of a coplanar filter structure within series IV.



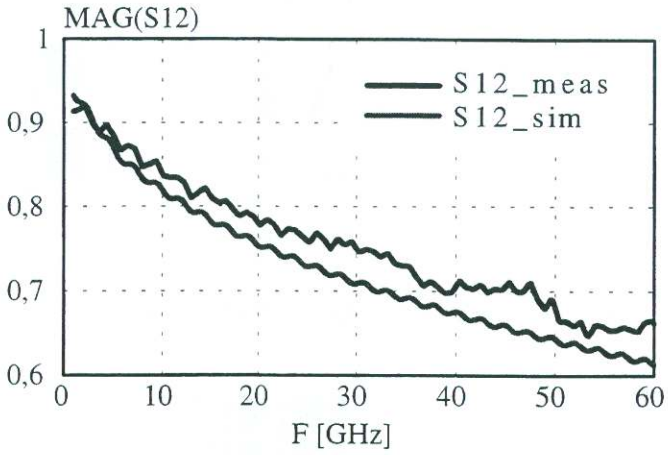
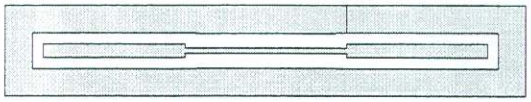


Figure 14: Verification of a 25mm long coplanar transmission line on GaAs



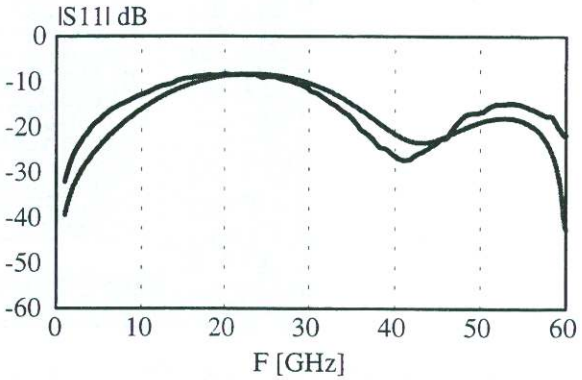
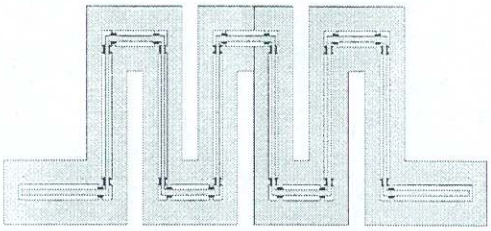


Figure 15: Verification of a double step structure on GaAs



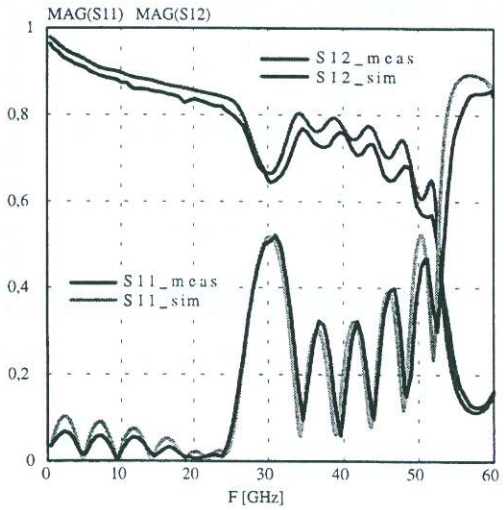


Figure 16: Verification of a meander structure with 12 bends on GaAs

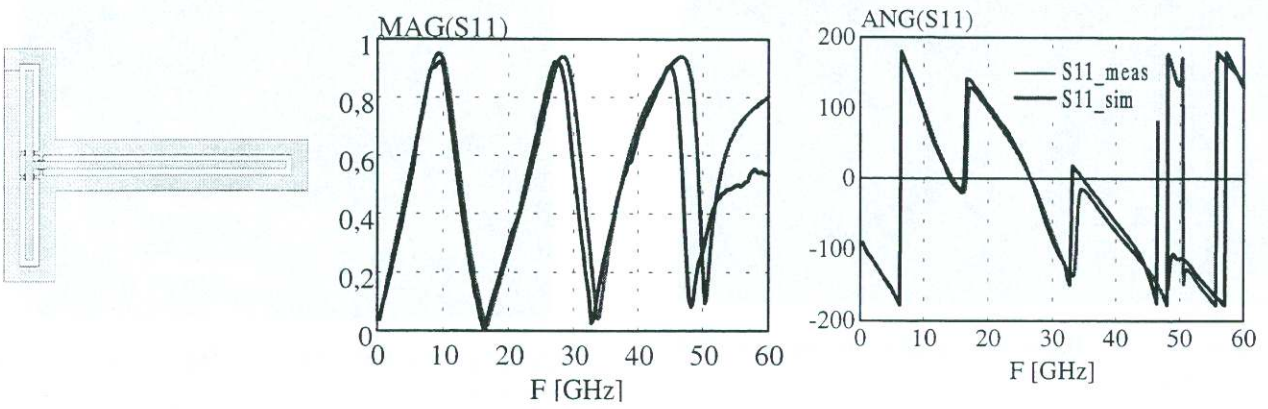


Figure 17: Verification of a resonant TEE-structure on GaAs

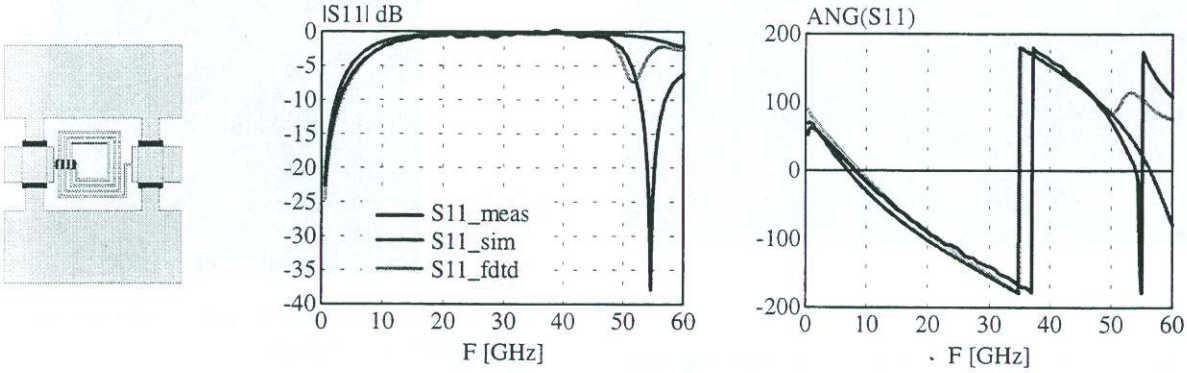


Figure 18: Verification of a 3.5 turn rectangular inductor on GaAs

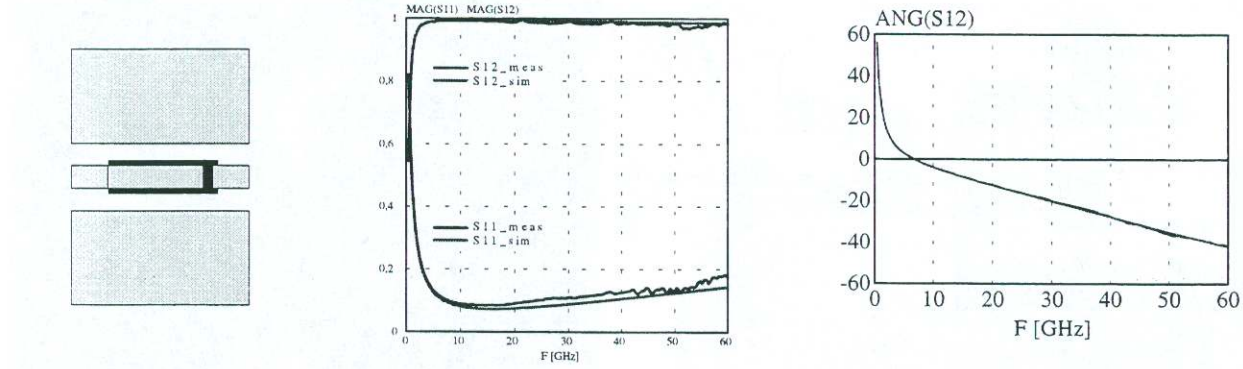


Figure 19: Verification of an MIM-capacitor on GaAs

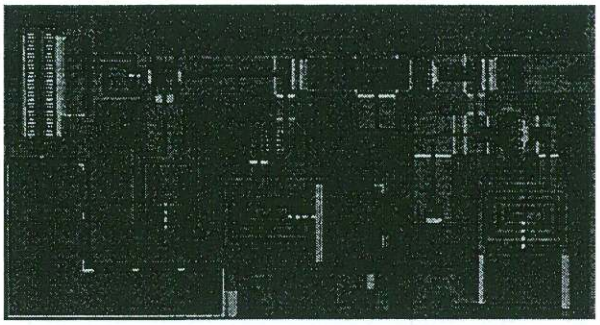


Figure 20: Oszillator for 29 GHz in coplanar line technique

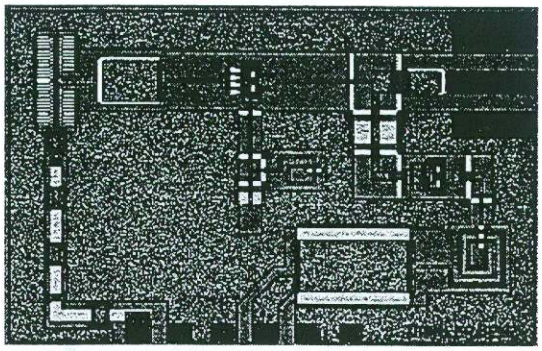


Figure 21: Oscillator for 38 GHz in coplanar line technique

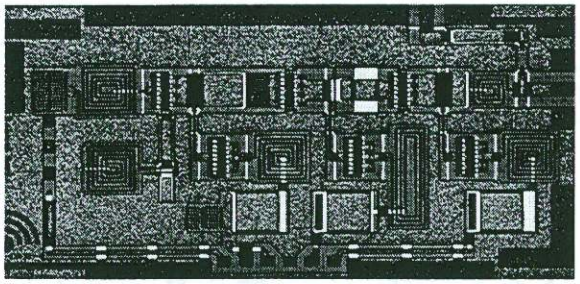


Figure 22: Oscillator for 5 GHz in coplanar line technique

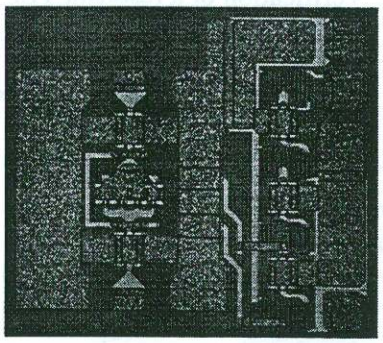


Figure 23: Switch for 1 GHz to 10 GHz in coplanar line technique

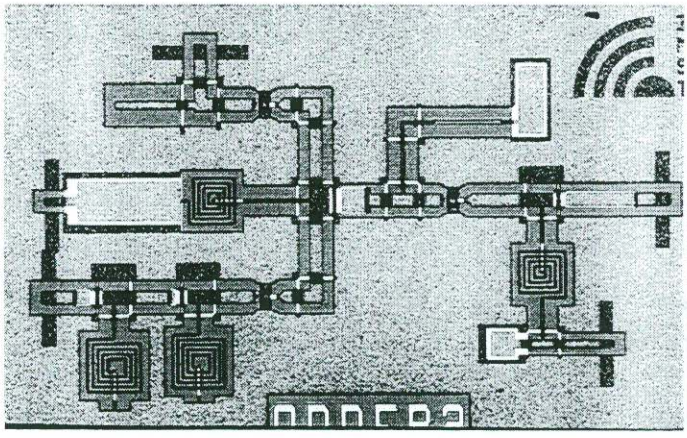


Figure 24: Up-converter for 6GHz to 60 GHz on GaAs

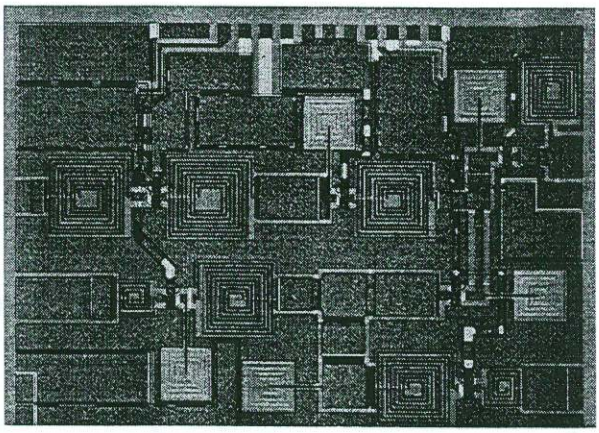


Figure 25: Amplifier for 2.4 GHz with three output ports

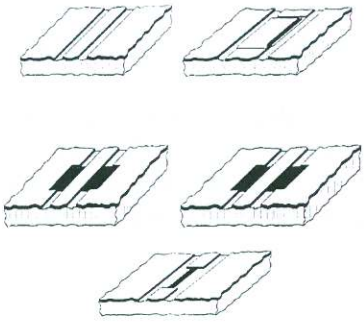
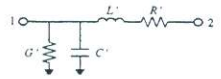
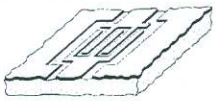
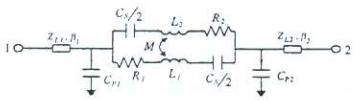
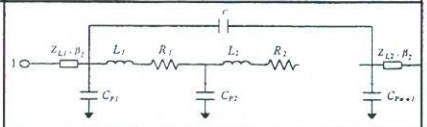
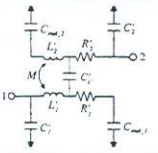
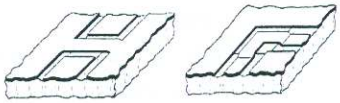
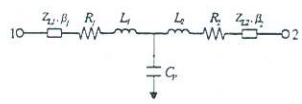
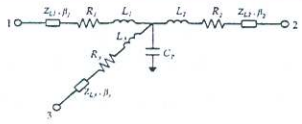
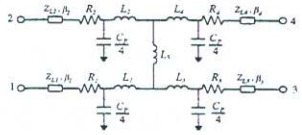
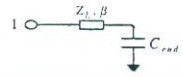
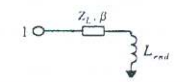
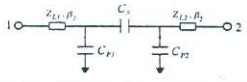
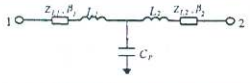
Name	Physical	Equivalent Circuit
C_LIN Coplanar Transmission Line **C_METVIA** CPW Inter Metal Via (no Step) **C_TFG** CPW Thin Film Resistor to Gnd **C_CAPLIN** CPW MIM-Capacitor to Gnd **C_TFR** Coplanar Thinfilm Resistor		
C_IDC Coplanar Interdigital Capacitor		
C_RIND Coplanar Rectangular Inductor		
C_MIM Coplanar MIM-Capacitor		
C_AIR Coplanar Airbridge **C_BEND** Coplanar Bend		
C_TEE Coplanar Tee-Junction		
C_CROSS Coplanar Cross-Junction		
C_OPEN Coplanar Open		
C_SHORT Coplanar Short		
C_GAP Coplanar Gap		
C_STEP Coplanar Step		

Figure 26: Coplanar elements of the smart COPLAN for Libra software