Equivalent Circuit of FET Active Loads for Non-Linear Applications

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ABSTRACT

FET-based active loads have been fabricated and tested, and their equivalent circuit extracted for linear and non-linear applications. The extraction procedure requires the availability of an equivalent three-terminal FET device for accurate model identification. The model proves to be easy to extract, accurate and general.

INTRODUCTION

Active devices are increasingly used as a replacement for passive elements in the design of monolithic microwave integrated circuits, with the advantage of smaller dimensions and better reproducibility. Active loads, i.e. transistors with gate and source terminals connected together (fig.1a), belong to this category. For small-signal applications the loads can be modelled by means of any linear representation (e.g. S-parameters), measured at all quiescent voltages of interest. In the case of large-signal applications however a non-linear model must be available. A natural choice is the standard equivalent-circuit model of an FET device, with the gate and source electrodes suitably connected. Since the elements of the equivalent circuit are not easily extracted from active load measurements only, an identical FET in a standard three-terminal (two-port) configuration has been fabricated on the same wafer (fig.1b). A simple connection of the gate and source pins of a standard equivalent circuit (e.g. [1, 2]) does not give satisfactory results; an analysis of the measurements shows that the different lay-out of the pad connections requires a radical modification of the parasitics, while the intrinsic part of the device must remain the same. A straightforward and effective procedure for the derivation of the active load model from the three-terminal one has been found and the model has proven to be quite accurate.

THE MODELLING PROCEDURE

As a first step a bias-dependent small-signal model of the three-terminal (standard) device is extracted. The device is a 0.5-µm gate, 200-µm periphery implanted MESFET from the Alenia foundry. The device's S-parameters are measured at several bias points, in our case in the range $V_{gs} = +0.5 \div -4.0$ V , $V_{ds} = 0.0 \div 5.0$ V for complete characterisation, with a few additional 'cold-FET' bias points ($V_{ds} = 0$ V, $V_{gs} > V_{bi}$) for accurate parasitic evaluation [3]. The extraction is pretty standard, and yields a linear bias-dependent model (fig.2a) that forms the basis of our procedure; in the figure the bias-dependent (intrinsic) elements are enclosed within the dashed line.

The equivalent circuit of the active load (fig.2b) is now extracted. As stated above, the intrinsic part of the circuit is the same (in black in the figure), and only the new parasitics (in grey) must be evaluated. This is done at a single bias point; in our case V_{ds} = 3 V. Parasitic capacitances are evaluated first. The gate-to-ground parasitic capacitance C_{pg0} has a different value from that of the three-terminal FET (C_{pg}) because of the different gate-source metallisation, and must be evaluated. The total drain capacitance C_{pd} on the other hand has not changed, but it is now splitted into two parts: a drain-to-source (C_{pds}) and a drain-to-ground (C_{pd0}) capacitance (fig.3a). The gate-to-ground (C_{pg0}) and drain-to-ground (C_{pd0}) capacitances are easily evaluated from the imaginary parts of the admittance matrix at low frequency (<10 GHz), since (neglecting L_{g1} and L_{d1}):

$$Y_{11} \cong Y_{al} + \frac{1}{R_{g0}} + j\omega C_{pg0} \qquad Y_{12} = Y_{21} \cong -Y_{al} \qquad Y_{22} \cong Y_{al} + \frac{1}{R_{d0}} + j\omega C_{pd0}$$

where Y_{al} is the admittance of the inner active load (fig.3b). The value of the drain-to-source parasitic capacitance C_{pds} is immediately computed by subtraction: $C_{pds} = C_{pd} - C_{pd0}$.
Next, parasitic resistances to ground R_{g0} and R_{d0} , representing the conductance of the substrate, are easily evaluated from the real parts of the admittance matrix for $\omega \rightarrow 0$, in particular from $Re[Y_{11}]$ and $Re[Y_{22}]$ (fig.4). Finally, the parasitic inductances L_{g1}, L_{g2}, L_{d1} and L_{d2} are similarly obtained by fitting the same real parts of the admittance matrix, but in the medium-high frequency range (fig.5). The parasitic elements are therefore all found at a single bias point with simple evaluation or fitting, and the equivalent circuit is now complete.

RESULTS AND CONCLUSIONS

The accuracy of the model can be tested at bias points different from the one used for parasitic evaluation. For instance, data at $V_{ds} = 0$ is show in fig. 6a and 6b, where the values of the intrinsic elements have been taken from the three-terminal device model at $V_{gs} = 0$ and $V_{ds} = 0$. The good agreement confirms that the extraction is sound and yields reliable results. Similar accuracy of simulation is obtained at all other bias points ($V_{ds} = 0 \div 5$ V).
In conclusion, the structure of the equivalent circuit of an active load and a simple and effective extraction procedure have been established, opening the way to linear and non-linear CAD applications in MMIC's.

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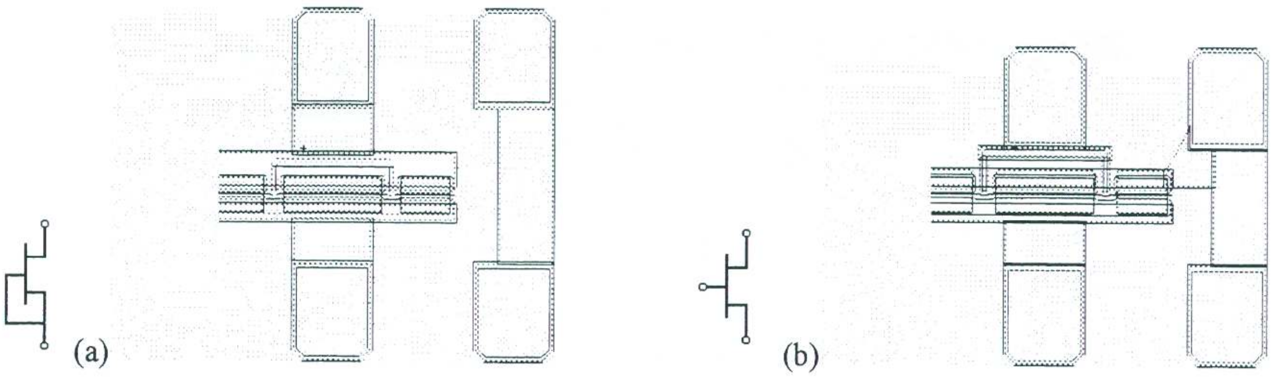

Fig.1 : Layout of the active load (a) and of the three-terminal transistor (b)

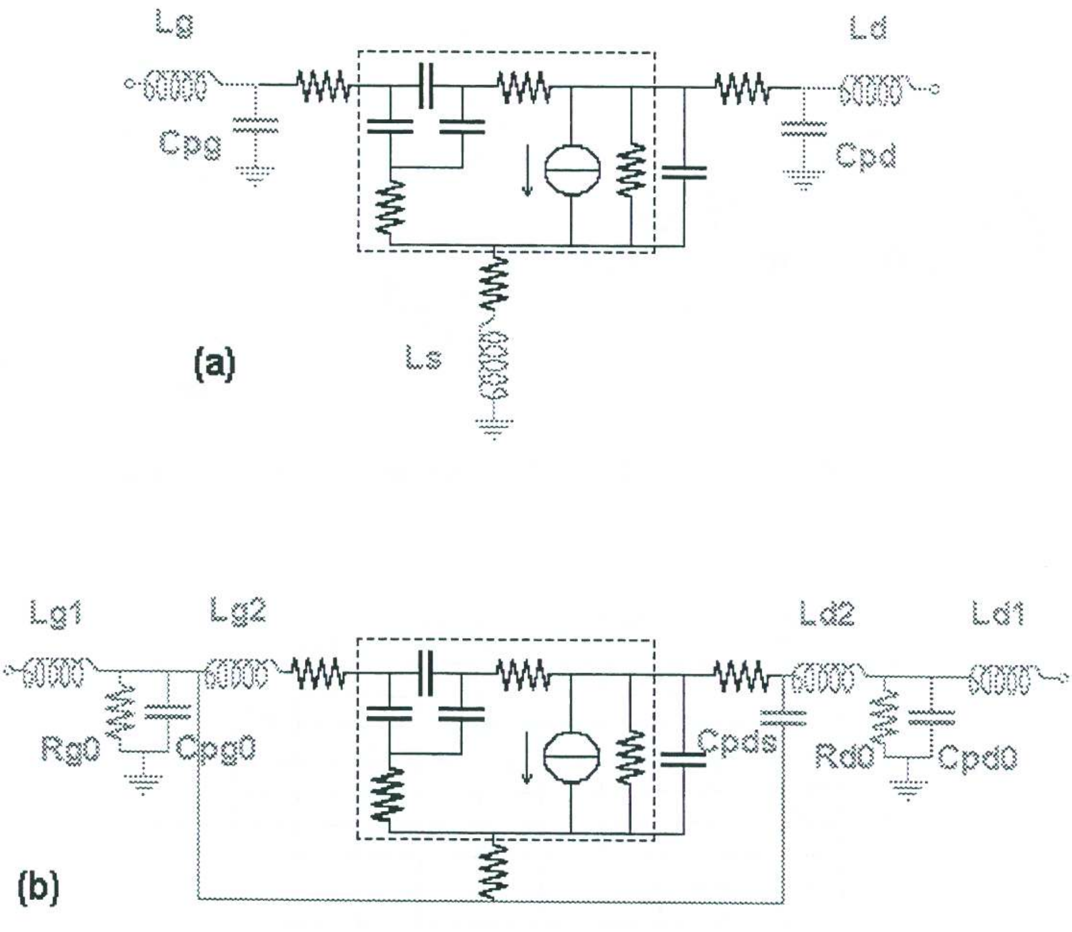

Fig.2 - The equivalent circuit of a three-terminal FET (a) and the modified equivalent circuit for an active load (gate and source terminals connected) (b); in black, unchanged elements.

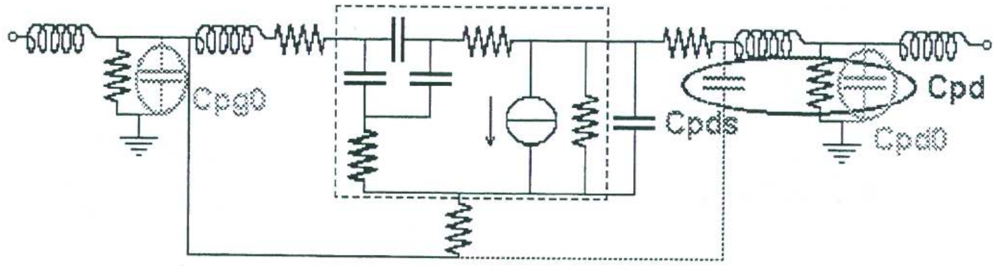

Fig.3a – Low-frequency approximation of the active load with parasitic capacitances to ground

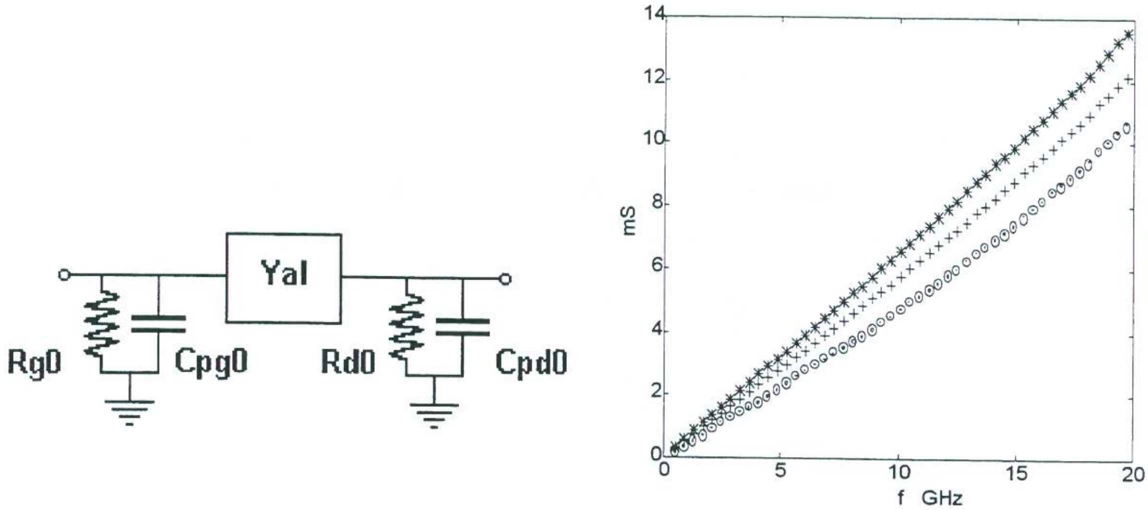

Fig.3b – Imaginary parts of the admittance matrix of the active load

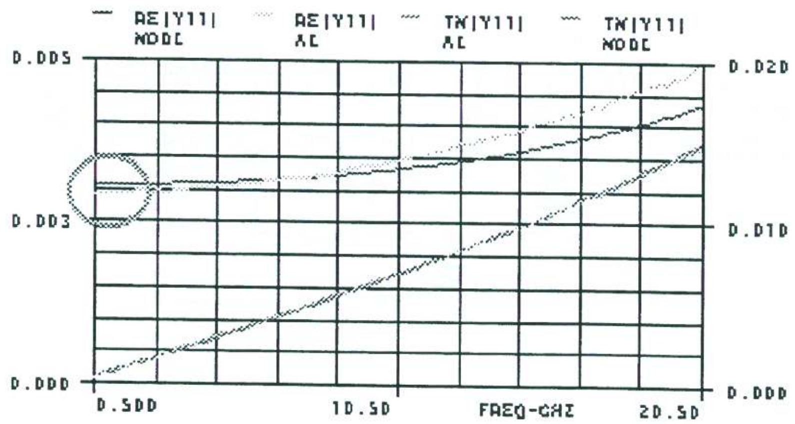

Fig.4 – Fit of Re[Y_{11}] for the evaluation of parasitic resistances to ground R_{g0} and R_{d0}

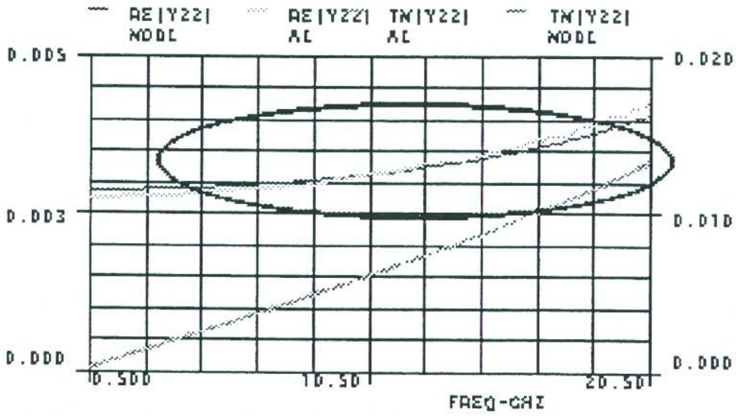

Fig.5 – Fit of Re[Y_{22}] for the evaluation of parasitic inductances L_{g1}, L_{g2}, L_{d1} and L_{d2}

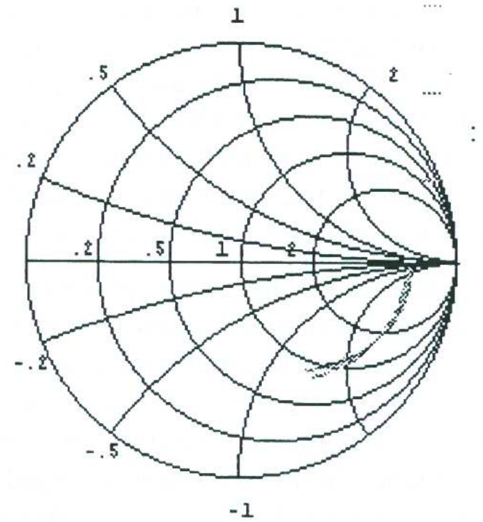

Fig.6a – Measured and modelled S_{11} and S_{22} of the active load at V_{ds} = 0 V

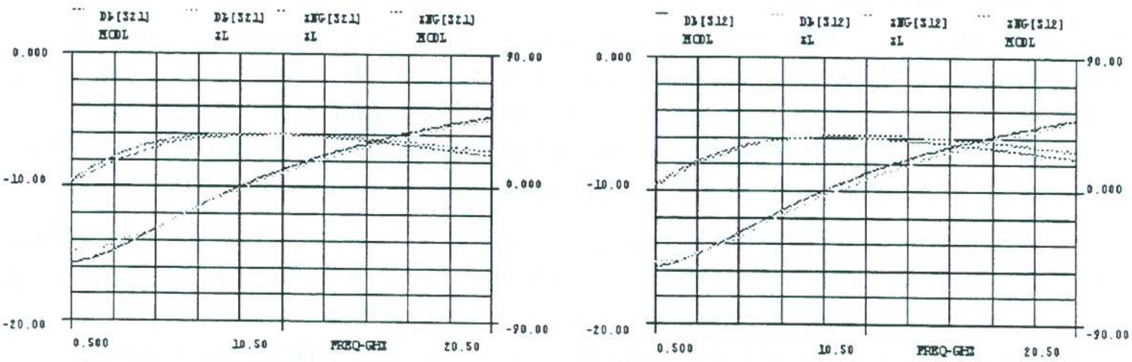

Fig.6b – Measured and modelled S_{21} and S_{12} of the active load at V_{ds} = 0 V