CAD Design of an Active MMIC Circulator at 21-26GHz Frequency Band.

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ABSTRACT.

In this work the design an active MMIC circulator is presented. The foundry process that has been used is the HEMT process of GEC-Marconi Materials H40 (6). The analysis of this circulator is performed using CAD techniques. Specifically the software tool HP-Eesof Series IV (5) is used throughout the design process. Simulation results are presented and a comparison between a typical ferrite circulator and this active design is performed.

Keywords : Active MMIC Circulator, HEMT, H40 process.

INTRODUCTION.

The need for a circulator that can be used in the future wireless handsets which will occupy a very small area and at the same time have almost the same specifications as a typical ferrite one was the motive for the preparation of this work.

MMICs have been widely used not only in the wireless telecommunications domain but anywhere that high frequencies and small area occupation was a vital design aspect. For this specific design the H40 HEMT foundry process of GEC-Marconi (5) has been used. The chip fabrication will be realized through the Eurochip action. The software that has been used is the HP-EEsof Series IV ver. 6.301 (6), and GEC-Marconi has provided all the necessary software libraries in order to design the whole chip concerning the linear and non-linear domain, statistical and yield simulations and finally produce the physical layout to be fabricated.

The circulator's specifications are shown in table.1 where the design effort is given to the upper ISM band with center frequency of 24GHz.

Frequency Range	21-26 GHz
Input Power Gain Compression at 1dB	+3dBm
Noise Figure max	7dB
Return Loss All ports	>13dB
Insertion Gain all ports	2dB+/-1dB
Isolation all Ports (21-26)GHz	>12dB
Isolation all Ports (23-25)GHz	>25dB
Power Dissipation max	0.12Watts
Total Chip Area	4mm^2

Table 1. Specifications of the active MMIC circulator

The design concept of the active MMIC circulator is shown in fig.1.

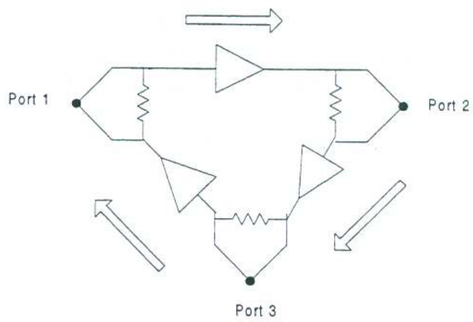

Figure 1. Design Concept of the Active MMIC Circulator

The microwave energy flows clockwise from port 1 to port 3. Inverse flow is prohibited due to the isolation of the amplifiers and mainly due to the isolation of the Wilkinson couplers used. Principal consideration has been given to the design of the Wilkinson dividers/combiners concerning the physical size which is minimized with the use of a semi-lumped technique. Isolation between the input/output ports of the wilkinson combiner/divider is also of great importance since this isolation mainly determines the isolation between the ports of the final design of the active MMIC circulator.

Concerning the amplifier used, a one stage reactive matching amplifier with minimum occupied area possible is designed. The amplifier has a gain of approximately 11dB and it is designed to overcome the losses of the Wilkinson dividers/combiners.

WILKINSON COUPLER DESIGN PROCEDURE.

The Wilkinson divider/combiner approach selected as in Prescott et al (1) is the semi-lumped elements one because compared with the distributed and the full lumped element approach has the following advantages :

- The area occupied is four times less than the distributed one.
- The isolation is in between the specifications of the distributed and the full lumped elements approaches.
- The bandwidth is also in between the specifications of the distributed and the full lumped elements approaches.
- The insertion loss is comparable to the distributed approach.

From the above statements it is obvious why the semi-lumped element approach has been chosen.

The insertion loss and the isolation between the ports 2-3 are shown in fig.2. The return losses are shown in fig.3 and the final optimized layout is shown in fig.4.

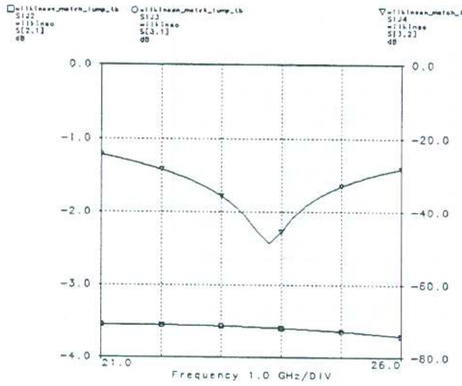

Figure 2. S21, S31 and S32 parameters versus frequency

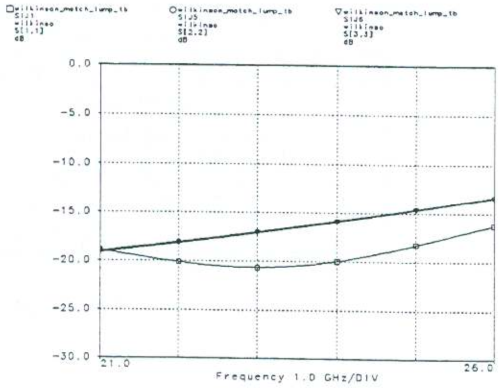

Figure 3. Return losses at all ports

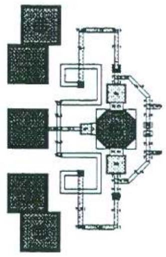

Figure 4. Final layout of the Wilkinson power divider/combiner

From Fig.2 it is shown that the insertion loss of the coupler is approximately 0.5dB which corresponds to a noise figure of 0.5dB also. Compared with the insertion loss of 0.3dB of a distributed design the value of 0.5dB is considered quite good. The isolation curve is centered at 24GHz and the worse value is below -25dB with maximum at 24GHz of -50dB which of course this is expected to be reduced in real on wafer measurements by at least 10dB.
The return losses shown in fig.3 are better than 13dB and the final layout which occupies an area of approximately 0.23mm^2 is shown in fig.4. In this figure the on wafer probe tester tips are shown in a configuration known as GSG (Ground-Signal-Ground) which have a pitch length of 200μm and a pad size of 100x100μm^2.

AMPLIFIER DESIGN PROCEDURE.

The amplifier design is based on a 2x60μm HEMT model with only one source via to ground as in Gasmi (2). The effort was to minimize the amplifier's layout occupied surface because this amplifier stage is copied in three others in order to overcome the inherent losses of the wilkinson dividers/combiners in between all the combinations of the ports 1-2-3.
The total amplifier occupied area is 0.4mm^2 and the gain is approximately 11dB+/-0.4dB. The input and output return losses are better than -10dB in the whole frequency range from 21GHz to 26GHz and the output 1dB power gain compression is +10dBm. The maximum noise figure achieved in the frequency range of interest is 2.7dB and this is considered as a quite good noise figure since no design care is taken into account concerning the noise figure response.
In fig.5 the S-parameters response of the amplifier are shown. In fig.6 the stability factor and the noise figure are shown. From the above mentioned figures it is evident that the amplifier is centered designed at 24GHz as the wilkinson coupler and it is stable in the whole frequency range of interest.

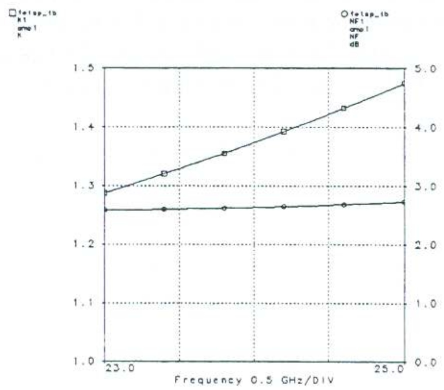

Figure 5. S-parameters response of the amplifier

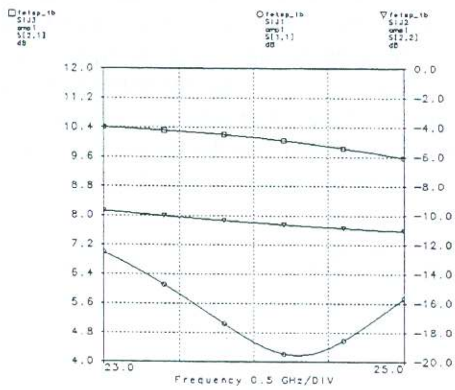

Figure 6. Stability factor and Noise Figure

In fig.7 the output power gain compression at 1dB is presented at the center frequency of 24GHz. From this plot the output gain compression is +10dBm as already stated. The third order intercept point is above +20dBm for a swept range of the input power from -10dBm to +10dBm. The results concerning the IP3 is given in fig.8

Figure 8. P1dB and IP3 of the amplifier stage for input power -10dBm to +10dBm range at 24GHz.

In fig.9 the physical layout of the amplifier is presented. The on wafer probe testing ports are not shown since the active circulator will be tested as an entirety.

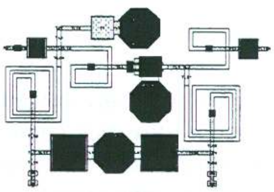

Figure 9. Physical layout of the amplifier

COMPLETE DESIGN OF THE ACTIVE CIRCULATOR

Since the sub-modules of the active circulator as in Berg et al (3) have been examined and tested then the whole design of the active circulator is checked based on the design principle of fig.1. One of the main crucial points is the phasing in between the ports of the circulator. In order to succeed the optimum isolation between the ports the phase difference between two adjacent ports should be ideally equal. The phasing as in Cryan et al (4) is carefully examined through the use of the electromagnetic simulator HP-MOMENTUM which is a module of the HP-EEsof software. The maximum phase imbalance in between any of two ports of the circulator is +/-3 degrees.
The insertion gain between the RF paths and the isolation at any combination of the circulator ports are given in fig.10. The return losses at all ports is given in fig.11.

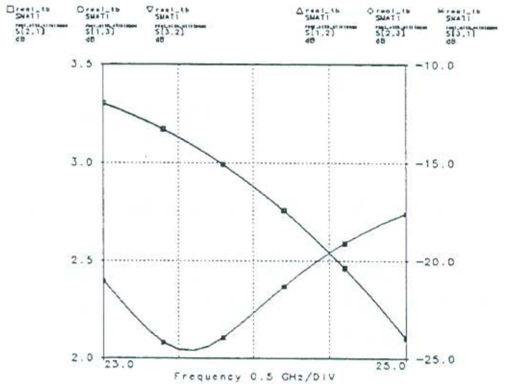

Figure 10. Insertion Gain, Isolation

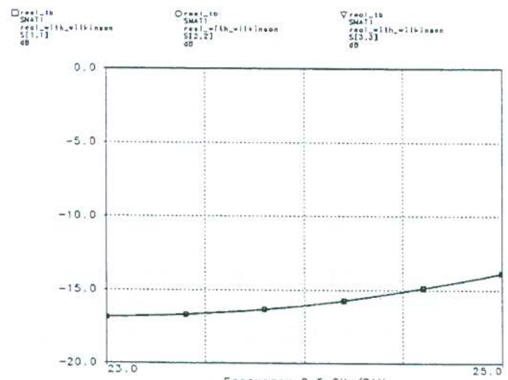

Figure 11.Return Losses at all ports of the active circulator.

The physical layout of the active circulator MMIC is shown in fig.12. The total area occupied is approximately $4mm^2$. The active area of the circulator is approximately $3mm^2$, the rest $1mm^2$ is occupied by the GSG probe tips that should exist on the wafer in order to easily test the MMIC circuit.

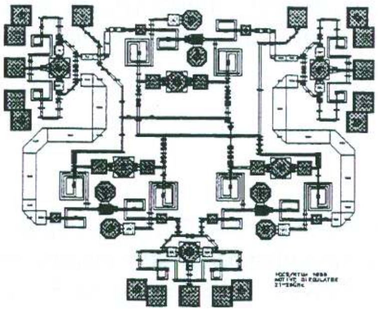

Figure 12. Physical layout of the active circulator MMIC

The bias lines for the gate and the drain ports of the HEMTs are brought all together into a two DC-ports network so that with a dual DC feed through the active circulator can be biased easily. The GSG RF ports are also shown. The chip is expected to be ready by the end of this year (1998) and so full S-parameter measurements will be performed concerning the insertion gain, isolation and return losses. Also non-linear measurements concerning the output power gain compression at 1dB will also be performed. The above mentioned measurements will be done through the use of the Carl Suss on Wafer Probe Tester, the vector Network Analyzer HP-8510C and the Spectrum Analyzer HP-8565E.
In the design of the active circulator it is very important to assure the stability of the whole system. Despite the fact that each amplifier is stable, when they are connected together with the couplers to form the active circulator MMIC it is probable to occur instability for certain conditions as in Berg et al (3). In order to prevent this happens, the isolation parameter of each pair of two adjacent ports should be high enough to have a certain phase and gain margin. Since from the simulation point view only a rough estimation can be done the real experimental results will show us the stability of the MMIC.

COMPARISONS BETWEEN FERRITE AND ACTIVE CIRCULATOR APPROACH

In table 2. a comparison between the ferrite (passive) and the active design approach is done. Depending on the application a choice is performed on the circulator topology to be used.

	Active MMIC approach	**Ferrite (passive) approach**
Surface occupied	$4mm^2$	$100mm^2$
Noise Figure	>5dB	<0.5dB
Output power at 1dB compression	> +10dBm	>+23dBm
Insertion loss/gain	> +3dB	< -0.4 dB
Isolation at all ports	18 dB typical	18 dB typical
Return losses at all ports	15 dB typical	15 dB typical
Bandwidth	Octave to Multi-octave	Octave
Stability	Stable under conditions	Stable due its passive nature

Table 2. Comparisons on the specifications between active and passive circulators.

From table 2. one can choose the circulator topology based on his design project needs. It is evident that the greatest advantage of the active approach over the passive one is its very small size. The rest parameters are under discussion and cannot be considered as advantages or disantvantages of the passive design over the active or vice versa.

CONCLUSIONS.

In this work a novel design for an active MMIC circulator is introduced. Besides some disantvantages like the inherent increased noise figure and the low power gain compression of such a design scheme, the extremely reduced size and the capability of integration of this design in telecommunication integrated circuits make it candidate for miniaturized system designs. Further work includes on wafer measurements of the circuit in order to verify the simulation results and some work on more compact and higher isolation power divider/combiner circuits which will ameliorate the performance of such a circulator.

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