A Fully CAD Consistent Model of MESFETs and HEMTs

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ABSTRACT

An empirical large-signal model of MESFETs and HEMTs has been developed which ensures the full charge conservation, numerical stability and small-signal consistency during computer-aided simulations. For a maximum of accuracy, the charges are directly extracted from the raw gradient experimental data and represented by optimized polynomial functions. The model is valid in reverse operation of the device too. It has been verified for a 0.5 µm gate length, 2 x 50 µm and 4 x 50 µm gate width PHEMTs and implemented into the Hewlett-Packard's MDS software.

INTRODUCTION

The device model must not only represent the device behaviour as accurately as possible, but it must respect the constraints imposed by the circuit simulation. These constraints are more critical than the model accuracy, because their violation may result in catastrophic failure of the simulation. Concerning the HEMTs and the MESFETs, the following conditions must be fulfilled [1], [2], [3]:

1) charges (not voltages) must be chosen as state variables;

2) the functions $Q(V)$ and $I(V)$ must be continuous, and more particularly at $V_d = 0$ when the source and the drain of FETs may change their roles ;

3) the matrix capacitances and conductances of the device must exactly satisfy the path independent integration conditions: $\frac{\partial C_{ij}}{\partial V_k} = \frac{\partial C_{ik}}{\partial V_j}$ and $\frac{\partial g_{ij}}{\partial V_k} = \frac{\partial g_{ik}}{\partial V_j}$;

4) the large-signal model must be consistent with the small-signal model.

Naturally, the model must be simple and easy to extract from data and to insert in the circuit simulator too.

None of existing models meets all the requirements of the circuit simulator enumerated above, which limits the field of their applications. The capacitance models described in [4] to [15] use voltages as state variables. In [4], [5], [6] and [14], only the dependence of the gate-source capacitance C_{gs} on the gate-source voltage V_g is taken in account. In [7], [8], [9], [10], [11], [12] and [15], the drain-source capacitance C_{ds} is assumed to be constant and even equal to zero [9]. These assumptions are good only in the saturated region. In the lookup-table models ([2], [16], [17], [18]), the terminal charges are extracted in a table form by numerical integration of the capacitance data, and then interpolated by spline functions ([2], [16], [17]) or fitted by analytical functions [18]. They are excellent, if the data and the integration are exact. Very often, the capacitance data are "noisy". And there are errors in the quadratures. So, the integration becomes path dependent [16]. The analytical charge models ([19], [20]) use transcendental empirical functions for the charges. The transcendental functions are somewhat simpler to write, but longer to compute than the polynomial ones, and special measures must be taken to avoid divisions by zero or imaginary results when using them [8]. The number of their coefficients is not sufficient to get a good fit to the data. In [20], only the gate charge is modeled, and the drain-source capacitance C_{ds} is assumed to be constant. Both models are not continuous at $V_d = 0$.

In this paper, we develop an empirical large-signal model of HEMTs and MESFETs which ensures the complete charge conservation, convergence and compatibility during the transient and small-signal simulations. The model is simple but rather accurate in all the saturation, linear and inverse device operating regions.

NODAL CHARGES EXTRACTION PROCEDURE

The large signal equivalent circuit of the device (Fig.1) is that used for exemple in [17], [18] and [19]. As analytical expressions for the charges and the capacitances, we suggest polynomial functions of the type $\Sigma a_{ij} V_g^i V_d^j$ ($i = 0, 1, 2, ..., j = 0, 1, 2, ...$), because : they are continued, as well as their derivatives; they can follow more closely the experimental data than transcendental functions, which in addition consume considerable computer time [8]; they can have enough coefficients to ensure a good fit, while respecting the constraints imposed by the simulation.

The danger of the fitting with polynomial functions is that ripples may occur when their order arises. To avoid this, and to meet all the requirements, we use the following procedure to find the optimal charge and capacitance expressions:

1. Choose analytical functions $C_{12}(V_g, V_d)$ and $C_{21}(V_g, V_d)$ which are able to fit closely the experimental data for C_{12} and C_{21}. Keep their coefficients literal (do not calculate their numerical values).

2. Integrate the functions $C_{12}(V_g, V_d)$ and $C_{21}(V_g, V_d)$ to obtain literal expressions for the nodal charges:

$$Q_g = \int C_{12}\, dV_d + a(V_g), \tag{1}$$

$$Q_d = \int C_{21}\, dV_g + b(V_d), \tag{2}$$

where $a(V_g)$ and $b(V_d)$ are the integrating constants.

3. Differentiate Q_g and Q_d to find the literal expressions $C_{11}(V_g, V_d)$ and $C_{22}(V_g, V_d)$. Try to fit the experimental data with them. If the fit is not good, change the functions $a(V_g)$ and $b(V_d)$ appropriately and restart the

procedure from Point 2. If a good fit is not found after many cycles, change suitably the functions $C_{12}(V_g, V_d)$ and $C_{21}(V_g, V_d)$ and restart the procedure from Point 1.

4. Calculate the coefficients of the functions $C_{ij}(V_g, V_d)$ in order to obtain the best fit to all the experimental data. During the optimization, ensure the continuity of the functions $Q_g(V_g, V_d)$ and $Q_d(V_g, V_d)$ at $V_d = 0$ in order to keep the model correct in the case of reverse operation of the transistor. To do this, the charge expressions $Q_{gi}(V_g, V_d)$ and $Q_{di}(V_g, V_d)$ in reverse operation have to be found and to be made equal to $Q_g(V_g, V_d)$ and $Q_d(V_g, V_d)$ respectively at $V_d = 0$. Supposing that the device is symmetric, in reverse operation the gate charge Q_{gi} will be done by the same expression as Q_g, and the drain charge Q_{di}, by the expression of the source charge $Q_s = -Q_g - Q_d$, in which V_g must be substituted by $V_g - V_d$, and V_d by $-V_d$. As a result, k equations $\varphi_k(a_{ij}, b_{ij}) = 0$ which link some coefficients a_{ij} and b_{ij} of the charge expressions will be found.

The error function to minimize is:

$$f = \Sigma(1 - \frac{C_{ij}^{p}}{C_{ij}^{exp}})^2 + \Sigma g_k \varphi_k(a_{ij}, b_{ij}), \tag{3}$$

where C_{ij}^{p} are the literal values of C_{ij} for a set of operating points (V_g, V_d); C_{ij}^{exp} are the experimental (extracted) values of C_{ij} for the same set of operating points (V_g, V_d); a_{ij} and b_{ij} are the polynomial coefficients of Q_g and Q_d respectively ; g_k are Lagrange multipliers ; to ensure the continuity of Q_g and Q_d at $V_d = 0$, the functions $\varphi_k(a_{ij}, b_{ij})$ should cancel at the end of the minimization.

The minimization is realized by solving numerically the system of equations:

$$\frac{\partial f}{\partial a_{ij}} = 0, \quad \frac{\partial f}{\partial b_{ij}} = 0, \quad \frac{\partial f}{\partial g_k} = 0.$$

One or more solutions are possible. The global minimum corresponds to the solution for which f is minimal.

MODEL REALIZATION AND EXPERIMENTAL RESULTS

In order to compare the simulated with the experimental results, the model was completed by the Curtice expression for the drain current [21]. However, the time constant was neglected, because it is implicitly enclosed in the matrix capacitances of our model:

$$I_0 = (a_0 + a_1 V_1 + a_2 V_1^2 + a_3 V_1^3)(1 + aV_d)\tanh(gV_D)$$

$$\text{with } V_1 = V_g\,[1 + b(V_{d0} - V_d)] \text{ and } V_{d0} = 2\text{ V}. \tag{4}$$

A special preliminary procedure was introduced to find the initial values of the coefficients in order to obtain the global optimization. The condition 3) was respected.

The experiments were made with 0.5 μm gate length, 2 x 50 μm gate width pseudomorphic high electron mobility transistors (PHEMTs). The device S-parameters were obtained by small-signal on-wafer measurements with LRM calibration in the frequency range from 0.1 to 40 GHz with a Hewlett-Packard equipment. The values of the extrinsic elements were obtained as in [22], except for C_{pd}, which was separated from C_{ds} as suggested in [23] by extrapolation of the measurements made on transistors with different gate width (2 x 50 μm and 4 x 50 μm). The intrinsic voltages V_g and V_d were calculated for each operating point from the extrinsic ones V_g' and V_d' and the DC current I_D as follows:

$$V_g = V_g' - I_D R_s, \quad V_d = V_d' - I_D(R_s + R_d). \tag{5}$$

All the measurements were made at 101 frequencies for each of the 96 operating points determined by $V_g' = -1, -0.8, -0.6, -0.4, -0.2, 0, 0.2$ and 0.4 V and $V_d' = 0, 0.2, 0.4, 0.6, 0.8, 1, 1.2, 1.6, 2, 3, 4$ and 5 V combinations. The threshold gate-source voltage of the device was found to be equal to - 0.82 V.

Then the incremental capacitances C_{ij} and conductances $g_m = g_{21}$ and $g_d = g_{22}$ were calculated from the intrinsic Y-parameters for each frequency and operating point :

$$C_{ij} = \frac{\mathrm{Im}(Y_{ij})}{\omega}, \quad g_{ij} = \mathrm{Re}(Y_{ij}). \tag{6}$$

In order to minimize the "noise" of the measurements and their frequency dispersion, their average values have been calculated for each operating point in the frequency range from 0.5 to 40 GHz.

Following the procedure described here, the optimal expressions for the charges have been found to be:

$$Q_g = a_{10}V_g + a_{20}V_g^2 + a_{40}V_g^4 + a_{50}V_g^5 + a_{60}V_g^6 + a_{70}V_g^7 + a_{01}V_d + a_{11}V_gV_d + a_{21}V_g^2V_d + a_{41}V_g^4V_d + a_{51}V_g^5V_d + a_{61}V_g^6V_d + a_{71}V_g^7V_d + a_{02}V_d^2 + a_{12}V_gV_d^2 + a_{22}V_g^2V_d^2 + a_{03}V_d^3 + a_{13}V_gV_d^3 + a_{04}V_d^4 + a_{14}V_gV_d^4 + a_{05}V_d^5 + a_{15}V_gV_d^5 + a_{06}V_d^6 \tag{7}$$

$$Q_d = b_{10}V_g + b_{20}V_g^2 + b_{40}V_g^4 + b_{50}V_g^5 + b_{60}V_g^6 + b_{70}V_g^7 + b_{01}V_d + b_{11}V_gV_d + b_{21}V_g^2V_d + b_{31}V_g^3V_d + b_{41}V_g^4V_d + b_{51}V_g^5V_d + b_{61}V_g^6V_d + b_{02}V_d^2 + b_{12}V_gV_d^2 + b_{22}V_g^2V_d^2 + b_{03}V_d^3 + b_{13}V_gV_d^3 + b_{23}V_g^2V_d^3 + b_{04}V_d^4 + b_{14}V_gV_d^4 + b_{24}V_g^2V_d^4 + b_{05}V_d^5 + b_{15}V_gV_d^5 + b_{25}V_g^2V_d^5 + b_{06}V_d^6 + b_{16}V_gV_d^6 + b_{26}V_g^2V_d^6 + b_{36}V_g^3V_d^6 + b_{46}V_g^4V_d^6 + b_{07}V_d^7 + b_{27}V_g^2V_d^7 + b_{37}V_g^3V_d^7 + b_{47}V_g^4V_d^7 \quad (8)$$

Fig. 2 to 5 compare the experimental (extracted) and the computed values of the matrix capacitances C_{ij}.

Fig. 6 and. 7 show the behaviour of Q_g and Q_d around $V_d = 0$. They are continuous and even monotonous functions.

In order to improuve these results even more, a further optimization was made with, as variables, all the coefficients of Q_g , Q_d and I_0 plus the extrinsic parameters of the device. Thus, the difference between the measured and the computed S-parameters was minimized for all operating points. Table 1 gives the values of the model parameters before (which corresponds to the figures 2 to 7) and after this optimization. Fig. 8 compares the measured and the computed scatering parameters for $V_d' = 0$ to 5 V and $V_g' = -1$ to 0.4 V at 20 GHz after the optimization. Fig. 9 shows the measured and the computed scatering parameters for $F = 0.5$ to 40 GHz at $V_d' = 1$ V and $V_g' = -0.2$V.

Similar results have been obtaned for a 4 x 50 μm gate width PHEMT.

The model has been implemented into the Hewlet-Packard's Microwave Design System as a simple two-port device. The same implementation is valid for both forward and reverse operation of the transistor, only the functions $Q_g(V_g, V_d)$, $Q_d(V_g, V_d)$ and $I_0(V_g, V_d)$ have to be switched at $V_d = 0$.

CONCLUSION

The model extraction procedure developed here allows to avoid any problem with charge nonconservation which is crucial for the CAD with MESFETs and HEMTs. The numerical stability during the large-signal simulations is ensured by the choice of polynomial functions for the charges and by their optimization under constraints in order to warrant their continuity even when V_d becomes negative. The applicated optimization method gives all the minima of the error function and makes possible the choice of the solution which corresponds to the global one.

In spite of its simplicity and of the numerous constraints it has to satisfy, our model is rather accurate in all the saturated, linear and inverse transistor operation, because the charge expressions are directly deduced from the raw capacitance (nonintegrated) data.

The same (current generator) equivalent circuit may be used for AC small-signal simulations. This small-signal equivalent circuit does not include any branche capacitance and time constant, and, therefore, has no need of their extraction! So does the large-signal model, which is fully consistant with it.

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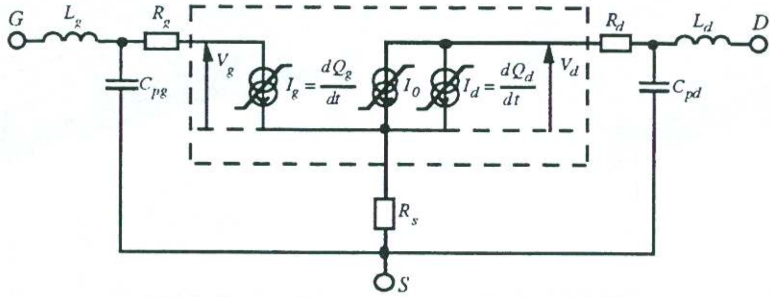
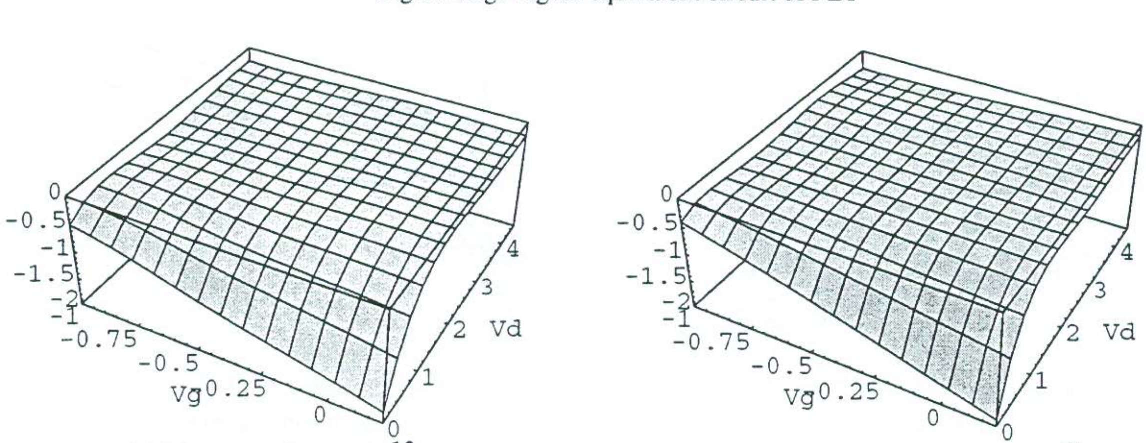
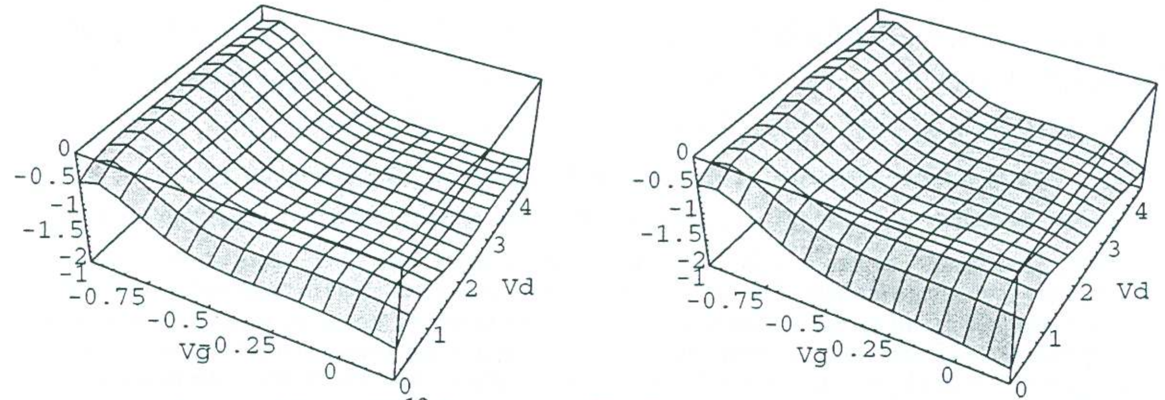


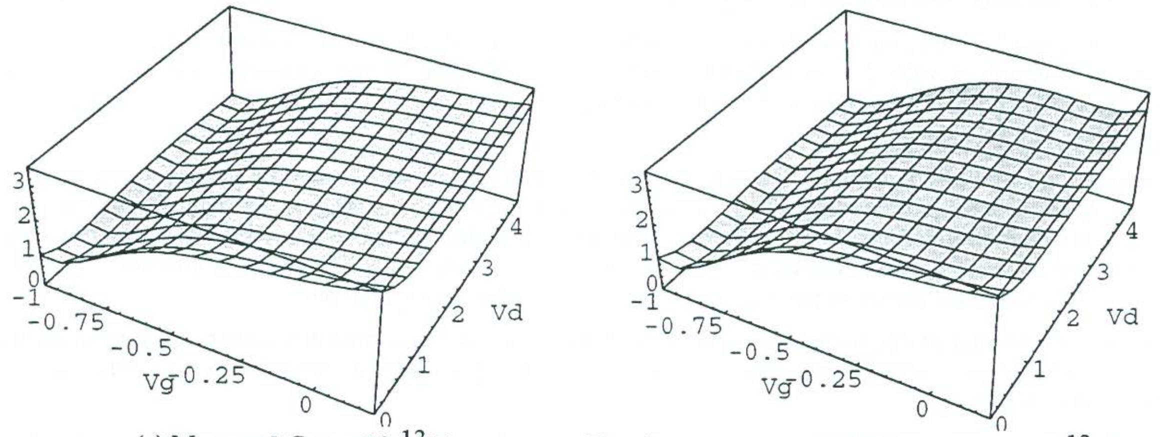
Fig.1. Large-signal equivalent circuit of FET



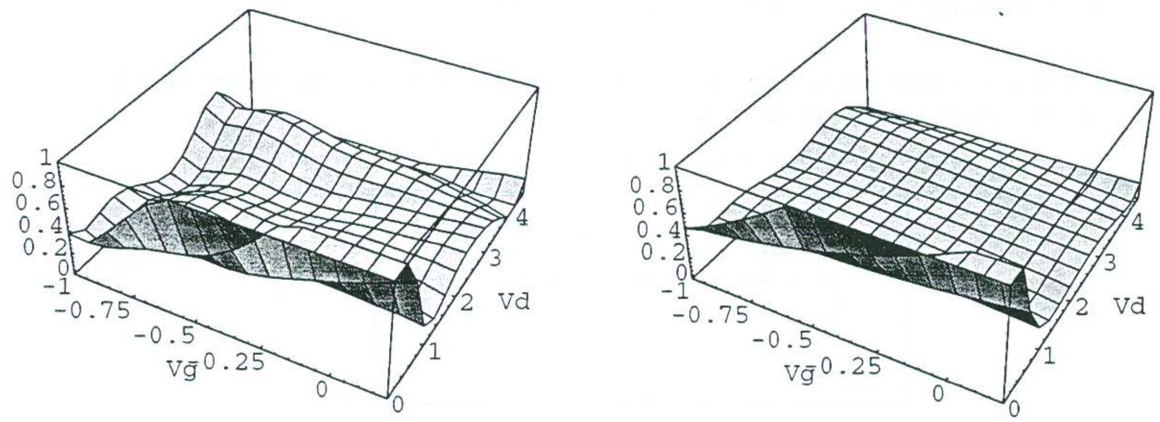
(a) Measured C_{12} x 10^{-13} F   Fig. 2   (b) Modeled C_{12} x 10^{-13} F



(a) Measured C_{21} x 10^{-13} F Fig. 3 (b) Modeled C_{21} x 10^{-13} F



(a) Measured C_{11} x 10^{-13} F Fig. 4 (b) Modeled C_{11} x 10^{-13} F



(a) Measured C_{22} x 10^{-13} F (extended scale) Fig. 5 (b) Modeled C_{22} x 10^{-13} F (extended scale)

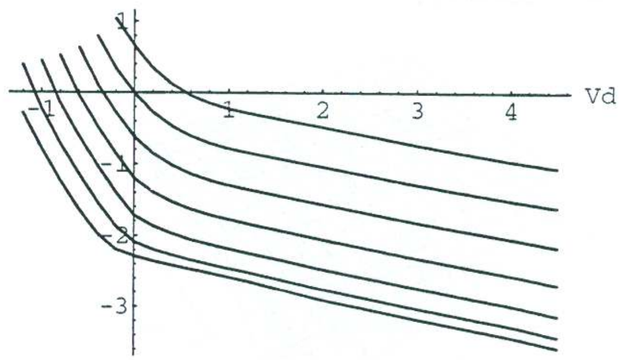


Fig.6. Gate charge Q_g x 10^{-13} C vs V_d with V_g = -1 V (the lower curve) to 0.2 V (the upper curve) by step of 0.2 V as a parameter

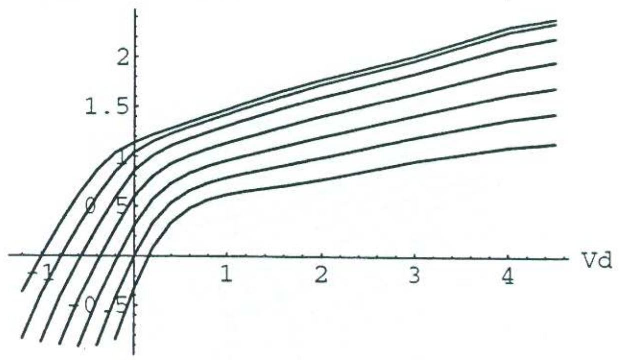


Fig.7. Drain charge Q_d x 10^{-13} C vs V_d with V_g = -1 V (the upper curve) to 0.2 V (the lower curve) by step of 0.2 V as a parameter

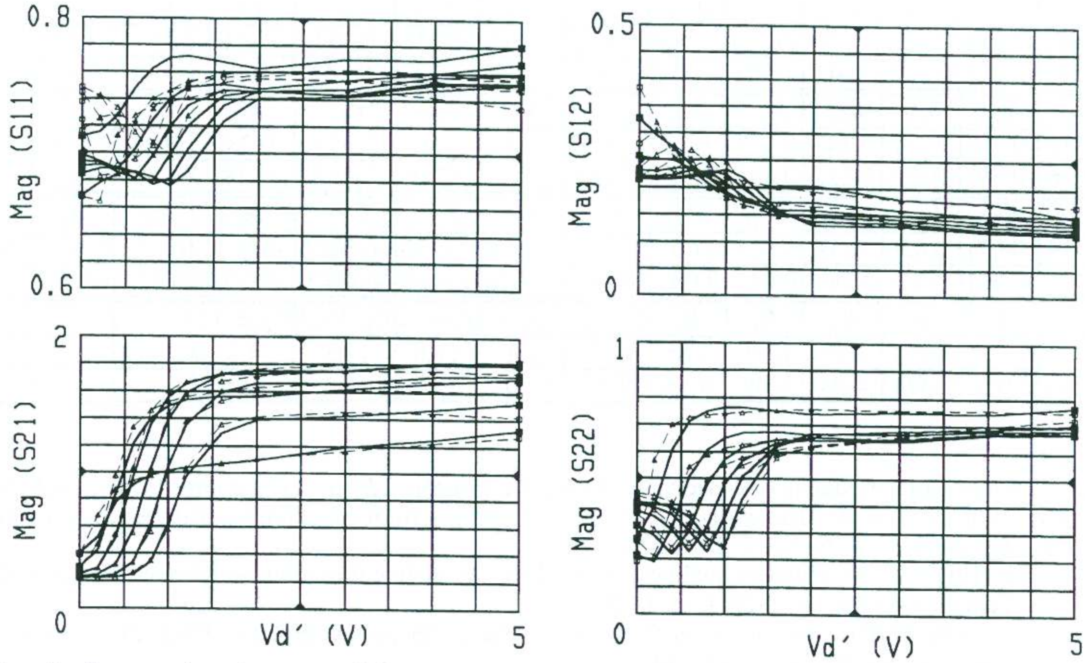


Fig. 8. Measured and computed S-parameters for Vd'=0 to 5 V and Vg'=-1 to 0.4 V at 20 GHz

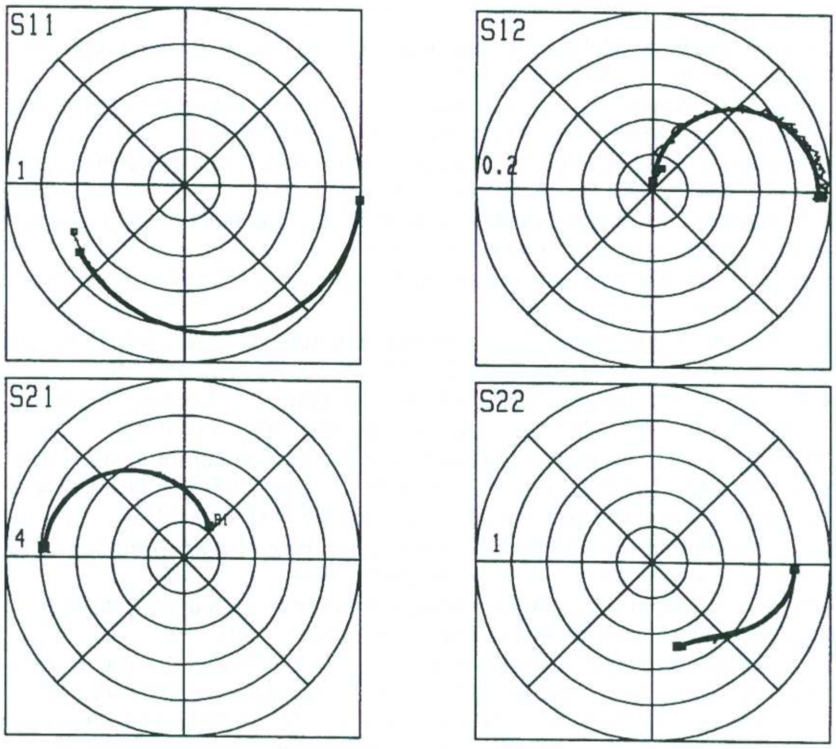


Fig. 9. Measured and computed S-parameters for F=0.5 to 40 GHz at Vd'=1 V and Vg'=-0.2 V

Table 1. The model parameters before (**1**) and after (**2**) the final optimization

	a_{10}	a_{20}	a_{40}	a_{50}	a_{60}	a_{70}	a_{01}	a_{11}	a_{21}	a_{41}	a_{51}	a_{61}	a_{71}	a_{02}	a_{12}
1	3.237	0.496	-0.075	1.081	4.151	2.561	-1.623	-1.352	-0.328	2.275	5.092	4.286	1.282	1.367	1.099
2	3.189	0.477	0.688	1.386	3.766	2.857	-1.321	-0.817	-0.088	2.055	5.098	4.168	0.809	1.097	0.711
	a_{22}	a_{03}	a_{13}	a_{04}	a_{14}	a_{05}	a_{15}	a_{06}	b_{10}	b_{20}	b_{40}	b_{50}	b_{60}	b_{70}	b_{01}
1	0.026	-0.681	-0.408	0.181	0.070	-0.024	-0.004	0.001	-1.618	-0.248	0.037	-0.540	-2.075	-1.281	2.324
2	-0.009	-0.561	-0.253	0.153	0.041	-0.021	-0.002	0.001	-1.594	-0.238	-0.344	-0.693	-1.883	-1.428	3.027
	b_{11}	b_{21}	b_{31}	b_{41}	b_{51}	b_{61}	b_{02}	b_{12}	b_{22}	b_{03}	b_{13}	b_{23}	b_{04}	b_{14}	b_{24}
1	2.878	0.812	-0.368	-0.148	0.248	0.175	-3.022	-3.886	-1.013	2.244	2.376	0.282	-0.931	-0.744	0.093
2	3.874	1.006	-0.507	-0.088	0.222	0.191	-3.722	-5.016	-1.023	2.745	2.997	-0.181	-1.139	-0.930	0.502
	b_{05}	b_{15}	b_{25}	b_{06}	b_{16}	b_{26}	b_{36}	b_{46}	b_{07}	b_{27}	b_{37}	b_{47}	a_0	a_1	a_2
1	0.217	0.115	-0.071	-0.026	-0.007	0.015	0.001	0.0005	0.001	-0.001	-0.0002	-0.0001	0.022	0.039	-0.0038
2	0.267	0.145	-0.221	-0.033	-0.009	0.042	0.002	0.0006	0.0016	-0.003	-0.0005	-0.0002	0.033	0.0523	-0.0285
	a_3	a	b	g	R_g	R_s	R_d	L_gE-12	L_sE-12	L_dE-12	C_{pg}E-15	C_{pd}E-15			
1	-0.023	0.071	0.008	3.484	2.48	6.25	7.85	9.74	0.1	17.8	13.8	7.7			
2	-0.058	0.050	0.022	4.444	4.08	8.49	9.46	9.59	0.091	17.5	13.7	7.76			

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