A New FET Extrinsic Parameter Extraction Method at Pinch-off Bias Utilizing Gate-Width Scaling Property

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ABSTRACT

A new FET extrinsic parameter extraction method is proposed, in which all the extrinsic elements can be determined directly from the S-parameters at pinch-off bias. It utilizes the measurement data of various gate-width FET's and the simple scaling property of each equivalent circuit parameters, eliminating some complex measurement steps such as forward gate bias measurement. Since the gate-width scaling characteristics are taken into account, the proposed method can be utilized for the MMIC design where the optimization of the FET gate-width is important. The proposed method was successfully applied to the modeling of 0.25μm GaAs P-HEMT.

INTRODUCTION

Direct extrinsic parameter extraction methods for GaAs FET's have been developed since late 1980's [1]. In most of these methods, somewhat complex measurements are required; the pad capacitances are extracted from the S-parameters at pinch-off bias, while the parasitic inductances and resistances are estimated from the DC measurement data and the S-parameters at forward gate bias. But the forward bias measurement is not suitable for the short gate-length GaAs FET's because it may lead to the degradation of the Schottky gate characteristics [2]. In addition, few of the previous works have ever dealt with the gate-width scaling characteristics in the modeling procedures, although the optimization of the gate-widths of FET's is often important in the design of MMIC's such as distributed amplifiers.

In this paper, we propose a new extraction method in which all the extrinsic elements can be extracted from the S-parameters at pinch-off bias only. In this method, the pad capacitances are extracted first, and then, with these results, the parasitic inductances and resistances can be extracted from the same measurement data. The problem of the insufficient constraints which often occurrs in the direct extraction method can be eliminated if the gate-width scaling property is utilized. We successfully applied the proposed method to the modeling of S-parameters of 0.25μm GaAs P-HEMT's [3] with 100μm, 250μm, and 300μm gate-width, in the frequency range of 1~ 40GHz.

PARAMETER EXTRACTION PROCEDURE

The applied equivalent circuit of the pinched-off FET is shown in Fig. 1. It is more exact than that applied in the previous work of Dambrine [1] in which they omitted C_{ds} and set $C_{gs}=C_{gd}\equiv C_b$. Although these two assumptions were inevitable for the direct extraction, they yielded inaccurate results. For example, the extracted C_{pg} was much less than C_{pd} [4]. In the previous modeling work utilizing the gate-width scaling [5], it was impossible to directly extract all the extrinsic elements because it used the same equivalent circuit that was proposed by Dambrine [1]. However, it might be possible to extract all the extrinsic elements without the above two assumptions by using the gate-width scaling property for the equivalent circuit elements and the appropriate measurement frequency ranges in the modeling procedures.

In the first pad capacitance extraction step, we can approximate the imaginary part of the Y-parameters of the equivalent circuit as eq. (1) ~ (3) at low frequency region(<5GHz), taking the gate-width scaling into account.

$$Im(Y_{11}) = \omega\,(C_{pg}+C_{gs}+C_{gd}) = \omega\,[\,C_{pg} + W_g \cdot (C_{gso} + C_{gdo})\,] \equiv \omega\, C_{gg} \tag{1}$$

$$Im(Y_{12}) = Im(Y_{21}) = -\omega\, C_{gd} \equiv -\omega\,[\,W_g \cdot C_{gdo}\,] \tag{2}$$

$$Im(Y_{22}) = \omega\,(C_{pd}+C_{gd}+C_{ds}) = \omega\,[\,C_{pd} + W_g \cdot (C_{gdo} + C_{dso})\,] \equiv \omega\, C_{dd}\ , \tag{3}$$

where W_g is gate-width, and C_{gso}, C_{gdo}, and C_{dso} are capacitances per unit gate-width. Thus, C_{gg}, C_{gd}, and C_{dd} can be extracted from the slopes of the Y-parameters of the measured data versus frequency. Fig. 2 shows the extracted C_{gg}, C_{gd}, and C_{dd} for various gate-width FET's. The pad capacitances C_{pg} and C_{pd} can be obtained from the intercept points at the y-axis in C_{gg} and C_{dd} curves [5]. They were extracted to have the almost equal values of 16.5fF and 17.0fF, respectively. Also, the intrinsic capacitances such as C_{gso}, C_{gdo}, and C_{dso} are extracted from the slopes of C_{gg}, C_{dd}, and C_{gd} curves in Fig. 2, and these results are used for the next inductance extraction step.

Then, the parasitic inductances can be extracted using eq. (4) ~ (6).

$$Im(Z_{11,meas}) - Im(Z_{11,mod}) = \omega\,(L_g+L_s) \tag{4}$$

$$Im(Z_{12,meas}) - Im(Z_{12,mod}) = Im(Z_{21,meas}) - Im(Z_{21,mod}) = \omega\, L_s \tag{5}$$

$$Im(Z_{22,meas}) - Im(Z_{22,mod}) = \omega\,(L_d+L_s)\ , \tag{6}$$

where Z_{meas} are the Z-parameters of the measured data after de-embedding the pad capacitances, and Z_{mod} are the Z-parameters of equivalent circuit which consists of the intrinsic capacitances only. Since the difference is more evident at high frequency, we used 20 ~ 40GHz data for this step. Fig. 3 shows the result of these differences for W_g = 250μm device. The three inductances are easily extracted from the slopes of these curves. As shown in Fig. 3, L_s was almost zero for all gate-widths. The extracted L_g and L_d are shown in Fig. 4 for each gate-width. As can be seen in Fig. 4, the parasitic inductances are made of the intrinsic and the extrinsic part, which can be expressed as eq. (7) and (8).

$$L_d = L_{d,ext} + L_{d,int} \cdot W_g \tag{7}$$

$$L_g = L_{g,ext} + L_{d,int} \cdot W_g\ , \tag{8}$$

where $L_{g,ext}$ and $L_{d,ext}$ are the extrinsic inductances which come from the pad and the feed line, while $L_{g,int}$ and $L_{d,int}$ are the scalable intrinsic inductances per unit gate-width.

Finally, in the similar manner, the parasitic resistances can be extracted from the real parts of the Z_{11} and Z_{22} of the measured data [6] using the gate-width scaling property.

$$Re(Z_{11,meas}) = R_g + R_s = W_g \cdot R_{go} + R_{so} / W_g \quad (9)$$

$$Re(Z_{22,meas}) = R_d + R_s = (R_{do} + R_{so}) / W_g \quad , \quad (10)$$

where R_{go}, R_{do}, and R_{so} are resistances per unit gate-width. By multiplying eq. (9) with eq. (10), we obtain eq. (11).

$$Re(Z_{11,meas}) \cdot Re(Z_{22,meas}) = (R_{do} + R_{so}) \cdot (R_{go} + R_{so} / W_g^2) \quad (11)$$

All the parasitic resistances can be extracted from the slope of eq. (10) and the intercept point at y-axis and slope of eq. (11) when eq. (10) and (11) are plotted versus $1/W_g$ and $1/W_g^2$, respectively. Fig. 5 shows the extraction results of the proposed method. The extracted values were R_{go}= 10.8Ω/mm , R_{do}= 0.775Ω · mm , and R_{so}= 0.275Ω · mm.

MODELING RESULTS

Fig. 6 shows the final modeling results at pinch-off bias. The excellent agreement can be seen between the measured and the modeled data for all gate-widths. The extracted extrinsic parameters were listed in table 1. To further validate our method, we applied the extracted extrinsic elements for the small-signal modeling of P-HEMT with W_g=250μm under the normal bias (V_{gs}=-0.5V, V_{ds}=2.0V). After de-embedding the extrinsic parameters, all the intrinsic elements were directly extracted as in the previous works [1][7]. The modeled S-parameters were compared with the measured data in Fig. 7, which also shows quite a good agreement between them with typical rms error of less than 5%. Fig. 8 shows the gate-width dependencies of the extracted intrinsic elements for the normally biased P-HEMT's. All the intrinsic elements were scaled very well with the gate-width at normal bias, just as the gate-width scaling property of the equivalent circuit elements was assumed in the proposed modeling procedures at pinch-off bias

CONCLUSION

In conclusion, we proposed a new FET extrinsic parameter extraction method based on the gate-width scaling property. Since it requires S-parameters at pinch-off bias only, some complex measurement steps can be eliminated including the forward gate bias measurement which often leads to the gate failure. In addition, by considering the gate-width scaling characteristics in the course of the parameter extraction, we can obtain the physically meaningful modeling results for the FET with various gate-widths. The small-signal model parameters of 0.25μm GaAs P-HEMT were successfully extracted with the proposed procedure. The proposed method is also applicable to the other FET's including Si-MOSFET's and InP-HEMT since there is no need for the forward bias measurement.

ACKNOLOGEMENT

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Table 1. Extracted Extrinsic Elements

C_{pg}(fF)	C_{pd}(fF)	R_{so}(Ωmm)	R_{do}(Ωmm)	R_{go}(Ω/mm)
16.5	17.0	0.275	0.775	10.8

L_s(pH)	$L_{g,int}$(pH/μm)	$L_{d,int}$(pH/μm)	$L_{g,ext}$(pH)	$L_{d,ext}$(pH)
0	0.21	0.13	2.9	35.8

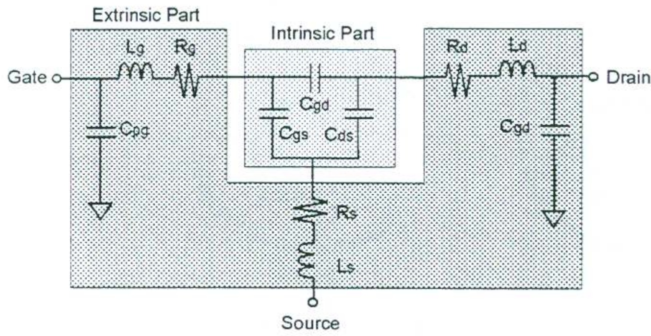


Fig. 1 The equivalent ckt of the pinched-off FET

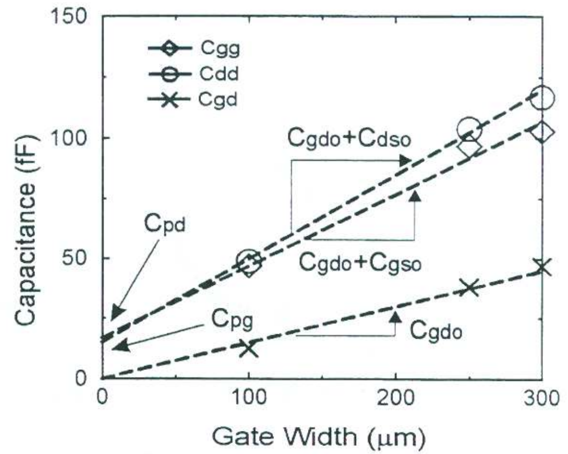


Fig. 2 The extracted C_{gg} and C_{dd} for various gate width

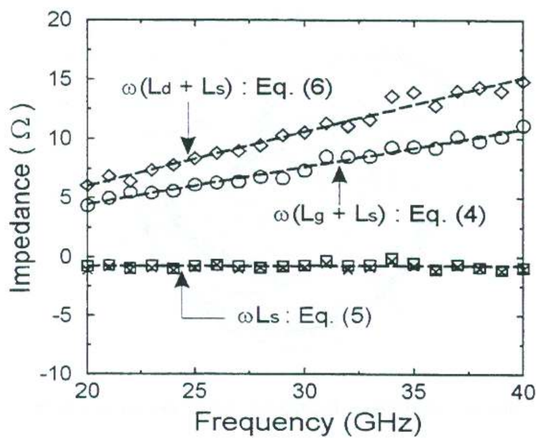


Fig. 3 Parasitic inductance extraction results for W_g=250μm FET.

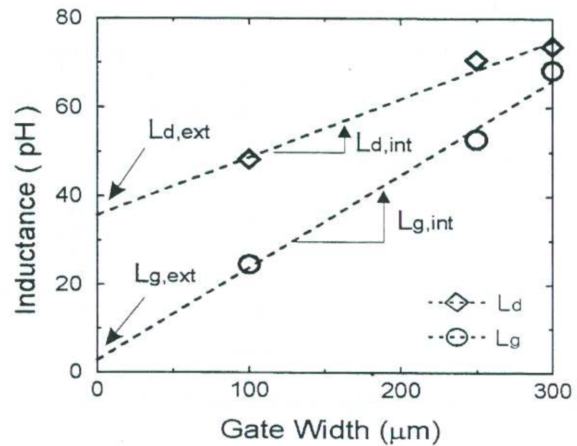
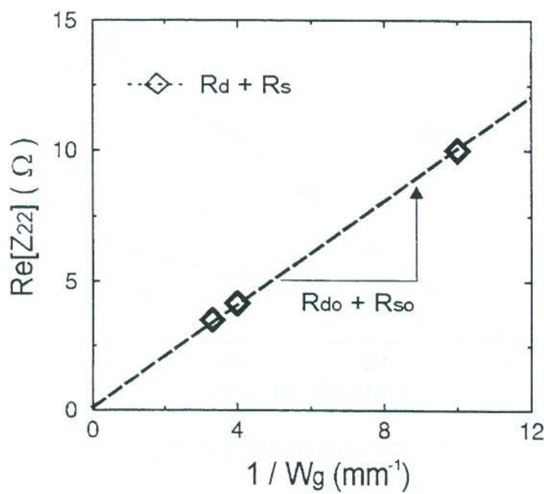
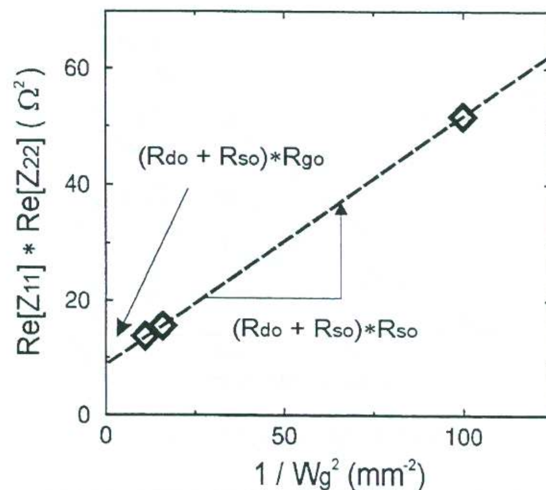


Fig. 4 The extracted L_g & L_d for various gate width

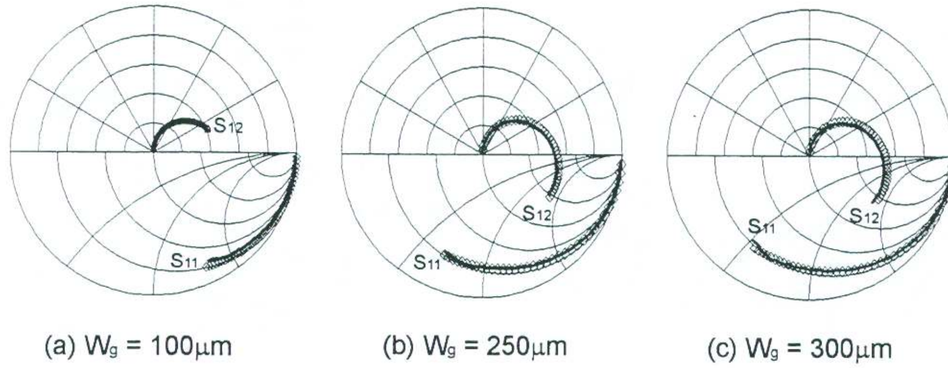


(a) $Re(Z_{22,meas})$ vs. $1/W_g$



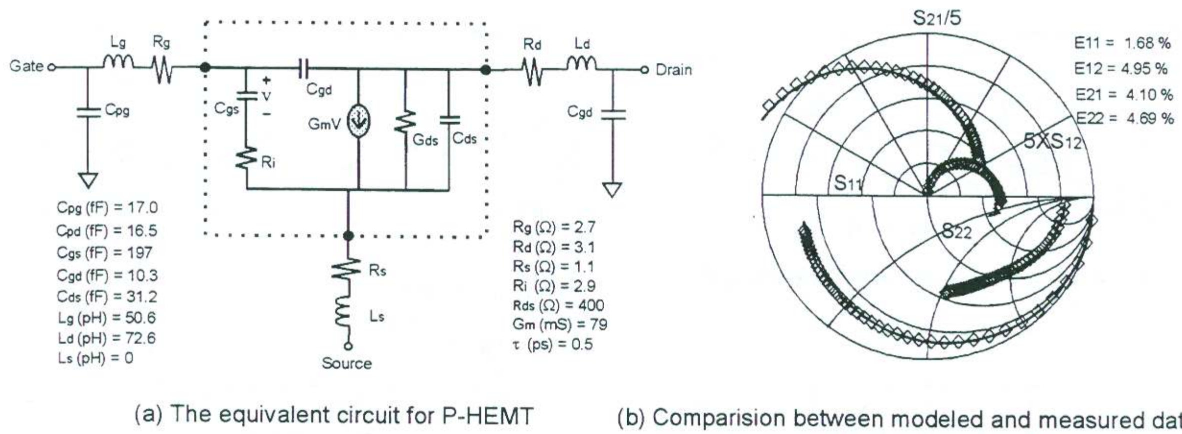
(b) $Re(Z_{11,meas})\ Re(Z_{22,meas})$ vs. $1/W_g^2$

Fig. 5 Parasitic Resistance Extraction



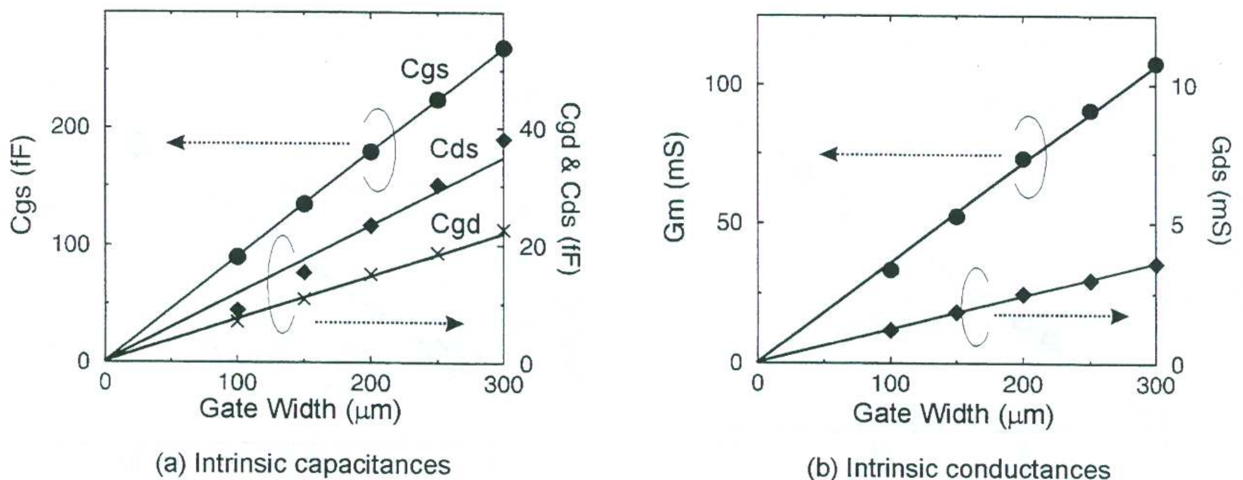
(a) W_g = 100µm (b) W_g = 250µm (c) W_g = 300µm

Fig. 6 The modeling results at pinch-off bias



(a) The equivalent circuit for P-HEMT (b) Comparision between modeled and measured data

Fig. 7 Small-signal modeling results at normal bias (Vgs=-0.5V & Vds=2.0V)



(a) Intrinsic capacitances (b) Intrinsic conductances

Fig. 8 Gate width scaling property of extracted equivalent intrinsic circuit elements at normal bias