A novel thermal resistance extraction technique for temperature-dependent FET modelling

Ingo Schmale and Günter Kompa

University of Kassel, Fachgebiet Hochfrequenztechnik
Wilhelmshöher Allee 73, D-34121 Kassel, Germany, Tel: +49-561-804-6535, Fax: -6529
ingo@hfm.e-technik.uni-kassel.de http://www.uni-kassel.de/fb16/hft/schmale.html

ABSTRACT

This paper proposes a novel technique for extracting FET thermal resistances. The technique is very simple since it requires only data from conventional DC measurements of the gate current, which makes it suitable for widespread application. It is essentially based on the gate-diode's high sensitivity to channel temperature increase engendered by device self-heating. After deriving and explaining the technique's procedural steps, its results for an 0.5µm-gate MESFET are critically discussed.

INTRODUCTION

With solid-state devices reaching permanently towards higher power densities, a precise modelling of the influence of temperature on the semiconductor properties becomes increasingly necessary [1-3]. Large-signal FET models are therefore being developed that take temperature into account as one further state variable besides the drain and gate DC voltages [4-7].

These models relate the dissipated power to some average of the non-uniform channel temperature increase via the layout- and substrate-dependent *effective* thermal resistance. In equivalent-circuit based modelling, it is common to assume a linear relationship between dissipated power and temperature increase. Even though this is not precisely true, it is a viable approximation especially in the saturation region [8].

Besides analytical [3] and optical techniques [1] for determining the value of the thermal resistance, two electrical methods have been proposed. The first, more common of them [3, 9], utilises the gate-forward diode voltage as the temperature sensor in a pulsed-current DC measurement. It can be easily enhanced to determine additionally the thermal time constant. The second method [8] requires less complicated instrumentation, since continuous DC measurements are sufficient. However, it requires an unpractical special test-transistor layout, to observe the gate-resistance change which serves as the temperature sensor.

In this paper, we present a technique that employs the gate diode as the temperature sensor, as in the pulsed electrical measurement method, but which works with simple continuous DC-measurements alone. We therein exploit the non-isothermal *channel* temperature development due to self-heating during DC measurements at constant ambient and chuck temperatures. Since this technique requires only standard measurement instrumentation, and no special test layouts, it is suitable for widespread application.

We exemplify our novel technique for an 0.5µm-gate 4x75µm MESFET (Fig. 1) from the GMMT F20 MMIC technology [10]. While the foundry quotes a power dissipation limit of 1W/mm, no constraints are specified concerning the maximal gate current. From experience, we decided to stay below 60mA/mm in our extensive gate-current investigations.

DC GATE-FORWARD MEASUREMENTS

The precise knowledge of the transistor DC currents at a large number of gate-forward bias points is the prerequisite for this experimental technique. Controlled via a computer, we deploy a semiconductor parameter analyser to sample the gate and drain currents on a tightly-spaced equidistant grid, with V_{GS} up to 0.95V in 0.05V steps, and V_{DS} from 0V to 3V. Ample use is hereby made of the instrument's feature to interrupt the measurement if either of the constraints of maximal power dissipation, or maximal gate or drain current is exceeded.

The measured gate-forward currents are given in Fig. 2 on a natural-logarithmic scale. This is the only suitable representation form, since the exponential nature of the diode yields a ratio of 1:1000 between the smallest and the largest current. Currents corresponding to V_{GS} of 0.7V or less are excluded since they are too noisy.

DE-EMBEDDING TO THE INTRINSIC DIODE REFERENCE PLANE

From Fig. 2, we can distinguish two regions of the transistor operation: While up to a drain-source voltage V_{DS} (extrinsic voltages are indexed by capital letters) of about 1.5V the gate-forward current decreases, it stabilises and slowly increases for higher values of V_{DS}. The first effect is chiefly engendered by the growing voltage drop across the parasitic feed-back resistance R_S' (see Fig. 3), that reduces the *intrinsic* gate-source voltage V_{gs} controlling the gate-source diode D_{gs}. Re-referencing the independent variables to the intrinsic voltage plane is achieved by evaluating:

$$\begin{pmatrix} V_{gs} \\ V_{ds} \end{pmatrix} = \begin{pmatrix} V_{GS} \\ V_{DS} \end{pmatrix} - I_G \begin{pmatrix} R_g + R_S' \\ R_S' \end{pmatrix} - I_D \begin{pmatrix} R_S' \\ R_D + R_S' \end{pmatrix} \tag{1}$$

This formula quantifies how the originally rectangular extrinsic voltage grid (V_{GS}, V_{DS}) is distorted to the intrinsic voltage grid (V_{gs}, V_{ds}) presented in Fig. 4. The transition of the sharp increase of $I_D(V_{DS})$ from the linear region to its nearly constant value of approx. 80mA in the saturation region is clearly reflected in the shape of the $V_{gs}(V_{ds})$-curves in Fig. 4. Since extrinsic and intrinsic gate voltages differ by up to 250mV at high values of V_{DS}, a strong drop of I_G results, when V_{DS} increases to 1.5V. Also, in the ohmic region of the transistor, the two diodes visible in Fig. 3 conduct, making it less suited for the investigation of the single diode's characteristics.

SIMPLISTIC ISOTHERMAL DIODE MODEL

In the saturation region, where V_{ds} is larger than approx. 1V, V_{gs} remains nearly invariant (Fig. 4). Here, only the gate-source diode D_{gs} conducts, controlled alone by the voltage drop V_{gs} across it. On a trial basis, the four measurement samples of each V_{DS}-value are initially fitted to the equation of an ideal diode:

$$I_G = I_{sat}\left(\exp\left(\frac{V_{gs}}{nU_T}\right) - 1\right) \tag{2}$$

with I_{sat} being the reverse saturation current, n the ideality factor, and $U_T = kT_0/q$ the temperature voltage of 26mV corresponding to a chuck temperature of 300K. However, the such fitted variables n and I_{sat} turn out to be functions of V_{DS}, which is due to the increase of I_G in the saturation region (see Fig. 2).

COMPLETE TEMPERATURE-DEPENDENT DIODE MODEL

The I_G current increase in the saturation region occurs with both HEMTs [7] and MESFETs [2], and is due to the rise of the channel temperature T_x in the *static* (as opposed to *pulsed* [11]) DC-measurements, making them effectively non-isothermal. Therefore, the temperature voltage $U_T = kT_x/q$ has to be related to the varying channel temperature T_x (and not the constant chuck temperature T_0). The channel temperature T_x itself is determined as:

$$T_x = T_o + R_{therm} * P_{diss} \tag{3}$$

with P_{diss} being the time-averaged dissipated power in large-signal applications, and R_{therm} the thermal resistance. Fig. 5. illustrates how linearly P_{diss} evolves for the measurement points in the saturation region. R_{therm}, strictly a function of temperature [12], can be introduced as a constant, since the temperature variations are small with respect to their average temperature (in K). The concept of a linear thermal capacitance is neither precisely correct [1], but is of no concern for steady-state high-frequency modelling using harmonic-balance approaches. This is because the effective time constant, quoted to be between 'a few' [11] and 150 µs [3], is several orders of magnitude longer than the RF signal period. This is, however, an upcoming issue when examining pulsed operations in transient analyses.

The full temperature dependence of the current through the rectifying Schottky contact has been derived from semiconductor physics [13, 14] as:

$$I_{diode} = I_{sat}(T_x)\left(\exp(\frac{V_{gs}}{nU_T(T_x)}) - 1\right) \quad \text{with} \quad I_{sat}(T_x) = A^{**}\, S\, T_x^2 \exp(\frac{-\Phi_b}{U_T(T_x)}) \qquad (4, 5)$$

where Φ_b is the Schottky junction barrier height, A^{**} the effective Richardson constant, and S the junction surface. Due to the exponential nature of Eqns. 4 and 5, it is adequate to combine the latter two variables in a new constant C via:

$$\exp(C) \equiv A^{**}\, S \qquad (6)$$

Instead of two as in the isothermal model, four parameters (R_{therm}, C, n, and Φ_b) are now employed to describe the diode current. They are fitted by applying a Simplex-based optimisation algorithm that minimises the least-square distance between the *logarithm* of the modelled and measured currents. Here, points with $V_{DS} < 0.25V$ are excluded, to separate the influence of the second diode D_{gd} (in saturation, D_{gd} is in reverse mode and mainly models the gate-drain breakdown).

In order to improve the modelling accuracy, we find that a better fit is obtained by including the parasitic resistance R_S' as an additional optimisation variable. R_S' then encompasses the known source resistance R_S and one third of the yet unknown channel resistance R_{CH} [2].

RESULTS AND DISCUSSION

The Simplex-based optimisation algorithm converges instantly with the parameters:

Parameter	R_{therm}	C	n	Φ_b	R_S'
Value	133	-15.4	1.51	0.50	3.4
Unit	K/W	$\ln(A/K^2)$	-	V	Ω

Tab. 1: Diode modelling parameters obtained by Simplex-search optimisation algorithm

The thermal resistance R_{therm} of 133 K/W leads to a maximal channel heating of 40 K, which is a typical value for such low power transistors [5]. From Eqn. 6, with C optimised and the junction surface S given by the geometry as 300µm*0.5µm, the effective Richardson constant can be determined to be $A^{**} = 0.14A/(cm^2K^2)$. However, S is overestimated this way, since current crowding towards the source-sided gate edge occurs. This leads to a corresponding slight underestimation of A^{**}. The effective Richardson constant is known to vary significantly from its theoretical value of $4.4A/(cm^2K^2)$ for GaAs due to charge generation and surface imperfections in the junction [14]. While A^{**} is well in the range typical for MESFETs, the ideality factor n = 1.51 is somewhat larger. Values reported for n are around 1.25 for MESFETs, and 1.65 for HEMTs [2]. The barrier height Φ_b of 0.5V is very consistent with results from an activation analysis carried out for a shallow-implant MESFET reported there, that also features an elevated value of n. That MESFET has the same gate dimensions as the one examined here, which permits to directly compare them, as n and Φ_b are also functions of the gate geometry [2].

The value of R_S' is slightly larger than the source resistance R_S extracted from 'cold' S-parameter measurements at $V_{DS} = 0V$ [10]. Under the assumption of bias independence of both R_S and the channel resistance R_{CH} in the examined bias range, a value of $R_{CH} = 4.2\Omega$ can be specified. By including R_{CH} (via R_S') into the optimisation, initial uncertainties about it, which are one reason for *pulsed* electrical DC measurements [1], can be solved.

As all the physical parameters describing the diode are well plausible, the quantitative correctness also of R_{therm} can be expected. Yet, the residual error after optimisation is relatively flat, giving rise to a possible uncertainty of R_{therm} of around ±20%. This is small compared to the general R_{therm} determination problems inherent in all experimental electrical techniques, as outlined in [9].

LARGE-SIGNAL EXPERIMENTAL VERIFICATION

Fig. 6 shows the dynamic input current vs. input voltage trajectory, as sampled with our waveform measurement system [15] at a fundamental frequency of 1 GHz. When the diode conduction sets on, the input voltage is clipped, which is well reproduced by the large-signal simulations. The observed agreement between large-signal measurements at different fundamental frequencies and input powers supports the validity of our modelling approach.

CONCLUSION

We have proposed a novel technique to determine R_{therm} which only requires conventional DC measurement equipment. Through an optimisation, five parameters have been fitted to model the gate-forward currents, one of which is R_{therm} that includes the influence of self-heating engendered by high drain currents. While these first results are very consistent with published data, comparative determinations with conventional experimental techniques should provide supplementary experimental evidence to further validate our novel technique.

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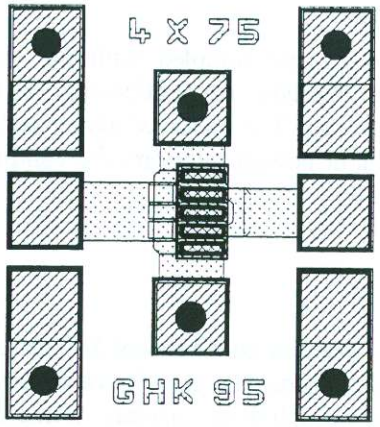

Fig. 1: Layout of the 4x75µm 0.5µm-gate GaAs MESFET considered in this paper. Chip size is approx. 0.3x0.3 mm^2. Measurements were performed on wafer.

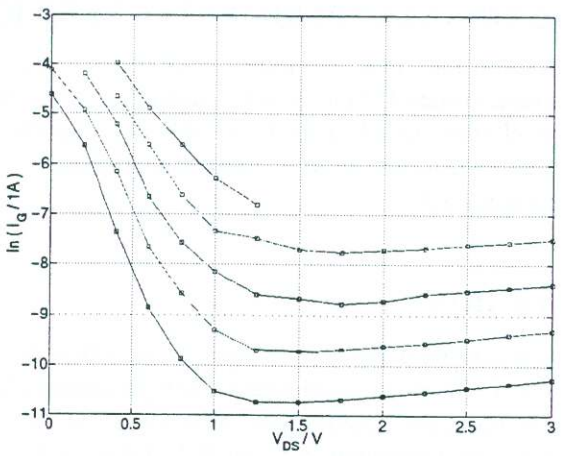

Fig. 2: Logarithmic representation of the measured gate-forward current as a function of V_{DS} with V_{GS} from 0.75 V to 0.95 V (step 0.05V).

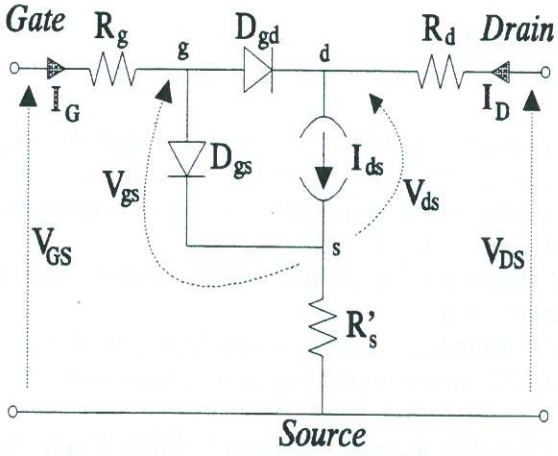

Fig. 3: Utilised equivalent DC circuit of a FET, showing the resistive parasitics and the intrinsic device. In saturation, only D_{gs} conducts. $R_S' = R_S + 1/3\ R_{CH}$

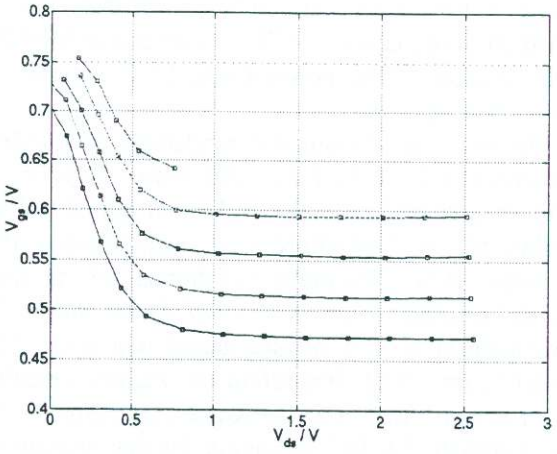

Fig. 4: Intrinsic voltages V_{gs} and V_{ds} of the measured points, as calculated in the voltage plane re-referencing (Eqn. 1). The corresponding extrinsic voltages are on a rectangular grid.

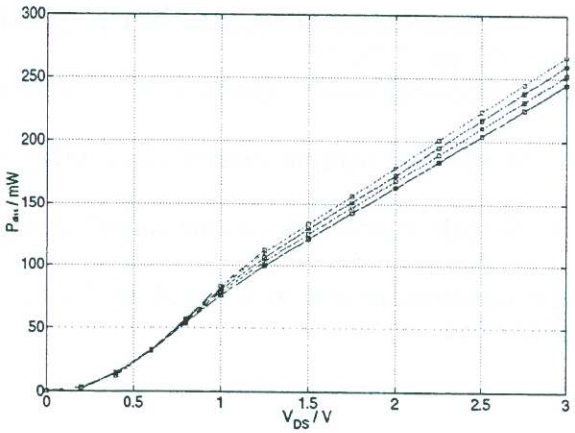

Fig. 5: Dissipated power corresponding to the measured bias points. For $V_{DS} > 1.5$V, the increase is very linear with V_{DS} due to I_{ds} being saturated at ≈ 80mA.

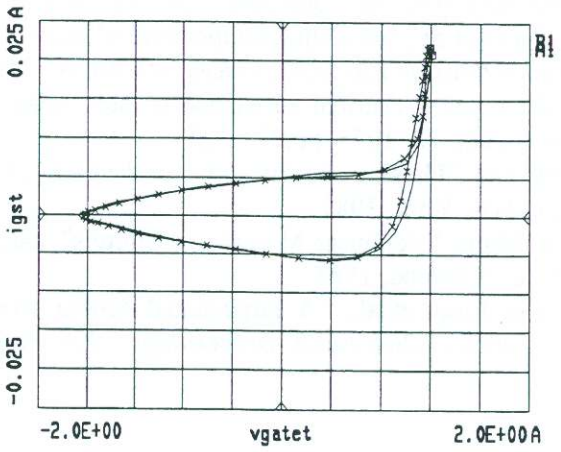

Fig. 6: Input trajectory at f_0 = 1 GHz, V_{GS} = 0 V, V_{DS} = 4 V, P_{in} = 10 dBm. Crosses: waveform measurements Lines: large-signal HB simulations