

A 23 GHz BASEBAND HBT DISTRIBUTED AMPLIFIER FOR OPTICAL COMMUNICATION SYSTEMS

A. Iqbal and I. Z. Darwazeh

Department of Electrical Engineering and Electronics, UMIST
P. O. Box 88, Manchester, M60 1QD, U. K.
Tel: +44 (0)161-200-4747
Fax: +44 (0)161-200-4770
E-mail: iqbala@fs4.ee.umist.ac.uk
darwazeh@umist.ac.uk

ABSTRACT

This paper reports on a practical HBT distributed amplifier MMIC suitable for optical receiver applications. The circuit topology is based upon application of a novel technique which allows baseband operation in conjunction with dc bias stabilisation and does not consume a large amount of chip area. $2 \times 2 \mu\text{m}^2$ single emitter finger InGaP/GaAs HBTs with $f_T = 60 \text{ GHz}$ and $\beta_{dc} \approx 100$ have been employed. Simulation results show a bandwidth extending from near-dc to 23 GHz and an S_{21} gain of $11 \pm 1 \text{ dB}$ at midband. The amplifier has a transimpedance gain of $45 \pm 1 \text{ dB}\Omega$ and a group delay variation of $\pm 30 \text{ ps}$ across the passband. Eye diagram simulations indicate its potential for handling data rates of up to 30 Gbit/s when employed as an optical receiver preamplifier.

INTRODUCTION

High bit rate optical communication systems require wideband optical receiver preamplifiers. For intersymbol interference free operation the upper cut-off frequency of the preamplifier must be greater than 0.7 times the bit rate of the non-return-to-zero (NRZ) digital signal [1]. In addition, the amplifier's gain must extend to sufficiently low frequencies, typically less than 100 kHz [2] so that long bit streams can be processed without introducing bit pattern induced errors. The required lower cut-off frequency is determined by the system standard used. For example, with the Synchronous Digital Hierarchy standard the lowest bit stream frequency is 8 kHz, although in practice a lower frequency limit of 30 kHz is sufficient for most applications [1].

The wide bandwidth of distributed amplifiers (DAs) renders them particularly suitable for use in high bit rate optical communication systems. MESFET and HEMT based DAs have been widely demonstrated [2-4], but the use of HBTs in DAs is a relatively new approach [5-7]. HBTs are expected to offer linearity, $1/f$ noise and power handling advantages over their MESFET/HEMT based counterparts, in addition to requiring less stringent lithographic requirements [8].

HBT BASED DISTRIBUTED AMPLIFIERS

To a large extent, the gain-bandwidth product of a distributed amplifier is determined by that of its constituent gain cells, which usually take the form of common-emitter HBTs (or common-source MESFETs/HEMTs) or cascode stages. In practice, a biasing arrangement must be implemented which does not compromise the gain-bandwidth product and dc bias stability of the amplifier. Due to the inherent current-controlled nature of HBTs, dc bias stabilisation with respect to ambient temperature variations poses a greater problem for HBT amplifiers than it does for those based on MESFETs/HEMTs. Various active biasing techniques exist for providing bias stabilisation, but incorporating them into a distributed amplifier circuit structure can be problematic and may result in compromises in performance. A simple method of providing a reasonable degree of stability of HBT collector current in the presence of moderate temperature changes is to employ an emitter resistor, R_e as shown in Fig. 1. The voltage, V_{emit} at the emitter terminal helps to minimise the effects of temperature induced changes in the base-emitter voltage of the transistor and thereby, helps to stabilise the collector current. In order to minimise gain reduction at low frequencies due to ac negative feedback, it is necessary to bypass R_e with a large emitter decoupling capacitor, C_e . In practice, the MMIC chip area available is limited, which restricts the value of C_e to several tens of pF. This limitation results in insufficient bypassing of the emitter resistor at low frequencies causing gain reduction and thereby, increases the lower 3 dB cut-off frequency. In effect, there is a trade-off between having dc bias stability and sufficient gain at low frequencies. The majority of the HBT based DAs reported in the open literature have been designed without bias stabilisation emitter resistors [5, 6]. As a consequence, the performance of such amplifiers is prone to noticeable change in the presence of ambient temperature variations. Suzuki *et al.* [7] have reported a HBT distributed amplifier employing emitter resistors for the specific purpose of reducing output signal distortion.

In a previous paper [9] we introduced the basics of a new technique for achieving simultaneous baseband operation and dc bias stabilisation of HBT based distributed amplifiers with respect to moderate ambient temperature variations. This technique does not employ large emitter decoupling capacitors and therefore results in a saving of chip area. Here, we present details of the application of this technique to produce a practical HBT distributed amplifier with the potential for use as a receiver in high bit rate optical communication systems. A similar technique has also been applied to high speed HBT based buffers and is reported in [10].

DESIGN TECHNIQUE FUNDAMENTALS

In Fig. 2(a) Z_{emit} is the impedance seen looking into the emitter terminal of a common-collector HBT. Fig. 2(b) shows the simplified hybrid- π equivalent model of such a HBT circuit from which Z_{emit} can be obtained as follows [9]:

$$Z_{emit} = r_e + \frac{(r_{bi} + r_{bx}) + (r_{\pi} \parallel c_{\pi}) + (R_1 \parallel R_2 \parallel C_B)}{\beta_{ac} + 1} \quad (1)$$

where \parallel signifies a parallel combination of impedances and the ac current gain, β_{ac} is given by

$$\beta_{ac} = \frac{g_m r_{\pi}}{1 + j\omega r_{\pi} c_{\pi}} \quad (2)$$

Z_{emit} can be expressed as a complex impedance with frequency dependent resistive and reactive components, $R(\omega)$ and $X(\omega)$, respectively, *i.e.*

$$Z_{emit} = R(\omega) + jX(\omega) \quad (3)$$

Fig. 3 shows the resistive and reactive components of Z_{emit} when a HBT with $f_T \approx 60$ GHz is employed in the common-collector circuit of Fig. 2(a), where for clarity, extension of the two curves to dc has been omitted. It can be seen that Z_{emit} remains dominantly resistive up to $\approx f_T$ of the transistor. Moreover, $R(\omega)$ assumes a low value of several tens of Ohms up to frequencies approaching f_T . It is these resistive properties of Z_{emit} that form the basis of the new technique.

Fig. 4 shows a common-emitter HBT amplifier in which the emitter resistor is actively bypassed by a common-collector HBT (Fig. 2(a)) in contrast to passive bypassing as shown in Fig. 1. Both transistors in Fig. 4 are identical in all respects. For comparison purposes the value of the emitter resistor, R_e is halved in the actively bypassed amplifier so as to keep its emitter voltage equal to V_{emit} . The overall circuit structure shown in Fig. 4 resembles that of a differential amplifier, but its operation differs in a fundamental way in that the common-collector HBT is utilised purely as an impedance. By considering Z_{emit} it can be seen that the common-collector HBT behaves like a low value resistor in parallel with R_e . Consequently, the effective resistance present at the emitter terminal of the common-emitter HBT is reduced, even at low frequencies, thereby allowing gain to be extended into the baseband region. In addition, bias stability with respect to temperature variations is not compromised because the dc emitter voltage, V_{emit} can be maintained. Moreover, the common-collector HBT consumes considerably less chip area than an emitter decoupling capacitor. Fig. 5 contrasts the simulated gain of the actively and passively bypassed amplifiers depicted in Fig. 4 and Fig. 1, respectively, where gain extension to dc has not been shown for clarity. The amplifier with active bypassing has an essentially flat 4 dB gain from near-dc to approximately 20 GHz and an upper 3 dB cut-off frequency of 73 GHz. The lower and upper 3 dB cut-off frequencies of the amplifier utilising passive bypassing are close to 0.5 GHz and 62 GHz, respectively. Its midband gain approaches 10 dB due to the low impedance of C_e in this operating region, but at low frequencies it deteriorates considerably to -11 dB. The gain flatness and extension of gain down to dc in the active bypassing case is achieved at the expense of gain itself. This occurs because Z_{emit} remains resistive, effectively at all frequencies within the passband and thereby lowers the overall gain of the amplifier.

Earlier work [9] has shown that in order for the active bypassing technique to be effective, the common-collector HBT must possess low values of r_{bi} , r_{bx} , r_{π} , r_e and c_{π} so as to minimise the resistive component of Z_{emit} . It can be seen from equation (1) that with the exception of r_e , all of the other terms of Z_{emit} are divided by β_{ac} which aids reduction of $R(\omega)$. Therefore, high values of β_{ac} and f_T are necessary to ensure that impedance scaling via β_{ac} occurs over a sufficiently wide bandwidth. The overall effectiveness of the active bypassing technique depends to a certain extent on the actual common-emitter HBT amplifier which possesses the emitter resistor requiring bypassing. This occurs because the ac feedback fraction arising from the coupled emitter terminal depends on both the characteristics of the common-emitter HBT, as well as on the effective impedance present at its emitter terminal.

Although the circuit shown in Fig. 4 can be used to demonstrate the technique of active bypassing by means of simulations, its biasing arrangement renders it unsuitable for use as a practical amplifier. This is because the circuit is

sensitive to power supply variations which can produce differences in the base-emitter voltages of the HBTs causing one of the HBTs to either cut-off or saturate. Appropriate modifications have been made to the biasing arrangement when the active bypassing technique is employed in the distributed amplifier design and are discussed in the following section. When applied to a practical amplifier, the active bypassing method has several disadvantages in that the common-collector HBTs introduce extra noise and also cause an increase in power consumption. Furthermore, the presence of these HBTs necessitates an additional power supply.

HBT BASED DA CIRCUIT STRUCTURE AND LAYOUT

Fig. 6(a) shows the overall circuit structure of the HBT based distributed amplifier where the number of sections was chosen to be four in order to maximise its gain-bandwidth product. The input and output artificial transmission lines (ATLs) are constructed in a microstrip environment and are both terminated by 50Ω loads, R_b and R_c , respectively. A 10Ω resistor, R_o is used to flatten gain response peaks that arise from the presence of a bondwire in the V_{cc2} supply rail. The nine grounded capacitors in the circuit help to decouple the V_{cc2} and V_{ee} supply rails. Fig. 6(b) shows the schematic of each cascode gain cell. The cascode cell formed by transistors Q_1 and Q_2 is used to increase the upper cut-off frequency of the amplifier. Q_2 is biased by the potential divider formed by resistors R_{fb} and R_{cb} , where C_{cb} serves as an ac bypass capacitor for the latter. R_{fb} provides ac negative feedback in order to maintain unconditional stability of the cascode cell. However, in doing so it also causes a reduction in the bandwidth of the DA. The design value of R_{fb} was selected so as to ensure unconditional stability of the cascode cell whilst minimising the loss of bandwidth. Bias stabilisation with respect to ambient temperature variations of the common-emitter HBT, Q_1 is achieved through the use of R_e , across which exists a potential difference of approximately 2 V. Following the discussion of active bypassing in the previous section the common-collector transistor, Q_3 is used to provide bypassing of R_e at signal frequencies. R_e also serves to stabilise Q_3 at dc. The dc base voltages of Q_1 and Q_3 are both close to zero volts because the high β_{dc} values ensure minimal base currents. A bypassed resistor, R_{cc} is necessary to equate the near-zero dc base voltage of Q_3 to that of Q_1 . Consequently, the $R_1 || R_2 || C_B$ term in equation (1) must be replaced by $R_{cc} || C_{cc}$. The base-emitter voltages of Q_1 and Q_3 are established through R_e using a single negative power supply, V_{ee} . This biasing arrangement ensures that the base-emitter voltages of Q_1 and Q_3 always remain equal and that any power supply variations are reflected equally in the collector currents of both transistors, thereby avoiding cut-off or saturation of either HBT. It also has the added advantage of providing good grounding of the input line idle port termination, R_b . The capacitor, C_{de} is necessary to provide decoupling of the collector of Q_3 .

The distributed amplifier employs $2 \times 2 \mu\text{m}^2$ single emitter finger InGaP/GaAs HBTs with $f_T = 60 \text{ GHz}$ and $\beta_{dc} \approx 100$. The nominal operating point of each HBT was chosen to be $I_c = 1.5 \text{ mA}$ and $V_{ce} = 2.5 \text{ V}$ in order to maximise current gain. HBTs with larger areas were constructed by connecting several $2 \times 2 \mu\text{m}^2$ HBTs in parallel. Q_1 and Q_2 are both composed of two HBTs in parallel as this was found to offer a good compromise between the gain and input capacitance of the cascode cell which directly affects the upper cut-off frequency of the input ATL. A parallel combination of four HBTs has been chosen for Q_3 in order to decrease the resistive element of the impedance ($Z_{emitter}$) seen looking into its emitter terminal.

Fig. 7 shows the layout of the HBT based DA implemented in MMIC form. Four identical actively bypassed cascode cells are present in the centre of the pad frame, each containing eight HBTs. The layout topology of the cascode cell is based upon a compromise involving minimising both the chip area consumed and the interconnect inductance between components, as well as reducing electromagnetic coupling. Since each cell requires four grounding points, adjacent cells share substrate vias in order to minimise consumption of chip area. The positions and orientations of the HBTs of the cascode cell and those of the active bypassing circuit were chosen to eliminate bends in the interconnect metal which may affect amplifier performance due to electrical line length shortening effects. At high frequencies the non-ideal characteristics of the thin film feedback resistor, R_{fb} cause its resistance to decrease, thereby resulting in a reduction in bandwidth. It was found that keeping the dimensions of R_{fb} to a minimum helped to maintain its nominal resistance value at high frequencies. The common-base HBT biasing resistor, R_{cb} has no function at ac and was therefore meandered to save space. The dimensions of R_{cb} were kept large so that its dc resistance value decreased at high frequencies, thereby aiding grounding of the base of the common-base HBT.

Meandered input and output microstrip transmission lines can be seen at the lower and upper halves of the layout, respectively. Their lengths were optimised for maximum gain-bandwidth product. Curved bends with large radii of curvature have been utilised to minimise line shortening effects and the separation between adjacent bends has been kept large in order to reduce electromagnetic coupling. The input line is terminated by the grounded 50Ω resistor, R_b present in the lower right quadrant of the chip and carries a current of $124 \mu\text{A}$. At dc the output line carries a total current of 16 mA and is terminated by the 50Ω resistor, R_c . It also functions as the positive V_{cc1} power supply rail. Simulations showed that good grounding of R_c could be implemented externally through the V_{cc1} power supply, but a large decoupling capacitor was included nevertheless if the need arises to ground R_c internally. The positive V_{cc2} supply rail runs along the upper half of the layout and carries a dc current of 24 mA , whilst the negative V_{ee} rail runs along the lower half and carries approximately 36 mA . Both supply rails were kept wide in order to reduce their inductances and

are decoupled via the nine grounded capacitors. The common-collector HBTs help to further decouple the V_{cc} rail. Input and output port probe pads are present at the bottom and top of the layout, respectively and are constructed by connecting substrate vias to the appropriate pads on the chip frame. Passive and active test structures separate from the amplifier have been placed at the upper and lower edges of the MMIC, respectively. The chip measures $2.5 \times 2.5 \text{ mm}^2$ and is expected to dissipate 220 mW of power. Off-chip ac coupling capacitors are required for correct operation of the distributed amplifier because sufficiently large metal-insulator-metal capacitors cannot be integrated on-chip.

SIMULATION RESULTS

Simulations of the HBT based distributed amplifier were carried out using full MMIC element models, with 0.2 nH bondwires also included. Fig. 8(a) shows that the lower 3 dB cut-off frequency of the amplifier is approximately 80 kHz. Extension of midband gain to dc is limited only by the size of the off-chip ac coupling capacitors which in this case was taken to be a practical value of 30 nF. Fig. 8(b) shows S-parameter simulation results from 1 GHz to 30 GHz. S_{21} is 11 ± 1 dB over the passband and the upper 3 dB cut-off frequency of the amplifier is 23 GHz. S_{11} and S_{22} are both less than -5 dB across the entire passband. The gain-bandwidth product of the amplifier was found to be limited by three main factors related to circuit topology and elements other than the HBTs and bondwires. Midband gain was deteriorated by the active bypassing circuit through the mechanism outlined in a preceding section. Bandwidth was reduced as a result of the resistor R_b decreasing in value at high frequencies, thereby causing excess negative feedback within the cascode cell. The increase in inductance and to a lesser extent, in resistance of the input and output microstrip transmission lines at high frequencies resulted in the characteristic impedance of the artificial lines deviating significantly from 50Ω . This caused a loss of gain-bandwidth product through reflections from the port terminations and can be seen in Fig. 8(b) as an increase in S_{11} and S_{22} at high frequencies.

The ratio of gain-bandwidth product (GBP) to that of active device f_T is a figure of merit that indicates the effectiveness of a circuit structure in exploiting the high performance characteristics of the HBTs. For the design under consideration $\text{GBP} = 81.6 \text{ GHz}$, $f_T = 60 \text{ GHz}$, making $\text{GBP}/f_T = 1.36$. As a simple comparison, a current high performance HBT distributed amplifier reported by Kobayashi *et al.* [6] employing InP based HBTs with $f_T \approx 80 \text{ GHz}$ achieves a gain of $\approx 6\text{dB}$ and a bandwidth of 55 GHz. This results in $\text{GBP} = 109.7 \text{ GHz}$ and $\text{GBP}/f_T = 1.37$.

The HBT distributed amplifier has a midband transimpedance gain of $45 \pm 1 \text{ dB}\Omega$ and frequency response characteristics similar to those of S_{21} . Its group delay variation is $\pm 30 \text{ ps}$ across the passband. Fig. 9 shows a simulated eye diagram for 30 Gbit/s 2^{15} -1 NRZ pseudo-random bit sequence data. A simple photodiode detector model with a total capacitance of 150 fF and a series resistance of 20Ω was assumed at the input of the amplifier. Sufficient opening of the eyes indicates that the amplifier is potentially capable of handling data rates of up to 30 Gbit/s when employed as an optical receiver.

CONCLUSIONS

The design details of a practical 23 GHz baseband HBT distributed amplifier based upon application of a novel technique have been discussed. This technique renders the amplifier bias stable with respect to moderate ambient temperature variations whilst allowing gain at low frequencies to be maintained, without the use of large emitter decoupling capacitors. Simulations show a midband gain of $11 \pm 1 \text{ dB}$ and a bandwidth extending from 80 kHz to 23 GHz. The GBP/f_T figure of merit is 1.36 and is comparable to current high performance HBT based distributed amplifiers. Results from eye diagram simulations indicate the amplifier's potential for use as a receiver in 30 Gbit/s optical communication systems.

ACKNOWLEDGEMENTS

The authors would like to express their gratitude towards G. A. Pettitt, W. S. Lee, M. G. Jones and A. Hadjifotiou of Nortel Technology (Harlow, Essex, U. K.) for their continuous help and support throughout this project. This work is funded by Nortel Technology and by the EPSRC (U. K.).

REFERENCES

- [1] Madani, K., "New Ultra-Wideband Microwave Amplifiers for 10 Gbit/s Optical Communications", *Microwave Engineering Europe*, pp. 49-56, December/January 1998.
- [2] Shibata, T. *et al.*, "A Design Technique for a 60 GHz-Bandwidth Distributed Baseband Amplifier IC Module", *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 12, pp. 1537-1544, December 1994.
- [3] Borjak, A. *et al.*, "High-Speed Generalized Distributed Amplifier based Transversal Filter Topology for Optical Communication Systems", *IEEE Trans. on Microwave Theory and Tech.*, Vol. 45, No. 8, pp. 1453-1457, August 1997.
- [4] Darwazeh, I. Z. *et al.*, "A Distributed Optical Receiver Preamplifier with Unequal Gate/Drain Impedances", *IEEE International Microwave Symposium Digest*, Orlando, Florida, 16-20 May 1995, pp. 219-222.

- [5] Nelson, B. L. *et al.*, "High Linearity, Low DC Power Monolithic GaAs HBT Broadband Amplifiers to 11 GHz", *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest*, May 1990, pp. 15-18.
- [6] Kobayashi, K. W. *et al.*, "A 50 MHz-55 GHz Multidecade InP-Based HBT Distributed Amplifier", *IEEE Microwave and Guided Wave Letters*, Vol. 7, No. 10, pp. 353-355, October 1997.
- [7] Suzuki, H. *et al.*, "InP/InGaAs HBT ICs for 40 Gbit/s Optical Transmission Systems", *19th IEEE GaAs IC Symposium Digest*, Anaheim, California, 12-15 October 1997, pp. 215-218.
- [8] Kim, M. E. *et al.*, "GaAs Heterojunction Bipolar Transistor Device and IC Technology for High-Performance Analog and Microwave Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 37, No. 9, pp. 1286-1303, September 1989.
- [9] Iqbal, A. and Darwazeh, I. Z., "A Novel Technique for Designing Wideband, Bias Stabilised HBT based Distributed Amplifiers for Optical Receiver Applications", *4th Communication Networks Symposium Digest*, Manchester, England, 7-8 July 1997, pp. 71-77.
- [10] Drew, J. D. *et al.*, "New Active Decoupling Technique Provides Extension to Lower Bandwidth Limit for HBT based MMICs", *5th International EDMO Workshop Digest*, London, England, 24-25 November 1997, pp. 181-186.

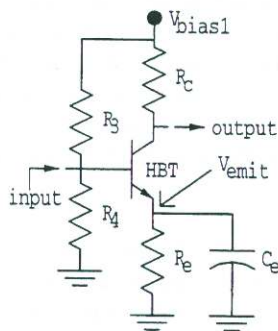


Fig. 1: Common-emitter HBT amplifier with passive emitter resistor bypassing

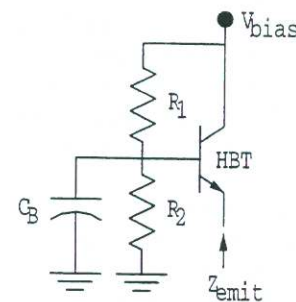


Fig. 2(a): Common-collector HBT circuit

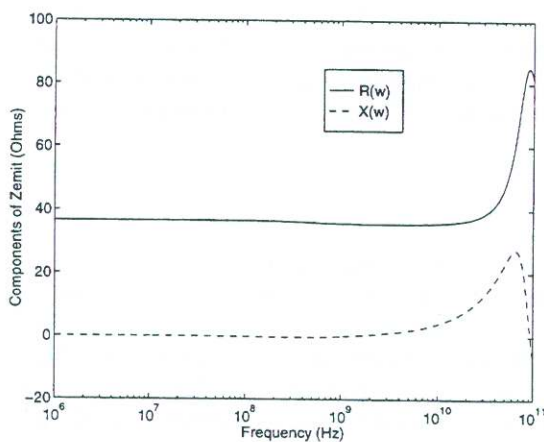


Fig. 3: Resistive and reactive components of Z_{emit}

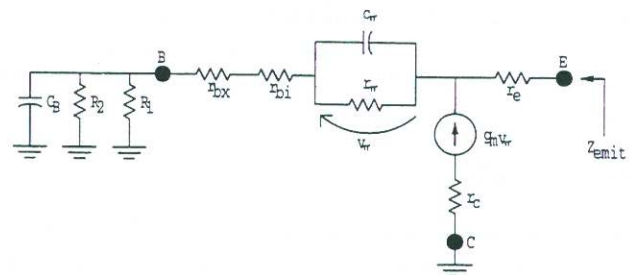


Fig. 2(b): Simplified small-signal common-collector HBT equivalent circuit

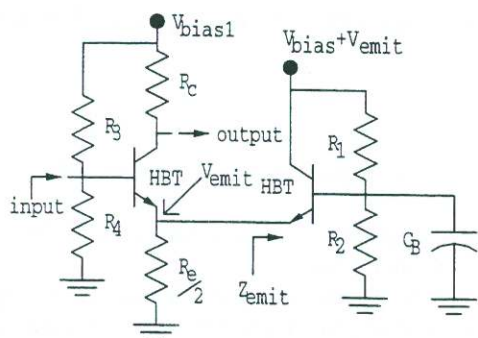


Fig. 4: Common-emitter HBT amplifier with active emitter resistor bypassing

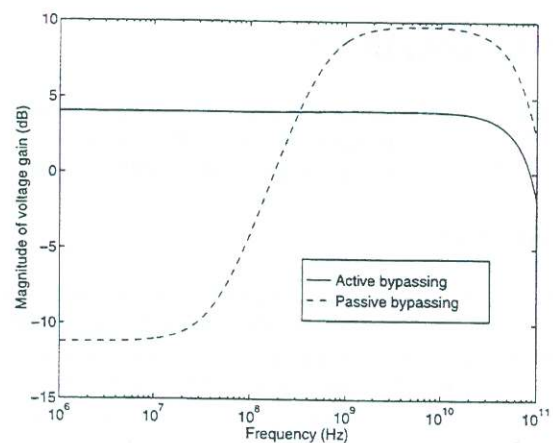


Fig. 5: Voltage gain magnitude for amplifiers utilising active and passive emitter resistor bypassing

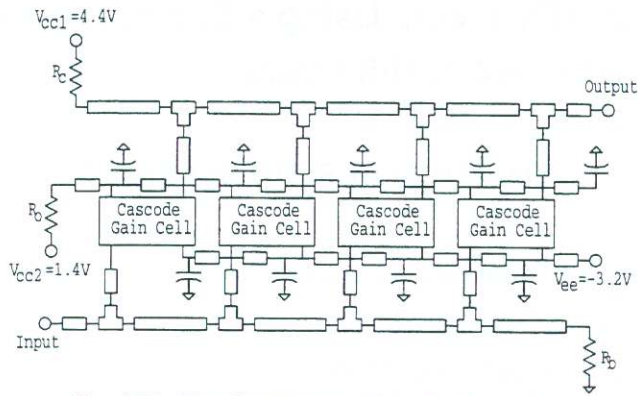


Fig. 6(a): Circuit structure of the HBT based distributed amplifier

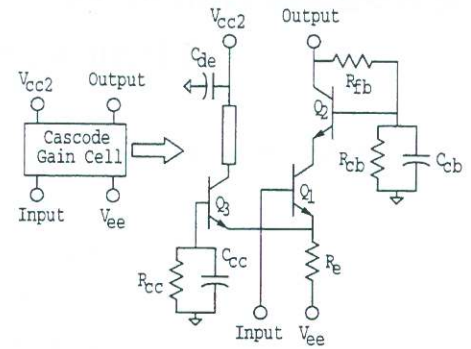


Fig. 6(b): Schematic of the HBT based distributed amplifier cascode gain cell

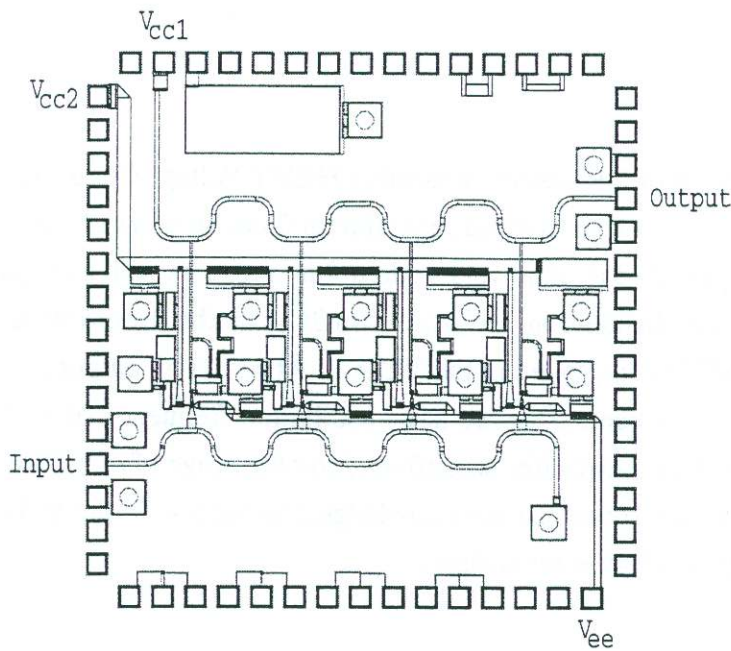


Fig. 7: Layout of the HBT based distributed amplifier MMIC

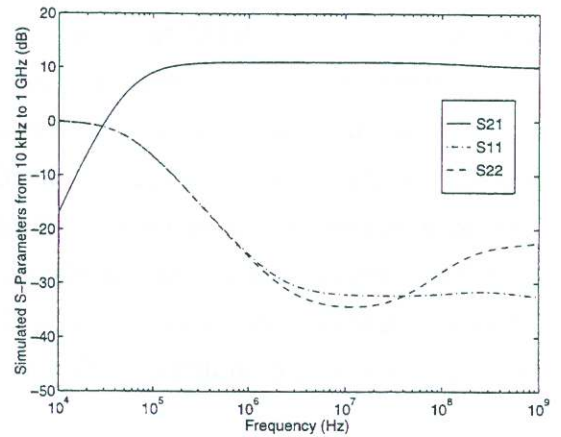


Fig. 8(a): Simulated HBT distributed amplifier S-parameters from 10 kHz to 1 GHz

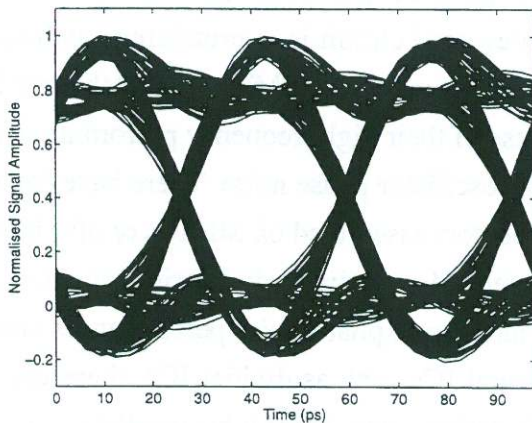


Fig. 9: Simulated 30 Gbit/s eye diagram for the HBT based distributed amplifier

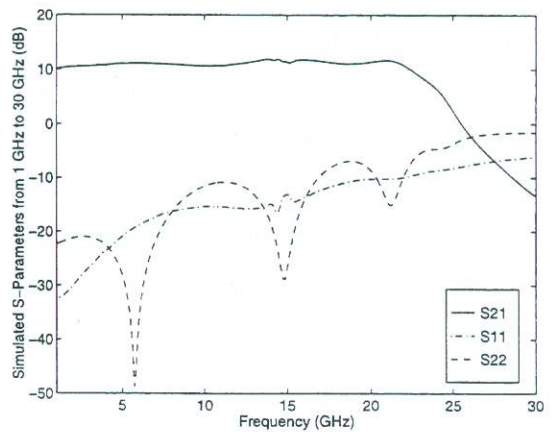


Fig. 8(b): Simulated HBT distributed amplifier S-parameters from 1 GHz to 30 GHz