# A "BACKGATING" MODEL INCLUDING SELF-HEATING FOR III-V FETs

F.Filicori*, A.Santarelli°, G.Vannini*,°, V.A.Monaco*

* DEIS - Department of electronics, computer science and systems, University of Bologna
Viale Risorgimento 2, 40136 Bologna, Italy. e-mail: ffilicori@deis.unibo.it
° CSITE/CNR - Research center for computer science and telecommunication systems
National Research Council - Viale Risorgimento 2, 40136 Bologna, Italy.

## ABSTRACT

A new approach, which takes into account both traps and thermal phenomena is proposed for the accurate modeling of deviations between static and dynamic (e.g., pulsed) drain current characteristics in III-V FETs. The model, which is based on the well known "backgating" concept, can easily be identified on the basis of conventional static drain current characteristics and small-signal, low-frequency S parameters. In the paper, the model formulation is developed along with some hints on its implementation in commercially available CAD tools for HB simulations. Experimental validation, consisting of comparisons between simulated and measured pulsed drain current characteristics, is also provided.

## INTRODUCTION

Accurate nonlinear modeling of III-V FETs for microwave circuit design should also account for low-frequency dispersive phenomena of the electrical characteristics due to deep level traps and surface state densities. These phenomena cause considerable deviations between "static" and "dynamic" (e.g., pulsed) measurements of the DC characteristics, or, if we think in terms of differential parameters, frequency dependent behaviour of the trans-admittance and output impedance even at low frequencies (e.g., lower than 100KHz).

Since microwave large-signal performance prediction involves accurate modeling of both DC and AC components of the drain current, efforts have been made by different research groups [1..10] to take into account low-frequency dispersion both in mathematical and equivalent circuit models.

It must be considered that the time constants associated with dynamic phenomena due to thermal effects, which become relevant in an electron device when large-signal operation is concerned, although somehow longer, are not always very different from those associated with traps or surface states (typically from fractions to hundreds of microseconds). Consequently, dispersion due to "traps" (with this term hereinafter we intend both surface state densities and deep level traps) cannot always be addressed separately from thermal phenomena due to power dissipation.

The empirical modeling approach of dispersive phenomena presented in [5] provides very good predictive capabilities of bias-dependent dynamic drain current deviations due to traps and thermal effects in FETs. Moreover, its technology independence has been widely verified [5,6]. However, due to the need for non-conventional instrumentation for pulsed measurements in the identification phase, its exploitation could result sometimes impossible.

In this paper a different, simplified approach[1] will be presented, which allows for an identification procedure based on conventional DC and small-signal low-frequency (e.g., the lowest operation frequency of a microwave network analyser) S-parameter measurements.

The proposed approach is based on the assumption that the macroscopic effects due to traps on the dynamic drain current may be regarded as a distributed electrical coupling (with very low cutoff frequency) between the gate/drain electrodes and the semi-insulator bulk (*"self-backgating"*) [1,8]. With respect to other recently proposed backgating models [8..10], our approach introduces a different, more convenient and consistent description of low-frequency dispersion due to traps and thermal effects.

[1]It could be shown that a linearisation of the backgating model presented here would lead to a particular case of the empirical model proposed in [5].

## THE BACKGATING MODEL

The backgating concept consists of introducing in the drain current characteristic $F^{DC}$ an equivalent gate voltage $v_{gx}$, as follows:

$$i_d(t) = F^{DC}\{v_{gx}(t), v_d(t)\} \tag{1}$$

$$v_{gx}(t) = v_g(t) + \alpha_g(v_g(t) - V_{g_0}) + \alpha_d(v_d(t) - V_{d_0}) \tag{2}$$

where $V_{g_0}$, $V_{d_0}$ are the average values of the applied voltages $v_g(t)$, $v_d(t)$ and $\alpha_g$, $\alpha_d$ are suitable parameters to be determined. Note that in static conditions we have $v_{gx} \equiv v_g$, while in dynamic operation, at a frequency above the cutoff of dispersive effects, $\alpha_g$ and $\alpha_d$ account for deviations due to traps by feeding back to the gate ("backgating"), dynamic deviations $v_g(t) - V_{g_0}$ of the gate signal and $v_d(t) - V_{d_0}$ of the drain signal.

This approach, although successfully used by some authors [8,9], can accurately predict dynamic deviations of drain current only when self-heating effects due to power dissipation are practically negligible. An improvement of the predictive capabilities of the model can be achieved by introducing a suitable additional power-dependent term. To this end, it is convenient to introduce the dynamic junction temperature deviation:

$$\Delta\theta(t) = \theta_s(t) - \theta_0 \tag{3}$$

which represents the difference between the temperature $\theta_s(t)$ under quasi-static operation and the actual junction temperature $\theta_0$ due to the average dissipated power (which can be assumed constant for operation above the thermal cutoff).

By introducing the thermal resistance $R_\theta$, the deviation $\Delta\theta$ can be expressed as:

$$\Delta\theta(t) = R_\theta(p_s(t) - P_0) \tag{4}$$

where $P_0$ represents the average dissipated power (in dynamic conditions) and $p_s(t)$ is the equivalent "quasi-static" dissipated power (i.e., the power which would be dissipated if $v_g(t)$, $v_d(t)$ were "slowly" time varying voltages, $p_s(t) \doteq F^{DC}\{v_g(t), v_d(t)\} \cdot v_d(t)$).

By assuming a linear dependence of the drain current on the dynamic junction temperature deviation we can write:

$$i_d(t) = [1 + K(p_s(t) - P_0)] \cdot F^{DC}\{v_{gx}(t), v_d(t)\} \tag{5}$$

where $K$ is a suitable thermal coefficient.

Model identification requires the determination of the three parameters $\alpha_g$, $\alpha_d$ and $K$. In order to carry out parameter extraction on the basis of conventional small-signal bias dependent measurements, eqn. (5) can be linearised, taking into account (2), with respect to $v_g(t)$ and $v_d(t)$ around a generic $V_{g_0}$, $V_{d_0}$ quiescent bias condition, leading respectively to:

$$g_m^{AC}\{V_{g_0}, V_{d_0}\} = [1 + K \cdot V_{d_0} \cdot I_{d_0} + \alpha_g] \cdot g_m^{DC}\{V_{g_0}, V_{d_0}\} \tag{6}$$

$$g_d^{AC}\{V_{g_0}, V_{d_0}\} = [1 + K \cdot V_{d_0} \cdot I_{d_0}] \cdot g_d^{DC}\{V_{g_0}, V_{d_0}\} + K \cdot I_{d_0}^2 + \alpha_d \cdot g_m^{DC}\{V_{g_0}, V_{d_0}\} \tag{7}$$

where: $I_{d_0} = F^{DC}\{V_{g_0}, V_{d_0}\}$.

Eqns. (6)-(7), represent the low-frequency dynamic transconductance $g_m^{AC}$ and output conductance $g_d^{AC}$ as functions of the static drain current $I_{d0}$, of its partial derivatives $g_m^{DC}$, $g_d^{DC}$ as well of the three model parameters $\alpha_g$, $\alpha_d$ and $K$. The static transconductance and output conductance terms may be obtained, for instance, through numerical differentiation of the measured DC drain current or by analytical derivation of the mathematical expression used to model the static behaviour of the device. Moreover, $g_m^{AC}$, $g_d^{AC}$ practically coincide with the real part of the corresponding small-signal, low-frequency[2] Y-parameters easily obtainable from S parameter measurements and further application of known matrix transformation formulas. Thus, the determination of the three model parameters can be conducted by minimising, on a suitable grid of bias conditions, the discrepancies between measured dynamic conductances and eqns.(6)-(7). An alternative identification procedure can be also adopted, optimising only the K parameter and determining $\alpha_g$, $\alpha_d$, for each guess of $K$, by applying eqns.(6)-(7) at a particular "nominal" bias condition $\hat{V}_{g_0}$, $\hat{V}_{d_0}$.

[2]A suitable frequency above the cutoff due to dispersive effects but low enough to neglect transistor capacitances.

## MODEL IMPLEMENTATION IN HARMONIC-BALANCE CAD TOOLS

The proposed approach is suitable for easy implementation in commercially available HB-oriented circuit simulators providing user-defined, look-up-table-based nonlinear modeling capabilities such as HP-MDS, HP-EEsof Libra IV, OSA90-Hope. In the following a brief explanation of the implementation in HP-MDS will be given.

In Fig.1 an MDS-like circuit schematic is presented, implementing the proposed backgating approach including thermal phenomena. In particular, the MDS implementation is carried out by means of a six-port Symbolically Defined Device[3], based on the model eqns. (2)-(5). By adopting a look-up table based model, the DC measurements can be made available in the MDS environment by means of the "dataset variables" IgDC, IdDC.

Two out of the six SDD ports provide the gate and drain device currents, while the remaining four ones are used for auxiliary purposes only. In particular, the auxiliary ports are needed in order to evaluate the mean values $V_{g_0}$, $V_{d_0}$, $P_0$ required in the backgating model eqns. (2)-(5). To this aim, an ideal low-pass filtering[4] (lpf) is applied at ports nr. 3, 4, 5 on currents which are numerically coincident with gate and drain instantaneous voltages and instantaneous power respectively. By simply closing the three ports on a 1 $\Omega$ resistance the variables $V_{g_0}$, $V_{d_0}$, $P_0$ are made available as port voltages. Moreover, a current-dependent current source closed on a 1 $\Omega$ resistance and connected at the zero-current port 6 is used to make available a port voltage V6 numerically coincident with the instantaneous drain current. This is necessary to compute the instantaneous power term -V6*V2 (see Fig.1).

The model schematic presented in Fig.1 can be used for nonlinear prediction of the device behaviour both in static and dynamic operating conditions above the cutoff frequency due to dispersive effects. In order to make the circuit suitable also for high frequency large-signal operating condition, an additional modeling of the nonlinear reactive effects is obviously needed. It is worth noting that the proposed approach can easily be embedded both in classic lumped equivalent circuits [9,10] and in look-up table based mathematical large-signal models [11].

## EXPERIMENTAL RESULTS

The described modeling approach has been tested on a Philips CFX32 MESFET device, whose DC drain current characteristics are shown in Fig.2. As can be clearly seen from the negative slope at high $V_{g0}$, $V_{d0}$ values, relevant self-heating effects take place in the device.

In order to evaluate the predictive accuracy of the proposed model and to highlight the role played by the additional power-dependent term, both the 2-parameter model (eqns. 1-2) and the 3-parameter one including the thermal correction (eqn. 2-5) have been identified by means of the minimisation procedure previously described.

In Figs.3-4 the predicted dynamic drain current values are compared with measurements obtained applying short, simultaneous voltage pulses at the gate/drain electrodes starting from the quiescent condition $V_{g_0}$=-2V, $V_{d_0}$=3V. As clearly appears, more accurate prediction of the drain current and its slopes is achieved with the three-parameter modeling approach.

In Fig.5 the same set of pulsed drain characteristics is compared with predictions obtained with the empirical model for dispersive effects proposed in [5]. It is worth noting how, despite of its dependence on only three "global" parameters, the backgating model including the self-heating correction term provides prediction capabilities of dynamic drain current deviations almost comparable[5] with the model in [5].

In Figs.6-7 the dynamic drain current characteristics, predicted with the 2- and 3-parameter model are compared with pulsed measurements, for another quiescent bias condition $V_{g_0}$=0V, $V_{d_0}$=5V. Also in this case the agreement is definitively better using the 3-parameter model.

[3]SDD is a particular MDS capability allowing for implementing nonlinear multi-port components, with port currents defined as nonlinear algebraic functions of port voltages, possibly followed by a frequency dependent filtering.

[4]The ideal low-pass filter, simply defined as an additional *dataset variable*, can be chosen with a cutoff frequency comparable with that competing to the dispersive effects due to traps and thermal phenomena. For the results presented in the following section a 10 KHz value has been set.

[5]Actually, the empirical model in [5] allows for a more reliable prediction of the drain current dynamic deviations over a wider range of quiescent bias conditions.

Finally, in Figs.8-9, the derivatives with respect to $V_g$ and $V_d$ of the measured and predicted dynamic drain current characteristics for the quiescent bias condition $V_{g_0}$=-2V, $V_{d_0}$=3V (Fig.4), are shown. Despite model prediction for this quiescent bias point is not as good as for the quiescent bias condition of Fig.7, the agreement is pretty good taking also into account the simplicity of the proposed model which is based on only three "global" parameters.

## ACKNOWLEDGEMENT

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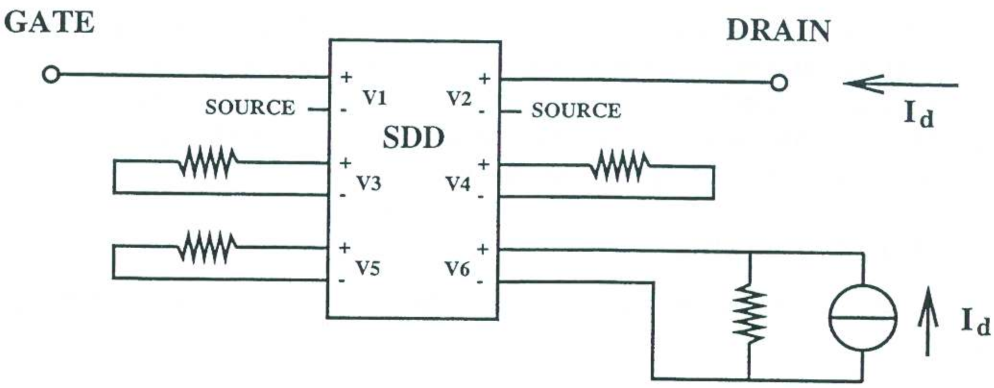



**PORT CURRENTS**

| PORT | WT. FCN. | EXPRESSION = I |
|---|---|---|
| 1 | 0 | IgDC[V1,V2] |
| 2 | 0 | (1 + K*(ps-V5))*IdDC[vgx,V2] |
| 3 | 2 | -V1 |
| 4 | 2 | -V2 |
| 5 | 2 | -V6 * V2 |
| 6 | 0 | 0 |

**WEIGHTING FUNCTIONS**

| WT. FCN. | EXPRESSION |
|---|---|
| 0 | 1 |
| 2 | lpf |

**EQUATION** vgx = V1 + AG*(V1-V3) + AD*(V2-V4)

**EQUATION** ps = V2* IdDC[V1,V2]

Fig. 1: HP-MDS implementation of the proposed backgating approach including thermal phenomena. In the figure, $IgDC, IdDC$ are the "dataset variables" corresponding to the gate and drain static current look-up tables and $K, AG, AD$ the three model parameters. Currents are defined positive when flowing into the SDD. Resistances value: 1Ω.

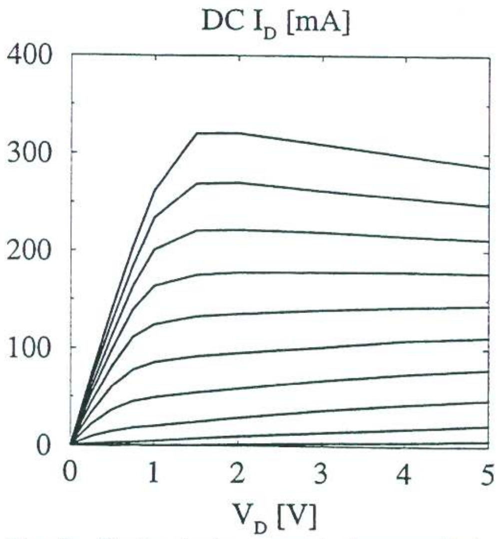



Fig. 2: Static drain current characteristics for a Philips CFX32 GaAs MESFET.

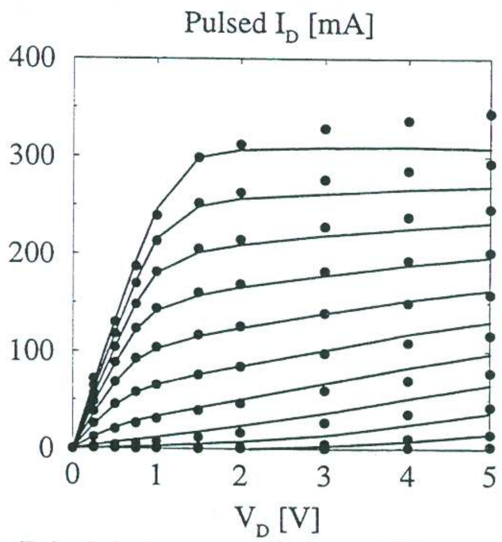
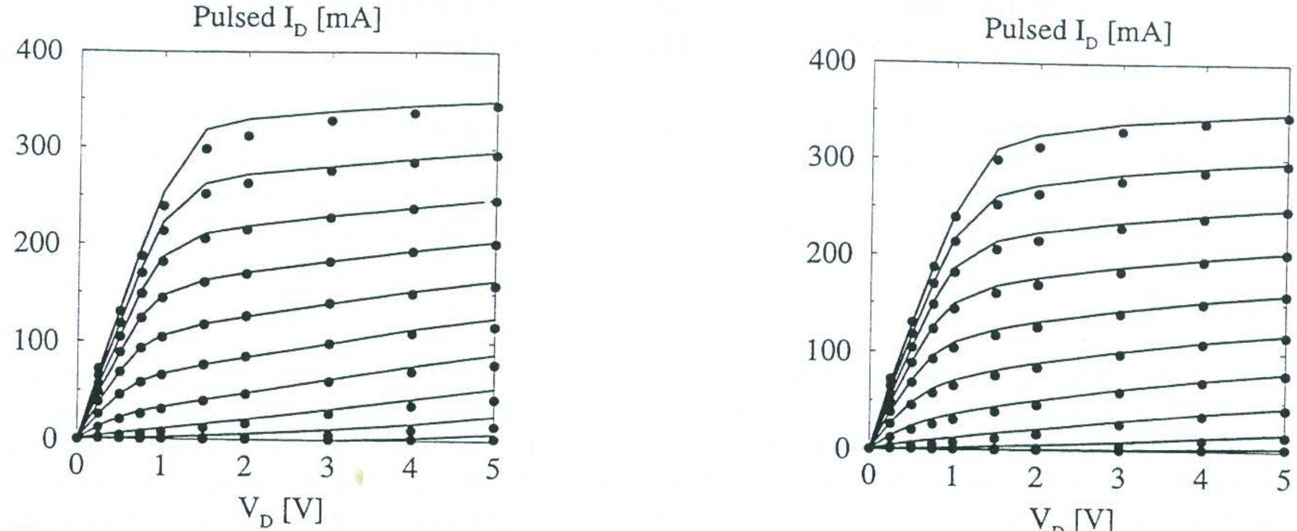
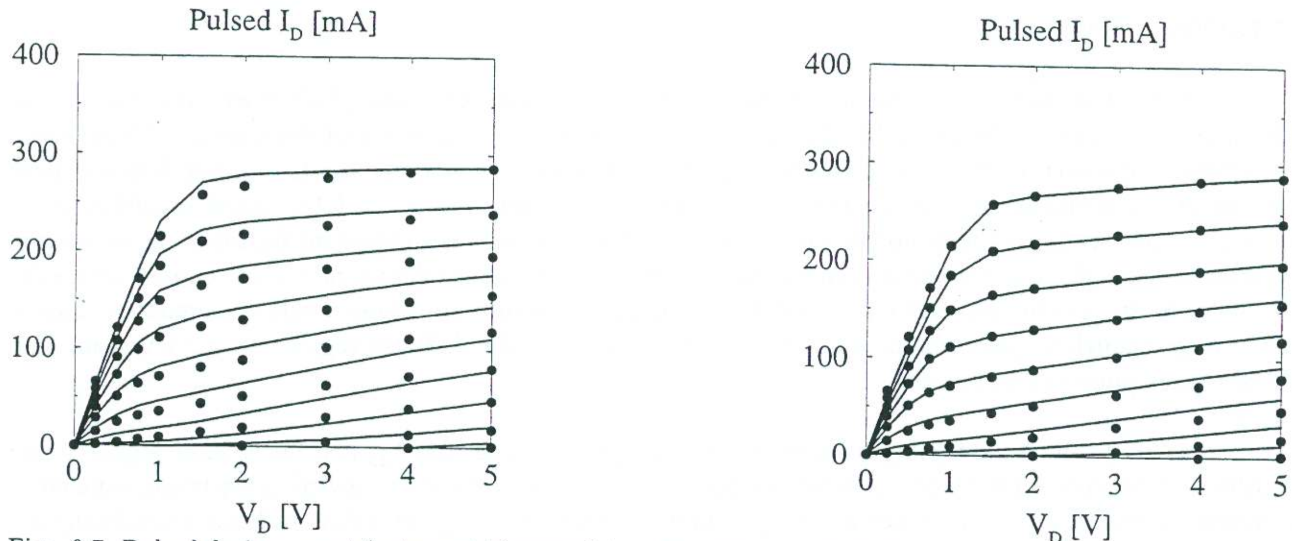


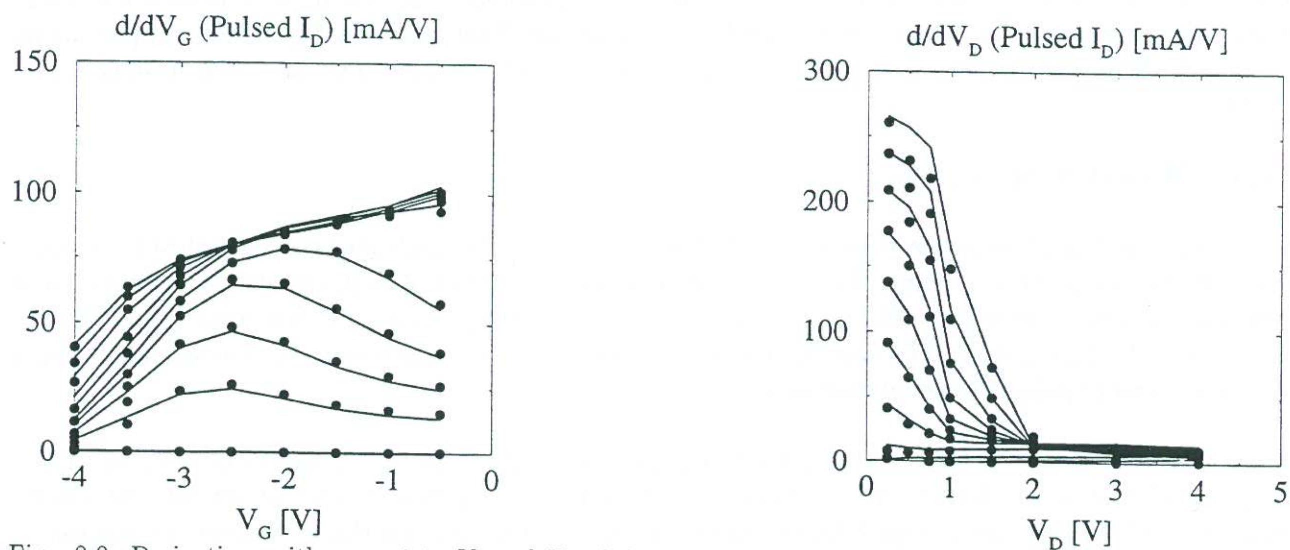

Fig. 3: Pulsed drain current (quiescent bias condition: $V_{g_0}$=-2V, $V_{d_0}$=3V). Comparison between measurements (•) and predictions (—) with the 2-parameter backgating model (eqns. 1-2).




Figs. 4,5: Pulsed drain current (same quiescent condition as Fig.3). Comparison between measurements (•) and predictions (—) with the 3-parameter backgating model (left) including self-heating (eqns. 2-5) and with the empirical model presented in [5] (right).




Figs. 6,7: Pulsed drain current (quiescent bias condition: $V_{g_0}$=0V, $V_{d_0}$=5V). Comparison between measurements (•) and predictions (—) with the 2-parameter backgating model (left) and the 3-parameter one including self-heating (right).




Figs. 8,9: Derivatives with respect to $V_g$ and $V_d$ of the measured (•) and predicted (—) pulsed drain current characteristics in Fig.4.