IMPROVING PERFORMANCES OF LOW-VOLTAGE POWER AMPLIFIERS BY SECOND-HARMONIC MANIPULATION

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ABSTRACT

The effect of second-harmonic loading on power amplifiers operated with a low-voltage supply is investigated. Closed-form expressions and design formulas are derived, making use of a simplified device model. The correctness of the assumptions and the range of validity of the derived expressions is then verified by means of a full non-linear analysis method and model: a sample low-voltage design for a power stage is performed, demonstrating the potentials of the method.

INTRODUCTION

Commercial applications of microwave circuits are pushing towards an increase of component's performances; moreover, the key element in many subsystems is the output stage, that must, at the same time, fulfil tight constraints on output power and efficiency. As an example in digital cellular communication, both the GSM and NADC standards, even with different modulation schemes and linearity requirements, demand the use of an high-efficiency power stage. An high efficiency may be utilised for an increased output power for the same dc consumption; conversely a reduction of the dc input power required to produce the same output power allows reduction in the size of the power supply and/or batteries. The percentage reduction in the dissipated power can be appreciable, allowing greatly reduced size and weight of the heatsink. The lower power dissipation also permits a reduction in the device junction temperature, with a consequent improvement in reliability [1]. Moreover, modern systems impose an upper limit for the biasing voltages, leading to a low-voltage design: the peculiar characteristics of this operating mode have not been fully exploited to date, and design methods not clearly defined. In most cases, the design strategy is to employ a design approach of the "tuned load" [2,3] or Class-F" [4,5] type, to take advantage of the inherent increase in power-added efficiency deriving from such approaches. More exotic operating classes can be used as well, including Class D or E [6,7] operation. In this paper an alternative approach, based on the manipulations of harmonic output signal components, is proposed and its performances compared with well-established techniques.

In high-efficiency power amplifier design techniques, a major effort from the designer is devoted to the choice and realisation of a suitable harmonic terminating scheme. For instance, if a "tuned load" operation is considered, the circuit topology is of the type shown on fig.1: fundamental-frequency output load is chosen according to some criterion (e.g. of the simplified [8] or fully non-linear [9] type), while higher harmonics are short-circuited by a number of resonant circuits. If a "class-F" approach is selected, short and open circuit terminations must be presented at the output of the device at even and odd harmonics respectively, as in fig.2, in order to synthesise as much as possible a square-wave like output voltage. A number of possible modifications to those approaches are possible, but the general philosophy is to minimise dissipated dc power on the active device appropriately shaping the current and/or voltage waveforms: in particular, maximum output voltage must occur at low (or zero) current levels and maximum current corresponding at very low voltages. Class-F or tuned load approaches, on the other hand, try to fulfil such criteria in a symmetric way, e.g. obtaining an output voltage waveform symmetrical around the bias point, due to the absence of even harmonic components. This is a suitable approach as far as maximum output power operation is concerned, i.e. if the full swing of output current and voltage can be exploited: power

performances are limited by the constraints imposed by physical limitations of the device, as gate-drain breakdown, gate-source junction forward conduction, device pinch-off and ohmic region. Optimum power performances are obtained biasing the device midway between physical limits and synthesising therefore a symmetrical voltage waveform. In low voltage operation, this picture is drastically modified: biasing voltages are dictated by the tight constraint on the minimisation of the number of battery cells. For this reason, active devices for low voltage operation should be characterised by a very low knee voltage (i.e. the output voltage marking the end of the device ohmic zone) and an high drain current, typically balanced with a reduction of the device breakdown voltage. The output voltage swing is limited therefore by the device ohmic zone and not by the gate-drain breakdown. In this situation, a major improvement of power performances can be obtained utilising a second-harmonic manipulation of the output voltage: the presence of a second-harmonic voltage component could actually flattens the voltage waveform for half of the cycle and peaks it in the remaining part (fig. 3); if this situation occurs with a proper phase relationship, as in fig. 3a, the dissipated dc power is minimised, and the resulting output power and efficiency increased. The basic scheme implementing such condition is depicted in fig.4.

MAIN ASSUMPTIONS AND VOLTAGE WAVEFORMS

The device output acts as an ideal current source, linearly controlled by the input gate-channel voltage, with an output impedance assumed to be linear and represented by the shunt connection of a drain-source resistance (R_{ds}) and capacitance (C_{ds}); in this condition, the drain-source voltage waveform depends on the harmonic terminations, i.e. it can be expressed as:

$$V_{ds}(t) = V_{ds,DC} - \mathrm{Re}al\left(\sum_{i=1} V_{ds,i\cdot f_0} \cdot e^{j2\pi i f_0 t}\right) = V_{ds,DC} - \mathrm{Re}al\left(\sum_{i=1} Z_{L,i\cdot f_0} \cdot I_{d,i\cdot f_0} \cdot e^{j2\pi i f_0 t}\right) \quad (1)$$

where $Z_{L,if0}$ is the termination presented to the i-th harmonic current component at the intrinsic drain terminals and $V_{L,if0}$ is the resulting drain voltage harmonic component. Since a complex termination may result in poorer performances for the power stage, we will focus our study on resistive ones, i.e. $Z_{L,if0}$ will be assumed as a purely resistive impedance. Circuit complexity and modelling issues suggest the control of the minimum number of harmonics. This results on the control of second and third harmonic components only.

If the harmonic terminating scheme is the "tuned load" one, i.e. if every harmonic component is loaded by an ideal short-circuit termination ($Z_{L,if0} = 0$, $i \geq 2$), the resulting voltage waveform is a pure sinusoid. When, as in the present case, the 1st and 2nd harmonic terminations are considered, the voltage waveform may be expressed as the sum of a DC, fundamental and second-harmonic components, i.e.:

$$V_{ds}(t) = V_{ds,DC} - V_{ds,fo} \cdot \cos(2\pi f_o t) - V_{ds,2fo} \cdot \cos(2 \cdot 2\pi f_o t) =$$

$$= \mathrm{V}_{ds,DC} - V_{ds,fo} \cdot \left[\cos(2\pi f_o t) + \frac{1}{\varepsilon_2} \cdot \cos(2 \cdot 2\pi f_o t)\right] \quad (2)$$

where $\varepsilon_2 = \dfrac{V_{ds,fo}}{V_{ds,2fo}} = \dfrac{R_{L,fo}}{R_{L,2fo}} \cdot \dfrac{I_{d,fo}}{I_{d,2fo}}$ is defined as the fundamental to second harmonic voltage components ratio. It is to note that the voltage waveform depends on the sign of ε_2, as it can be noted from fig. 3. The 2nd harmonic voltage component must be "out-of-phase" with respect to the fundamental one to properly flatten the voltage waveform (fig. 3a), i.e. the sign of the two voltage components must be opposite, in order to avoid what happens in fig. 3b. To obtain such a behaviour however, output current harmonic components must appear with the proper phase relationship: in particular, the second-harmonic current component, as generated by device nonlinearities (mainly by the device pinch-off limitation and/or input diode forward conduction), must be opposite in phase with the fundamental-frequency component. If this is not the case, proper input and/or output complex harmonic terminations must be employed.

The "hard" limitations of the device constrain the flattened voltage waveform not to exceed a minimum (knee voltage) and a maximum (breakdown voltage) value: under the assumption of a low voltage design, i.e. neglecting the occurrence of the device gate-drain breakdown, only the minimum value of the drain voltage waveform is concerned. Such minimum value(s) can be easily derived from **(2)**; the angles at which the minima occur are functions of ε_2:

$$\begin{aligned} &\omega_0 \cdot t_x = 0 && \text{if } \varepsilon_2 < -4 \\ &\omega_0 \cdot t_x = \pm acos\left(\frac{-\varepsilon_2}{4}\right) && \text{if } \varepsilon_2 > -4 \end{aligned} \qquad (3)$$

Is possible to define a "Gain Coefficient" $\beta(\varepsilon_2)$ as the ratio between fundamental frequency component and the minimum value (excluding DC) assumed by the voltage waveform, i.e.:

$$\beta(\varepsilon_2) \equiv \left| \frac{V_{ds,f_0}}{V_{ds}(t_x) - V_{ds,DC}} \right| = \frac{1}{\cos(\omega_0 \cdot t_x) + \frac{1}{\varepsilon_2} \cdot \cos(2\omega_0 \cdot t_x)} \qquad (4)$$

Using such a coefficient, the time-varying (RF) part of the voltage waveform can be normalised:

$$V_{ds,norm} = -\beta(\varepsilon_2) \cdot \left[\cos(2\pi f_o t) + \frac{1}{\varepsilon_2} \cdot \cos(2 \cdot 2\pi f_o t) \right] \qquad (5)$$

The overshoot factor $K(\varepsilon_2)$ can be defined as

$$K(\varepsilon_2) \equiv V_{ds,norm}\Big|_{t=\frac{1}{2f_o}} = -\beta(\varepsilon_2) \cdot \left(-1 + \frac{1}{\varepsilon_2} \right) \qquad (6)$$

The gain coefficient $\beta(\varepsilon_2)$ behaviour *vs.* ε_2 is plotted in fig.5, where the voltage waveform peak value $K(\varepsilon_2)$ is also shown.

The gain coefficient $\beta(\varepsilon_2)$ can be interpreted as the increase in fundamental frequency amplitude allowed by the use of a 2nd harmonic component with the proper phase. It means that, for a given voltage limitation imposed by the device (knee voltage), a greater fundamental voltage component and therefore higher output power can be obtained. Moreover, since the drain current is not modified (at least to a first approximation) by the harmonic terminations, the DC power dissipation remains unaffected, leading to an increased drain efficiency.

The allowed increase in the fundamental frequency voltage component that can be obtained using a 2nd harmonic manipulation procedure ($V_{ds,fo/H2}$) over the tuned load value ($V_{ds,fo/TL}$) can be therefore expressed by:

$$V_{ds,fo}\Big|_{H2} = \beta(\varepsilon_2) \cdot V_{ds,fo}\Big|_{TL} \qquad (7)$$

As a consequence, the output power and drain efficiency can be written in terms of the corresponding Tuned Load quantities:

$$P_{RF,H2} = P_{RF,TL} \cdot \beta(\varepsilon_2) \qquad (8)$$

$$\eta_{d,H2} = \eta_{d,TL} \cdot \beta(\varepsilon_2) \qquad (9)$$

SAMPLE DESIGN

In order to demonstrate the effect of the proposed harmonic terminating scheme for a low voltage design (V_{DD}=3 V), three stages have been designed, employing a tuned load, Class F and second harmonic tuning respectively; the device selected is a medium power MESFET from GMMT with a Class AB gate bias; the device model used is a modified Materka full non-linear one, extracted using multibias S-parameter pulsed-dc measurements. For each design, the choice of the fundamental-frequency load has been optimised by means of the technique in [9] and input termination has been selected to get maximum input power transfer at large-signal (conjugate large-signal input match). The design rationale is the following: for a given drive level (9 dBm in this

case), the output drain current waveform and its harmonic components are the same for the three harmonic terminating schemes and harmonic amplitude and phase manipulation is possible imposing different harmonic terminations. In particular, for the Tuned Load case, harmonic voltage components are not present (short-circuit output terminations), leading to a purely sinusoidal output voltage waveform. For the Class-F design, an open circuit termination imposed at third harmonic generates a third-harmonic voltage component through the device output conductance; this component has already the correct phase relationship with the fundamental one, so leading to a symmetric flattening of the voltage waveform, with a corresponding increase in output power and power added efficiency. In the case of second-harmonic manipulation proposed in this contribution, the use of output harmonic terminations is not sufficient to achieve a proper phase relationship between the fundamental and second harmonic components. These can be easily demonstrated from a Fourier analysis of the assumed drain current waveform [2,3]. The use of an input second harmonic manipulation is therefore necessary, for instance simply terminating the device input on the same fundamental impedance. In this way, the voltage waveform shaping can be performed by simply loading the device with an output resistive load at second harmonic.
The voltage waveforms for the three different cases, at the same input drive level, are shown in figure 6, while the corresponding load curves are shown in figure 7, superimposed on the output characteristics.
Output power and power-added efficiency are plotted in fig. 8 and 9 respectively. An increase of 40.7% over the Tuned Load solution has been demonstrated for the output power, while the power-added efficiency shows a corresponding increasing of 36.5 %, well in agreement with the expected values forecasted by the gain coefficient. For sake of completeness, the relevant improvements with respect the indicated Class-F solution, result to be 32 % for Pout and 25.5 % for PAE, so demonstrating the effectiveness of the proposed second-harmonic manipulation scheme. Moreover, the control of second harmonic component has been achieved by simple circuit topologies.
As noted before, another aspect of the second-harmonic manipulation is the voltage waveform peaking toward gate-drain breakdown; this effect may be a problem only if maximum output power is requested from the device, but it is not in the present case of low-voltage operation. As it is possible to note from fig.6 and 7, voltage peaking does not reach 8 V, corresponding to an overshooting of 1.93, well away from gate-drain breakdown phenomena in actual devices and well in agreement with the factor $K(\varepsilon_2)$ (fig.5).

CONCLUSIONS

The potential of second-harmonic loading on power amplifiers, operating at low-voltage, has been demonstrated. Using the inherent non-linearities of an actual devices, the second harmonic output current component, with the proper phase, has been generated and utilised in order to produce the right voltage waveform shaping. A major improvement in output power, gain and PAE has been obtained in a sample low-voltage design of a power stage.

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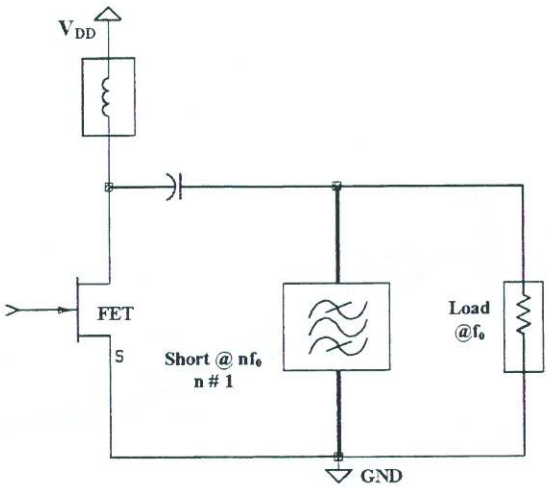

Figure 1: Harmonic terminating scheme for the tuned load design

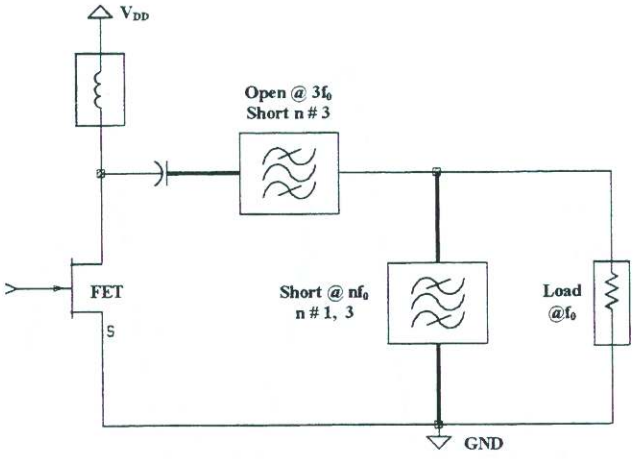

Figure 2: Harmonic terminating scheme for the Class F design

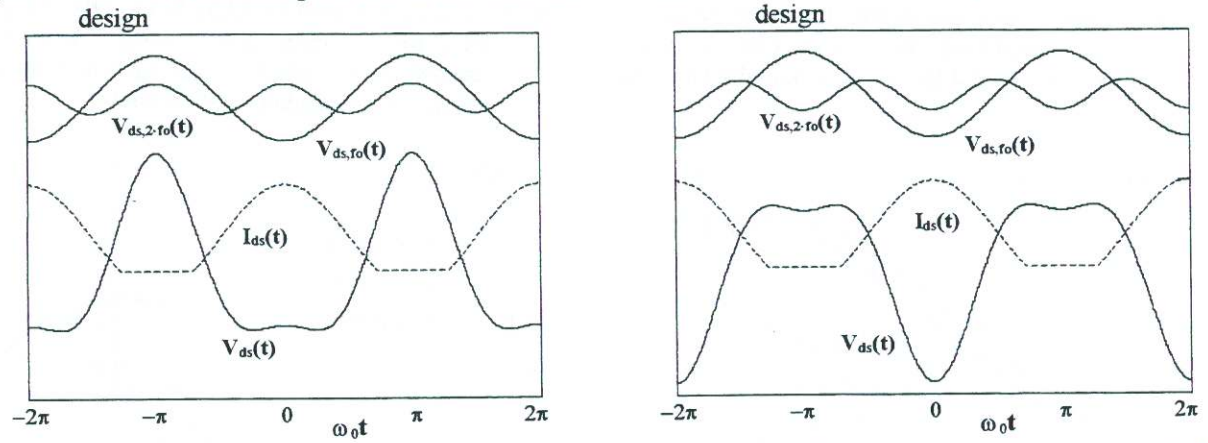

Figure 3: Output voltage as the sum of a DC, fundamental and second harmonic components: (a) out-of-phase components, (ε_2<0) and (b) in-phase components (ε_2>0).

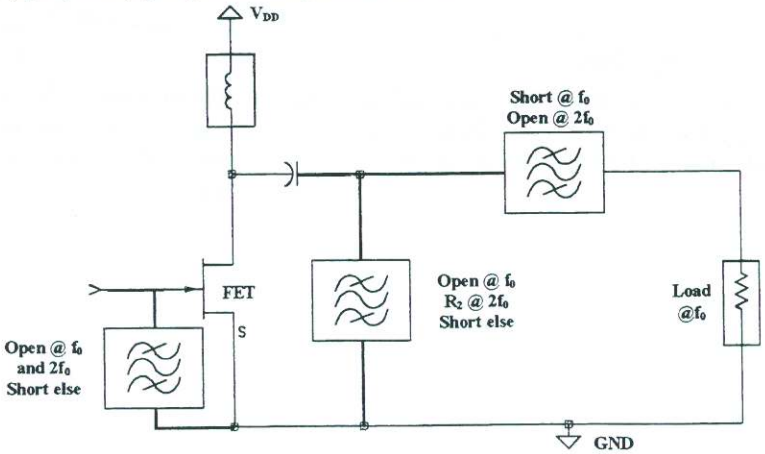

Figure 4: Harmonic termination scheme for the proposed second harmonic manipulation

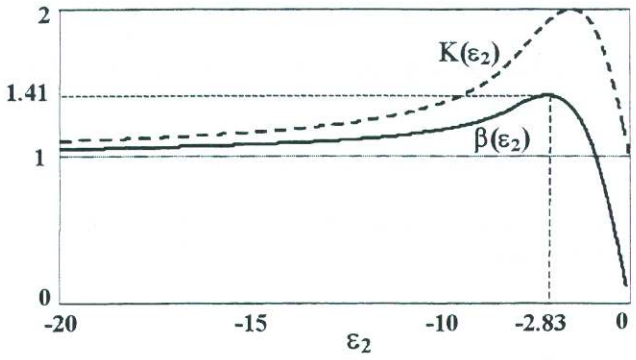

Fig.5: Gain coefficient $\beta(\varepsilon_2)$ (solid line) and overshoot factor $K(\varepsilon_2)$ (dashed line) as functions of the ratio between fundamental and second harmonic voltage components (ε_2).

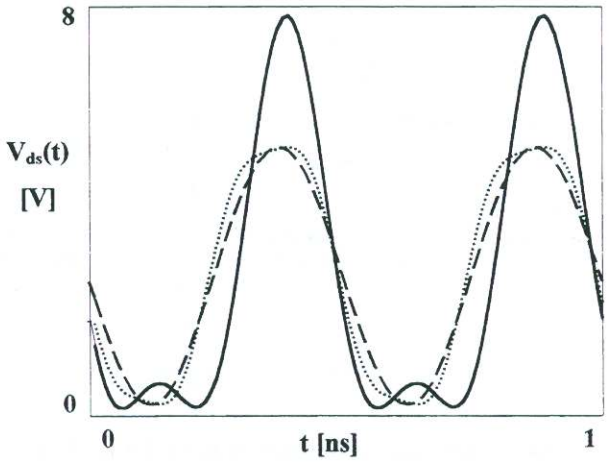

Figure 6: Output voltage waveforms for the three design cases: Tuned load (dashed line), Class-F (dotted line) and Second-Harmonic Manipulation (solid line)

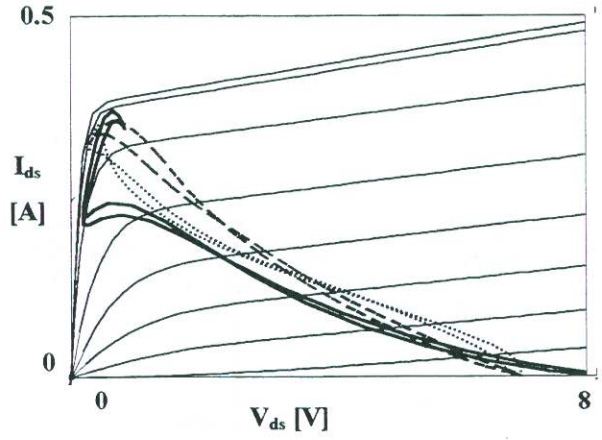

Figure 7: Load curves corresponding to the selected drive level for the three design cases: Tuned load (dashed line), Class-F (dotted line) and Second-Harmonic Manipulation (solid line)

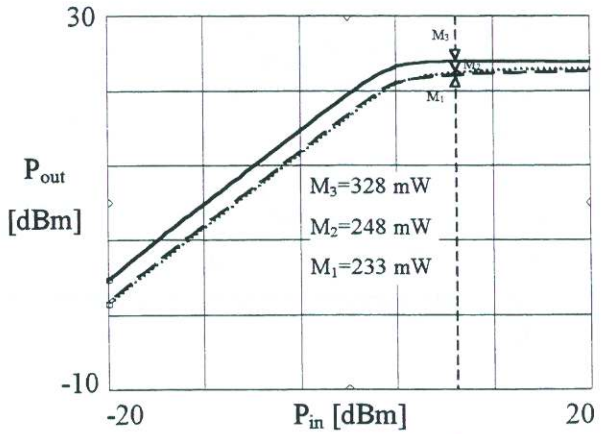

Figure 8: Output power for the three reference cases: Tuned load (dashed line), Class-F (dotted line) and Second-Harmonic Manipulation (solid line)

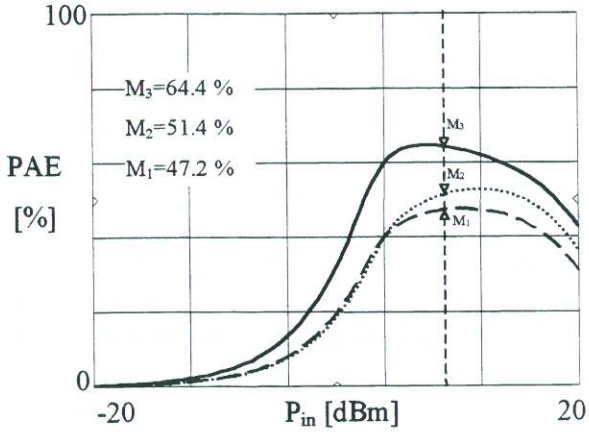

Figure 9: Power-added efficiency for the three reference cases: Tuned load (dashed line), Class-F (dotted line) and Second-Harmonic Manipulation (solid line)