Adjustable Pulse Shaping Filter with Active Impedance Matching for Optical Soliton Communication Systems

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ABSTRACT

It will be presented the design and the experimental results of a monolithic post-detection filter suitable for a 10 Gbit/s optical soliton receiver. The main advantages are full integration, electrical tunability and active input and output impedance match.

INTRODUCTION

In the design of optical soliton systems at multigigabit transmission rates, special care must be given to the post-detection receiver filter. This filter has the main function to reshape the received soliton pulses providing well defined pulses with low intersymbol interference and low telegraph distortion, at the input of the decision circuit. It has also the function of reducing the noise at the input of this device. A well designed post-detection filter, effecting appropriate pulse shaping, can improve significantly the performance of the optical system. However, there are constraints in filter design: it must be easily fabricated, insensitive to manufacturing tolerances, have a reasonable physical size and must also easily integrated with the other optical receiver components. The filter must also present a good input and output impedance match in the frequency range where the signal energy is concentrated, to avoid the back reflections. These reflections can deteriorate significantly the system performance, Hauenschild and Rein (1). The electrical tunability is other requirement in order to adjust the filter for different soliton pulse widths and also to compensate the changes in nonideal receiver response or other distortions due to ageing and temperature variations. We will present an active post-detection filter with a broadband impedance match and electrically adjustable, developed for an optical communication system demonstrator of the European Community project, ACTS 045, "UPGRADE".

CIRCUIT DESCRIPTION

Figure 1 shows a simplified circuit diagram of the designed filter. The filter input stage uses a common-gate (CG) configuration FET with the bias resistors R_{s1}, R_{g1} and R_{d1}. This stage provides an active input impedance matching in a very broadband frequency range, Niclas (2). At frequencies reasonably lower than the transition frequency of the FET device, F_T, the input impedance of this stage (neglecting the effect of R_{s1}) is given by:

$$Z_{in}^{'} \approx r_s + \frac{r_{ds} + R_L}{1 + g_m r_{ds}} \qquad (1)$$

where r_s is the FET source resistance, r_{ds} the drain-source resistance, g_m is the transconductance and R_L is the load resistance of the CG stage. The product $g_m \times r_{ds}$ is approximately independent of the channel width, depending only on the device polarisation. For the process used this product takes values ranging from 11 to 16.6 for a drain current from $0.17 \times I_{dss}$ to $1 \times I_{dss}$ (3) where I_{dss} is the drain-source saturation current. For these relative high values of $g_m \times r_{ds}$ and neglecting the low value of the rs, the input resistance of the CG configuration can be approximated by:

$$Z_{in}^{'} \approx \frac{1}{g_{mo}}\left(1+\frac{R_L}{r_{ds}}\right) \qquad (2)$$

From the above expression we can conclude that the input resistance is inversely proportional to the transconductance of the active device. Then, adjusting the FET bias, the input impedance can be electronically tuned for minimum return-loss. For high values of r_{ds} this stage performs a good isolation between input and output ports and therefore attenuates the filter back reflections at the attenuation band. Other advantage of using a CG stage is to transform the input impedance (50 Ω) into a high impedance ($\cong R_{d1}$) over a very wide frequency range. Figure 2 shows the predicted input and output impedance of the CG stage, taking into account the parasitic elements of the HEMT for a frequency range from approximately DC to 20 GHz. It can be observed that this impedance translator transforms, in a very broadband frequency range, the 50Ω input impedance into a higher output impedance ($Z_{CGout} \cong 135\Omega$). The high output impedance provided by the CG reduces significantly the filter capacitor values, which allows the use of voltage variable capacitors (VARICAPs) to perform a fine filter tuning. The VARICAPs were realised using reverse biased diodes, D_1 and D_2 (Figure 1). These capacitors associated with the inductance L_1, L_2 form the basic filter network. The filter elements were optimised to convert the soliton pulses at the input of the optical receiver to pulses near a 100% raised cosine format. Table 1 compares the optimised element values of the designed filter with the values obtained for a conventional 50Ω double terminated LC ladder filter with an identical frequency response. It can be observed that by using the impedance translator the capacitor values were reduced more than 80% compared with a conventional filter.

The output stage has the main functions to isolate the filter from following stages and also to provide a lower output impedance ($\cong$ 50Ω). The capacitors C_3, C_4 and C_5, were included for filtering the bias V_g, V_{c1} and V_{c2} respectively.

The equalizer was implemented on MMIC GaAs process D02AH from Philips Microwave Limeil (PML). This process provides Field Effect Transistors with high electron mobility (HEMT) with very short gate lengths (0.2μm). The HEMTs of D02AH process have typical values of F_T=62 GHz and N_F= 0.9 dB @ 12 GHz with G_A=11.5 dB (3). The filter layout is shown in Figure 3, the chip size is 1×1.5mm and has 100 μm of thickness.

EXPERIMENTAL RESULTS

The MMIC was mounted on a designed package and connected to the external circuits by using bond-wires.

Figure 4 a) and b) compares the measured frequency response (|S21| @ 50Ω) of the active pulse shaping filter (solid line) with the simulation (dashed line) and with the idealised target response (dotted line), on logarithm and linear scales, respectively. From these figures we can observe that the simulated and predicted transfer functions are very close in a broadband frequency range and also that this filter provides a good out of band insertion loss providing an efficient signal noise reduction.

Figure 5 illustrates the filter frequency responses for two different sets of VARICAP voltages. We can observe that by adjusting the VARICAP voltages is possible to change the filter frequency response in order to allow a fine filter tuning.

Figures 6 a) and b) show respectively the experimental input and output impedance match of the active filter at 50Ω. These results are also compared with the impedance match of a theoretical 50Ω double-terminated LC ladder filter . It is possible to observe the great advantage of using active impedance match: the active filter exhibits an experimental input and output impedance match better than 10dB, for the frequency ranges greater than 15GHz and 20 GHz respectively. A 50Ω double-terminated LC ladder filter has only impedance match greater than 10dB for frequencies less than 2 GHz.

Figure 7 shows the computed eye diagram from the frequency data for a pseudo random bit sequence with a length 2^7-1 where it can be observed a good eye opening, vertically and horizontally, with low intersymbol interference and low telegraph distortion.

CONCLUSIONS

A novel post-detection filter with electrical tunability and active input and output impedance matching has been implemented. The electrical tunability has the advantages to optimise the performance of the optical front end for different pulse widths and formats and also compensate the changes in nonideal receiver response or other distortions due to ageing and temperature variations. The filter exhibits a good input and output impedance match to avoid the performance degradation due to the back reflections. The filter was designed in GaAs MMIC technology in order to have a small physical size and allows the integration with the other receiver componentes.

ACKNOWLEDGEMENT

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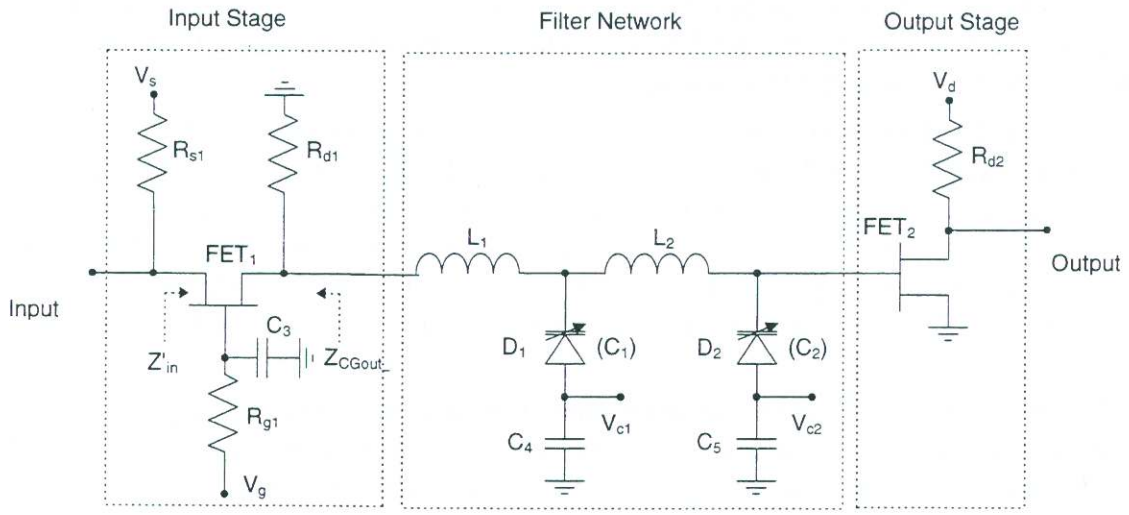


Figure 1. Circuit diagram of the GaAs MMIC filter with active input and output matching.

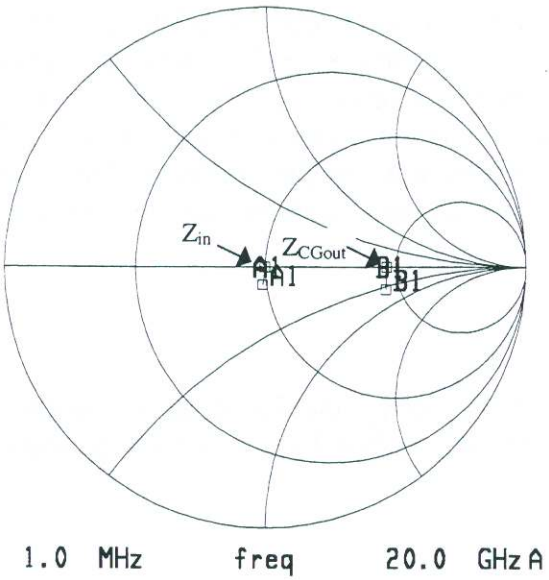


Figure 2. Predicted input and output impedance of the CG stage

	LC Ladder Filter with Active Impedance Translator	LC Ladder Filter 50Ω double-terminated
C_1	94 fF	575.5 fF
C_2	127 fF	868.5 fF
L_1	4.1 nH	1.3 nH
L_2	6.0 nH	4.1 nH

Table 1. Comparison of the optimised element values of the designed filter with the values of an 50Ω double-terminated LC ladder filter.

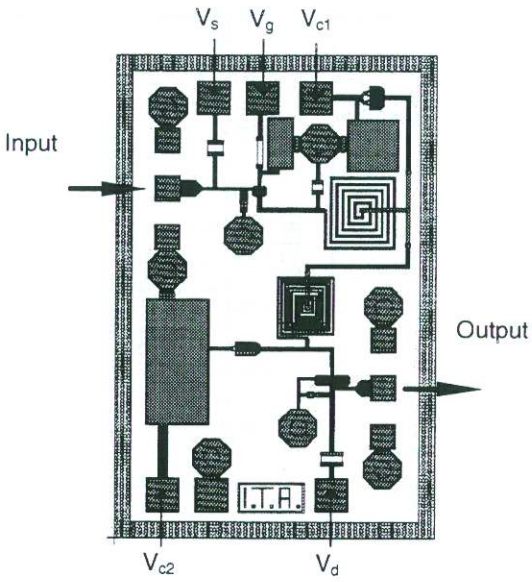
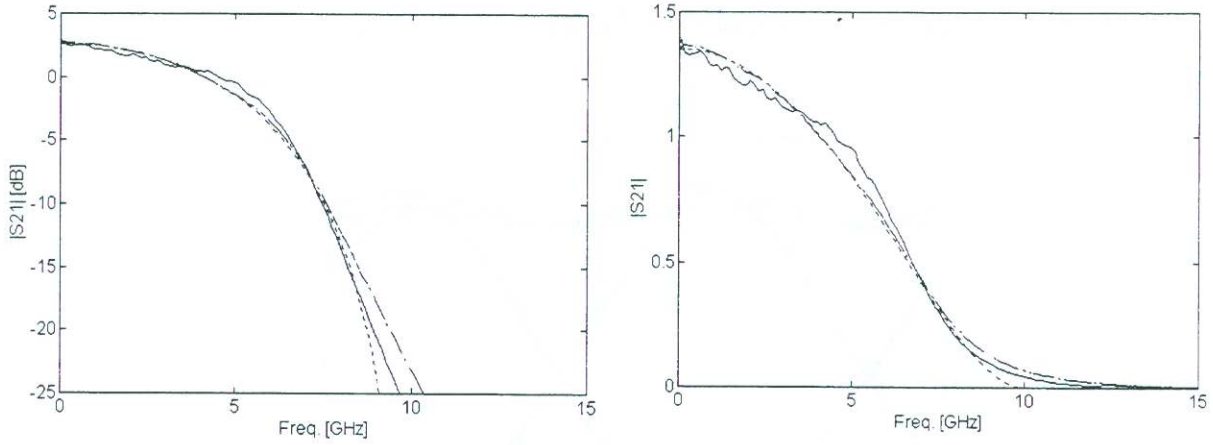


Figure 3. Layout of the signal shaping filter designed in GaAs MMIC technology.



(a) (b)

Figure 4. Comparison of measured (solid line), computed response (dashed line) and idealised responses (dotted line) on logarithm (a) and linear scales (b).

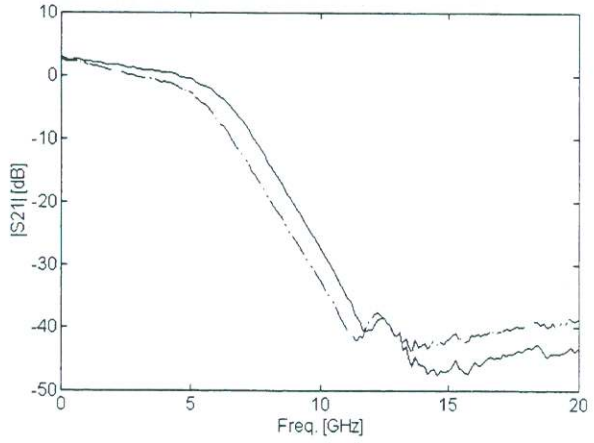


Figure 5. Filter frequency responses for two different sets of VARICAP voltages.

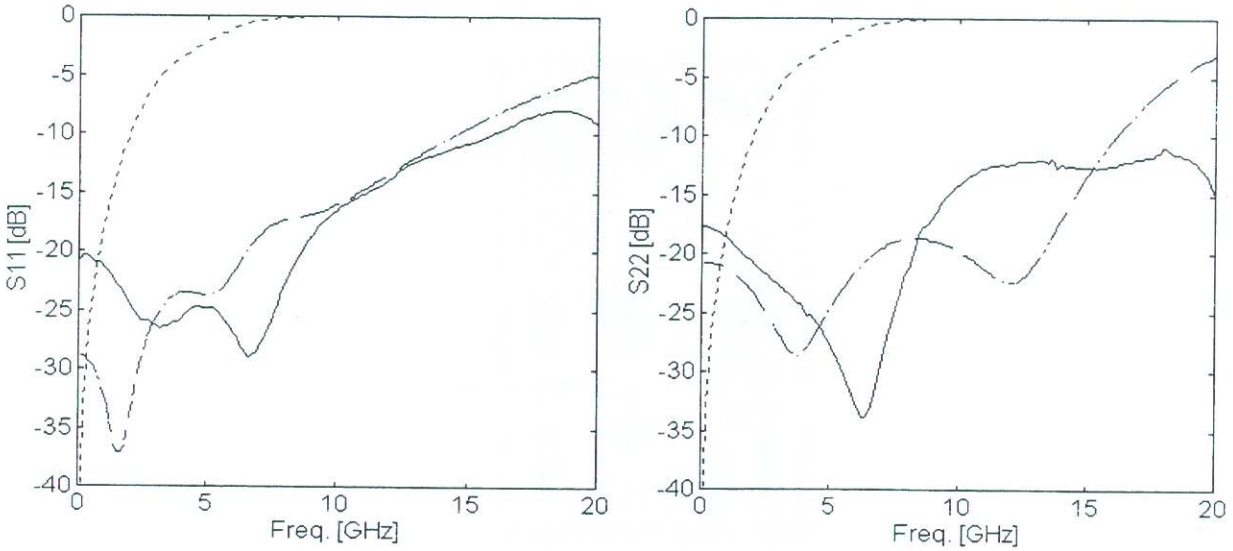


Figure 6. Measured (solid line) and simulated (dashed line) filter input (|S11|) and output (|S22|) impedance match (at 50Ω). The dotted line represents the impedance match of a conventional 50Ω double-terminated LC ladder filter.

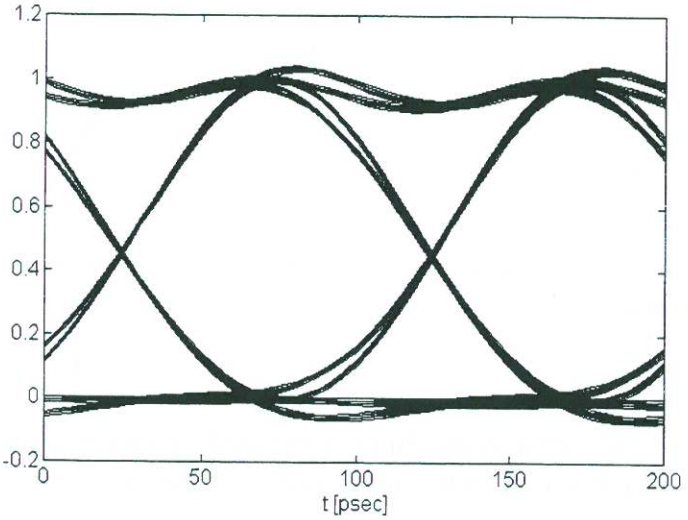


Figure 7. Computed eye diagram from the frequency data.