

# Ignoring the Obvious: Possibilities for On-chip Linearisation of RFIC Power Amplifiers

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*Possibilities for on-chip linearisation of RFIC PAs are reviewed. The issues are not just technical, but include some important paradigm shifts which the RFIC user community must traverse.*

## INTRODUCTION

The requirements of multi-carrier PA (MCPA) basestations in the worldwide mobile phone system has caused a major re-invention of PA linearisation techniques over the last decade. The multicarrier signal environment and the accompanying regulatory emission requirements impose a very stringent set of operating parameters; instantaneous bandwidth, signal peak to average ratio, and ACP/IM specifications can be an order of magnitude more stringent than in the much simpler case of a single channel mobile transmitter. For this reason, linearised PA products which have appeared on the market in recent years are complex subassemblies, containing a plethora of built-in test and monitoring functions.

This paper proposes that at chip level designers have been intimidated by the apparent complexity of PA linearisation schemes as a result of observing and reading the unquestionable difficulties and complexities of MCPA implementation. A key paradigm difference between MCPA and handset RFIC PA is that in the latter case, an improvement in linearity measured in terms of *just a few dB* reduction in ACP can have a *major impact on the production yield* of the product. This is in sharp contrast to an MCPA application, where a reduction in ACP of 20dB or more is typically required from a linearisation scheme. As a result, open-loop architectures have been the standard for handset PA products. It is arguably true to say that no other consumer electronic device has ever been sold in such large volumes, with a completely open-loop architecture, than the typical handset PA module.

Linearization methods are typically characterized into 3 main categories: feedback, predistortion, and feedforward. These techniques will be considered in the following sections, with the intended viewpoint of an RFIC handset PA designer. The generically distinct requirements of the handset application require the

traditional linearization methods to be subjected to a good deal of transmutation.

## FEEDBACK TECHNIQUES

Feedback is a more familiar technique for the RFIC designer than it is for a typical PA designer, being widely used at lower frequencies. At GHz frequencies, and especially when using higher power RF transistors which have high parasitic capacitances, the delay through a typical multistage PA is too high for effective use of negative feedback as a linearisation technique. This "ruling" applies even for so-called "indirect" feedback methods, which use a detected, or downconverted, signal envelope rather than the RF carrier itself. The handset application represents an interesting "gray area" for feedback possibilities. Whereas a typical matched high power (eg 50Watt LDMOS) device may in itself have a group delay measured in tens of nanoseconds, a 1Watt HBT may be between one and two orders of magnitude lower. It is thus somewhat surprising that feedback has been little used in 1G and 2G handset PAs [1]. Signal bandwidths measured in tens of kilohertz are essentially tolerant of feedback loop delays of a few hundred picoseconds. Unfortunately, this realisation may be too late; the 3G systems using WCDMA will require much higher signal bandwidths.

## PREDISTORTION

Predistortion techniques have recently been the most rapidly evolving sector in PA linearisation. This has been due mainly to the availability of DSP hardware which is fast enough to perform predistortion functions on the signal envelope in "real" time. In particular, the signal can be predistorted at the baseband level, in the digital world prior to DAC and upconversion. It is indeed an irony that in the near future PA linearisation may become obsolete due to the more widespread use of predistortion as part of the baseband signal generation process. Although appealing, this particular path has some

hazards, most notably the dramatically increased bandwidth of a predistorted signal; as much as a 10:1 increase in bandwidth can be incurred by predistorting a signal to a level such that a PA can be driven up to its 1dB compression point.

The more conventional analog predistorter, with a suitable DSP/DAC driver may still have some advantages. Such a configuration, shown schematically in Fig.1, may still represent a useful and adaptable RFIC product. The RFIC designer can easily implement on-chip digital attenuation and phaseshifting functions. The system DSP can address such a device directly, without need for expensive intermediate DACs (Fig.2).

Simulation of a typical handset PA shows that just 4-bit controls, with LSB of 0.1dB/1 deg, can have a major impact on the ACP of a PA swinging into its compression region. This is in complete contrast with a corresponding MCPA digital predistortion system, where as much as 14 bit precision has been quoted as being necessary to meet stringent multicarrier ACP and IM specifications.

It is important to note that in considering the above predistortion schemes, it has been assumed that the PA characteristic is sufficiently well characterised, and is sufficiently repeatable over a production run, that the predistortion algorithms in the DSP software can be fixed. This turns out to be a substantial issue in the MCPA case, where immense precision is required in setting the predistortion algorithms (often a look-up table is used). In the much less demanding environment of the handset, however, it may be a viable strategy to assume the same predistortion algorithm can be applied over a production run without any need for "fine-tuning" on a case-by-case basis. This is another example of where RFIC PA designers should not be intimidated by the complexity, both in theory and in practice, of a typical MCPA predistortion system.

## FEEDFORWARD

A typical MCPA feedforward system appears to be a complex subassembly which contains functions (couplers, isolators, combiners) which are difficult to realise on-chip. The basic concept of feedforward does, however, lend itself to some consideration for on-chip possibilities. The feedforward loop can in basic terms be considered a "post-distortion" device, where the necessary correcting signal is generated and added to the main signal. Such a correcting signal does not necessarily have to be generated in the conventional manner using a gain and phase cancellation loop, and the output summing can be implemented without having to use a high directivity coupler. Fig.3 shows one possible variation, in which the output transistor has its cells paralleled in a conventional manner at the output, but the input is split in a suitable ratio allowing different bias

and/or drive arrangements between the two segments. In this example, the smaller segment is biased well into Class C operation, whereas the main segment is biased for conventional Class AB operation. The Class C segment only starts to contribute to the output when the main segment starts to exhibit gain compression.

Such an arrangement is a pragmatic implementation of a more general technique known as "derivative superposition", whereby segmenting the output transistor and applying smaller bias differences to the different segments can result in substantial linearisation action [2]. Output transistor segmentation can be considered to be a distant relative of the conventional feedforward technique, which has realistic implementation possibilities for the RFIC designer. One is tempted to speculate on how much improvement could be obtained on just about any current RFIC PA product if the manufacturer took the simple step of allowing different bias levels for two or more segments of the output transistor. Once again, it has to be assumed that the user does not have to set the multiple bias voltages on a case-by-case basis; repeatability is, however, a long touted benefit offered by RFIC processes.

## ANALOG AND DIGITAL BIAS ADAPTION

The RFIC environment offers some other possibilities for PA linearisation, which do not fall under the above three conventional headings. One such method, bias adaption, is probably the most widely used in current RFIC products, and has been the focus of several patents. In particular, the application of a scaled replica of the detected signal envelope to the gate or base bias of the output transistor can modulate the gain appropriately so as to obtain useful linearisation action. Such a basic technique can be implemented at three levels of sophistication: (1) simple analog detection, scaling, and summation; (2) use of a DAC which receives a digital drive signal from the system signal processing DSP; (3) direct on-chip digital drive. The third option represents an opportunity for the RFIC designer to offer a solution which does not require a fast intermediate DAC, and can be driven directly from the system DSP, much in the same way as illustrated in Fig. 2 for gain and phase controls.

## AM RECONSTRUCTION

The possibilities for using a highly efficient PA whose output is then amplitude modulated to "construct" the final required signal have already been significantly exploited by the RFIC community [1,3,4]. The "EER" transmitter, frequently (but questionably) attributed to Khan [3] has apparently been developed to production-worthy chipset hardware. The outphasing RF transmitter has also been widely discussed in literature both old and

new [1,5], and offers another variation on the AM reconstruction theme. In the outphasing transmitter the need for a baseband power buffer is eliminated, but a suitable power combiner would probably need to be realised off-chip. There is another dimension to outphasing, which is the need to recover power from the “dump” port of the combiner in order to maintain acceptable system efficiency. Again, this has been demonstrated at chip level [6]. Manufacturers of these products however have so far been dismayed at their poor reception from the system manufacturing community. This appears mainly to be due to the system design paradigm shift such products traverse; the RFIC component manufacturer is apparently striking too far into the territory of the system designer, and at present the system manufacturer seems reluctant to relinquish the design and manufacturing flexibility which a stand-alone PA product offers. Here, it seems for sure, the heading “ignoring the obvious” applies. AM reconstruction is a well proven technique for a new generation of handset RFIC products but has yet to gain acceptance.

## CONCLUSIONS

Other than some very rudimentary analog predistortion tricks, the RFIC PA community still seems to be ignoring, or encouraged by system manufacturers to ignore, the possibilities for linearisation being widely exploited by MCPA designers. The situation can be summarized as follows:

- At signal bandwidths up to a few tens of kilohertz, feedback methods can be, and have not been, exploited
- The handset PA designer has a totally different perspective on the benefits of a few dB of linearisation action, in comparison to the MCPA designer who typically needs 20-30dB of linearisation
- A simple rudimentary linearisation scheme in a handset RFIC application can be considered entirely as a yield enhancing technique, without a requirement to allow for more stringent specifications
- RFIC designers are probably intimidated by the complexity of MCPAs which use predistortion or feedforward techniques. These techniques can be implemented in simpler forms when the linearisation goals, and the signal bandwidths, are much more modest
- AM reconstruction techniques represent a major paradigm shift for RFIC designers, being system level rather than component level concepts.

They undoubtedly represent a new and lucrative generation of RFIC products, but timing the “acceptance curve” is a tough call for marketers and corporate managers; some have already paid a heavy price for their overly optimistic projections

- A sting in the tail: if RFIC PAs can be made sufficiently uniform in their performance characteristics, baseband predistortion using a fixed non-linear template will eliminate the need for linearisation in the PA and designers will need to re-focus on efficiency and cost issues

## References

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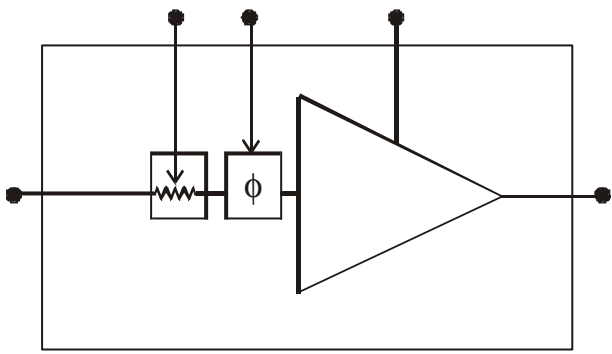


Fig.1 RFIC PA with on-chip predistortion controls

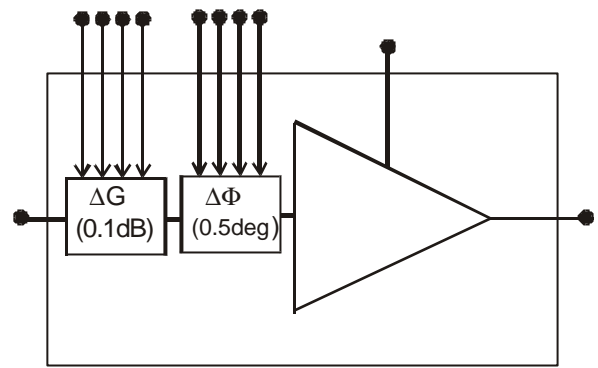


Fig. 2 RFIC PA with direct on-chip digital gain and phase control for predistortion applications

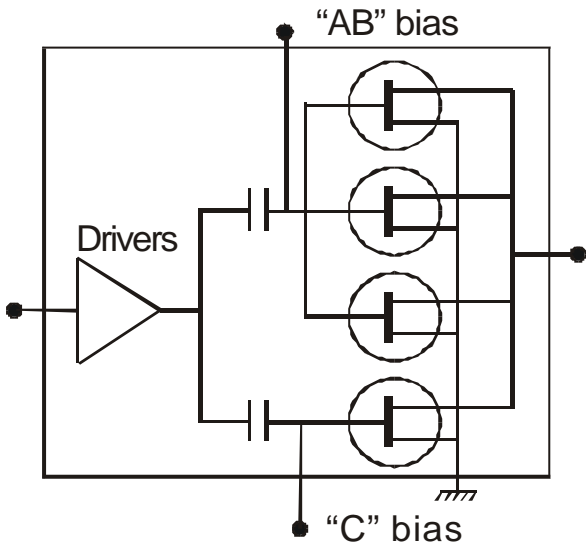


Fig.3 Quasi-feedforward RFIC PA using segmented bias on output transistor.