STATISTICAL TECHNIQUES FOR MMIC DESIGN SENSITIVITY AND CHIP YIELD ANALYSIS

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ABSTRACT

This paper describes the first application of Taguchi SDOE to the sensitivity analysis of a MMIC amplifier. The technique demonstrates clearly which of the simulated performance parameters, including the one dB compression point derived from non-linear simulation, are sensitive to which of the device matching elements. The adaptability of the Taguchi technique is also demonstrated by applying it to the tolerance analysis of the same MMIC. Correlation of some of the HEMT parameters is now taken into account by the analysis, and the results are compared to those obtained by a fully correlated database sampling technique.

INTRODUCTION

The increasing demand for MMICs in commercial applications is forcing MMIC designers to develop both right-first-time design strategies to reduce NRE costs, and process tolerant designs to minimise individual die cost during production. Right-first-time MMIC design relies on well characterised, and well modelled active and passive elements so that the designer can produce chips with measured performances very close to the simulated performance. As the operating frequency of MMICs is pushed higher and higher, the model uncertainties become more important because any errors in the models start to represent a significant proportion of the element impedance. In order to minimise the effect of these errors on the measured chip performance, the designer must carry out a sensitivity analysis on all the passive elements in the matching circuits to identify those elements most critical to the performance and ensure that these elements are laid out in such a way as to minimise modelling errors. Process tolerant design requires a good knowledge of the process variations, and the way this affects the active device performance, together with the design tools and techniques which allow quick assessment of the chip yield during the design phase.

This paper details the first application of Statistical Design Of Experiment (SDOE) techniques, described by Taguchi (1, 2), to the sensitivity analysis of a 26 to 30 GHz HEMT MMIC power amplifier, and shows clearly which elements the P_{1dB} compression point is most sensitive to, using the minimum number of time-consuming non-linear simulation trials. The paper goes on to apply the same technique to the tolerance analysis of the HEMT amplifier, and compares the results obtained to those for a different amplifier on the same process using an alternative database sampling technique.

TAGUCHI SDOE FOR MMIC SENSITIVITY ANALYSIS

Many fabrication areas have used Taguchi, Statistical Design Of Experiments for problem solving, process centring and tighter process control, such as Green and Launsby (3), but their application to MMIC design has so far been limited to the tolerance analysis detailed by Marsh and Wadsworth (4). The Taguchi principle is to perform a small number of balanced simulation experiments in which the matching element values are varied to high and low values (typically +-10% to mimic possible modelling errors), and the resulting simulated performance of the chip is noted. The combinations of the high and low value of each element for each simulation experiment are precisely defined by standard orthogonal arrays. The orthogonal nature of the array allows the performance measures, such as gain, match and P_{1dB} point, for the high and low values of each element to be extracted and averaged. The result is a list of the partial spreads of each performance measure due to each matching element. The overall performance spread is the root-sum-of squares of each partial spread so only the large values are significant. In this way the most sensitive matching elements, causing the largest spread in the performance, are clearly identified. Further details of the practical application of the technique was given in the tolerance analysis paper by Marsh and Wadsworth (4).

This technique was applied to the sensitivity analysis of a 26 to 30 GHz two stage HEMT power amplifier, a layout plot of which is shown in figure 1.The bias feed elements such as the spiral inductors, and the DC blocking capacitors were not varied because they only have a second order effect on the chip RF performance. The components that were varied were all the matching elements of both gain stages of the amplifier. To reduce the size of the orthogonal arrays required, it was decided to perform a sensitivity analysis on one gain stage at a time. Inductive microstrip matching elements were varied in length by +-10% to mimic possible errors in their model representation or reference plane errors where they meet at T and cross junctions. MIM capacitor matching elements were varied +-10% in both their side dimensions to mimic possible errors in their model representation or capacitance modification due to the proximity of other components such as grounded through GaAs vias. For this experiment, all the elements were varied by the same percentage of their physical dimensions to highlight the relative difference in sensitivity of the RF performance (if the modelling errors can be quantified, the sensitivity analysis can be further refined to vary the component elements by this known amount).

In this case, the performance measures for the first stage analysis were the input reflection and transmission scattering parameters (S11, S21) and the output power at one dB gain compression (P_{1dB}), and for the second stage analysis were the output reflection scattering parameters (S22), S21 and P_{1dB}. A spreadsheet programme was used to take the nominal and spread values of the element variables, and use the L8 orthogonal array to produce the values that must be used in the eight simulation runs. The elements values were manually edited in the default variable block of a standard RF simulator before each simulation run and the performance measures noted. The performance measures from each simulation run were then entered back into the spreadsheet which used the Taguchi analysis to derive the partial spreads. The resulting partial spread tables for the stage one and stage two analysis are shown in figures 2 and 3, respectively.

There is a lot of interesting data in these tables and the full interpretation of this can be quite involved, but there are several observations that can be seen clearly:

Considering first the stage one analysis in figure 2, it can be seen that the largest performance spread by far is in the low frequency gain, and this spread is most sensitive to the input shunt capacitor Cip2. Investigation can now focus on this capacitor, and the layout of the chip can be changed to ensure that possible modelling errors associated with this matching element are minimised. This includes taking care that it is connected in the same way as the characterisation capacitors were connected during model development, and spacing out nearby components so that they do not have a large affect on the fringing capacitance.

Secondly, the stage one analysis shows that the P_{1dB} point is very insensitive to all the matching elements, which suggests that only the second stage is limiting the power performance, and that this first stage is operating correctly, well within its linear region.

Initial observation of the second stage analysis shows that the greatest spread is in the high band P_{1dB}, and that this is caused by the output series inductor element LosB and the output shunt capacitor Cop. The fact that these elements are determining the output stage power load line, and hence the chips' compression characteristics shows that this sensitivity analysis agrees with common understanding of power amplifier design.

It can also be seen that the gain at the low band edge is again affected by the input matching shunt capacitance element Cip, and that the high band gain is most sensitive to the output shunt capacitor Cop. As for the first stage, the layout of only these most sensitive components in the second stage can now be adjusted to minimise the difference between their modelled and actual RF response.

The performance measures used in this analysis included the output power at one dB gain compression (P_{1dB}), which was derived from a power compression sweep of the MMIC using non-linear models of the HEMTs and harmonic balance simulation. Each non-linear simulation took about one minute to run. The time taken for the rest of the analysis, once the spreadsheet has been set-up, was as follows: ten minutes to input the nominal and spread values and read off the simulation trial values; half an hour to edit the simulation variables and perform the eight non-linear simulations; and another ten minutes to input the performance measure results back into the spreadsheet and print out the partial spreads. Alternative sensitivity analysis using Monte-Carlo techniques would require over one thousand non-linear simulations for high confidence levels, taking over 16 hours to complete, compared to less than one hour for the Taguchi technique.

TOLERANCE ANALYSIS

Now the circuit has been desensitised to model errors, the circuit must be designed to be high yielding against the known process variations. The Taguchi tolerance analysis detailed by Marsh and Wadsworth (4) showed that knowing the process variations, and the effect these had on the overall performance spread and mean value, one can also calculate the MMIC yield against a specification limit. This Taguchi tolerance analysis technique was applied to the HEMT power amplifier, but for the first time now included correlation between C_{ds} and R_{ds}, and correlation between g_m and C_{gs}.

The importance of the additional HEMT parameter correlation to this technique is explored by examining the results of those obtained by a fully correlated database sampling technique. Using this technique, a database of transistor equivalent circuit model element parameters has been utilised in the evaluation of the performance of a broad band 10 to 36GHz gain block designed and fabricated using the same HEMT process. The database was derived from measurements on transistors of size 2x60µm. However, because the equivalent circuit model is scaleable over a range of device sizes and bias conditions (i.e. percentage Idss) the database may also be used in the evaluation of a broad range of circuits. The database contains over 200 sets from several batches of wafers gathered as part of routine process control monitoring. An important feature of this work is that in the database the correlation between the transistor parameter elements is fully maintained. A Monte Carlo analysis of the gain of the two stage circuit is shown in Figure 4. Transistor data sets were sampled from the database in a random manner to build up the response. The distribution in gain at a frequency of 26GHz is shown in Figure 5. The predicted mean value is 11dB with a standard deviation of 0.6dB.

The corresponding measured results for the circuit are shown in Figures 6 and 7. The average gain at 26GHz is 10.96dB with a standard deviation of 0.5dB. The predictions are therefore in good agreement with the measured results. Thus this database sampling technique may be used effectively to predict MMIC yields for the circuit prior to committing to wafer manufacture. The only drawback with this method is that it takes about 8000 simulations, over about an hour, to perform the analysis with 95% statistical confidence and only +-1% error.

The Taguchi tolerance analysis of the 26 to 30 GHz two stage HEMT power amplifier, including the additional correlation, used the gain and input match at the band edges as the performance measures to compare to the specification limits which were: S21>12 dB, S11<-10 dB @ 26.5 and 29.5 GHz. The time taken to edit the variables and perform the eight simulation trials was about 20 minutes. The results of the eight simulation trials gave pass rates of 99.9% for S11 @ 26.5 GHz; 99.1% for S21 @ 26.5 GHz; 100% for S11 @ 29.5 GHz; 85.2% for S21 @ 29.5 GHz, giving an overall predicted pass rate of 84%. When the HEMT MMICs have been fully measured, the actual circuit yield can be compared to this predicted figure.

CONCLUSION

The first application of Taguchi SDOE to the sensitivity analysis of a MMIC amplifier has been described. The technique demonstrates clearly which of the simulated performance parameters, such as output power and gain, are most sensitive to which device matching elements, so that these elements may be laid out in the most accurate way. The adaptability of the Taguchi technique has also been demonstrated by applying it to the tolerance analysis of the same MMIC. The technique, as applied to tolerance analysis, was developed further from previous applications to include correlation of some of the HEMT parameters, and the results of this analysis are compared to those obtained by a fully correlated database sampling technique.

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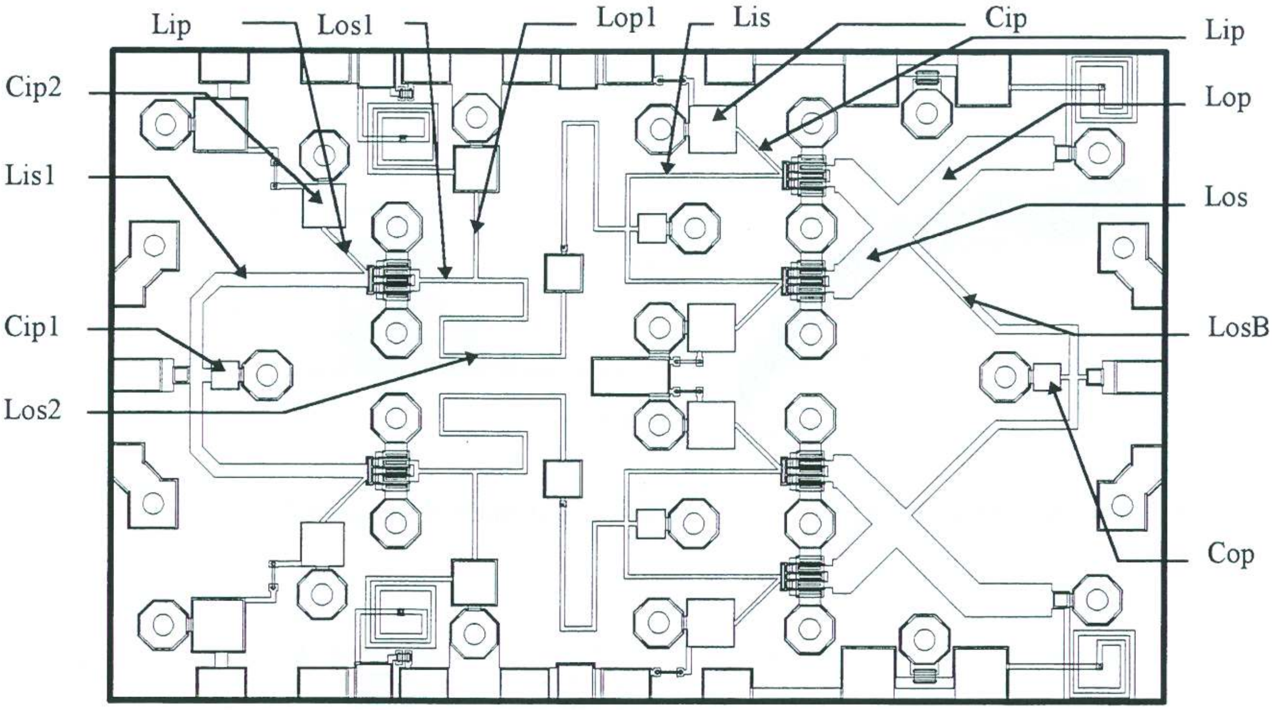

Figure 1: Layout of the 26-30 GHz HEMT power amplifier showing matching element.

Measurement	S21(26GHz)	S11(26GHz)	P1dB(26GHz)	S21(30GHz)	S11(30GHz)	P1dB(30GHz)
Element	partial σ	partial σ	partial σ	partial σ	partial σ	partial σ
Cip1	0.13	-0.02	0.01	-0.31	0.04	0.00
Lis1	0.14	0.00	0.01	-0.31	0.07	0.02
Lip1	1.43	-0.04	0.03	0.28	-0.07	0.00
Cip2	2.92	-0.07	0.04	-0.05	0.04	0.00
Los1	0.23	-0.04	-0.02	-0.08	0.02	-0.01
Lop1	0.17	-0.01	0.03	-0.04	0.01	0.02
Los2	1.20	-0.11	0.03	0.03	0.00	-0.03
total σ	3.48	0.14	0.07	0.53	0.12	0.04

Figure 2: Partial spreads of the measured parameters vs the stage one matching elements

Measurement	S21(26GHz)	S11(26GHz)	P1dB(26GHz)	S21(30GHz)	S11(30GHz)	P1dB(30GHz)
Element	partial σ	partial σ	partial σ	partial σ	partial σ	partial σ
Lis	0.12	0.03	0.14	0.00	0.02	0.15
Lip	0.14	-0.02	-0.04	-0.01	0.01	0.04
Cip	0.49	-0.03	-0.03	0.01	0.00	0.08
Los	-0.04	0.01	0.00	0.04	-0.02	-0.06
Lop	-0.21	0.02	0.05	-0.03	0.00	0.09
LosB	0.26	-0.03	0.20	0.34	-0.11	-0.60
Cop	0.12	-0.02	0.29	0.42	-0.13	-0.73
total σ	0.64	0.07	0.38	0.54	0.17	0.97

Figure 3: Partial spreads of the measured parameters vs the stage two matching elements

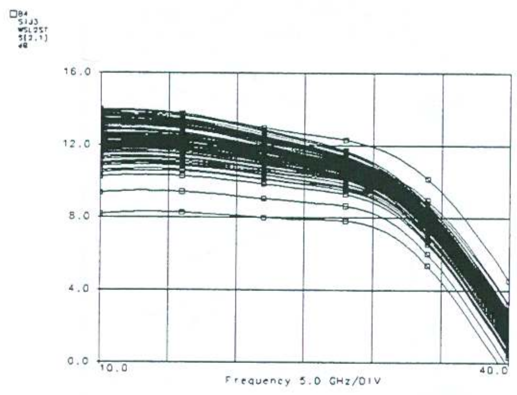

Figure 4 :Monte-Carlo simulation of gain

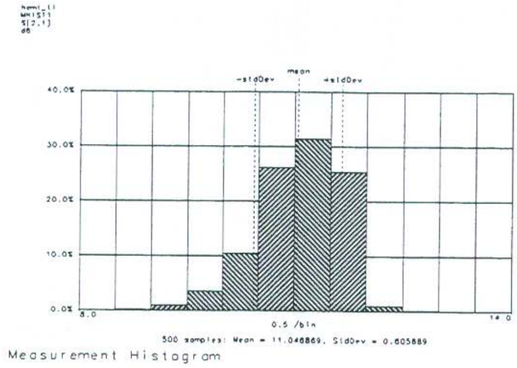

Figure 5: Distribution of gain at 26 GHz

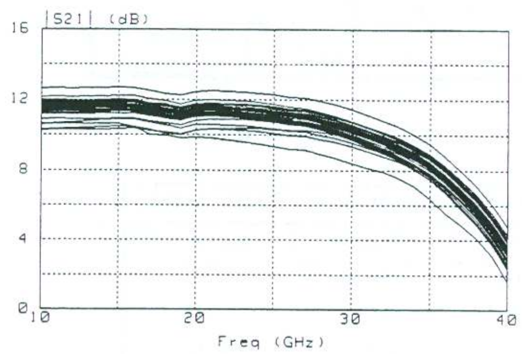

Figure 6: Measured gain

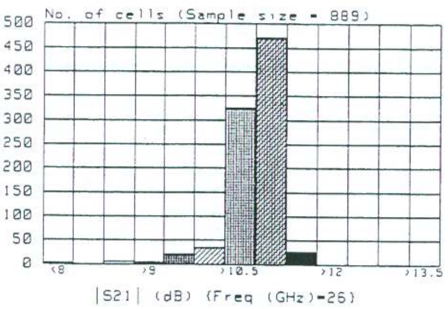

Figure 7: Measured gain distribution at 26 GHz