High Performance Device Technologies for Future Communications Satellites

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ABSTRACT – Future communications satellites will require an order of magnitude improvement in the cost/performance of microwave/analog/digital device technologies in order to meet the needs of universal telephony access, computer networking, tele-imaging, telecommuting, videoconferencing, and high-speed Internet. Microwave and millimeter wave technologies for ultra-low noise amplifiers, high efficiency power amplifiers and high-speed analog/digital circuits capable of operating at multi-gigabits per second are being developed to meet this demand. An overview of the status and issues related to these development efforts is presented.

I. INTRODUCTION

As wireless systems move into the next century, the importance of the satellite as part of the network (Fig. 1) increases with each new demand on the system. There is intense competition in the satellite industry to set the new standard for the global information infrastructure, with systems such as AMSC, Iridium, ICO, Globalstar, Teledesic, Astrolink, Spaceway and many others vying for their share of the market. In order to meet the needs of ever increasing commercial and personal data throughputs, today's satellite carrier link frequencies are moving from C-band into the higher Ku- and Ka-bands for up/down links and V-band or optical for cross-links. In the next ten years, the carrier link frequencies will move even higher to accommodate the ever increasing demand for more bandwidth. These wider channel bandwidths will allow satellites to relay the vast amount of information demanded by two-way voice, video telephony, medical imagery, Internet data transmission and other simultaneous communications. The ability to quickly adapt to changing customer needs requires a very flexible on-board switching network, which allows resources to be re-allocated to high demand users at a moment's notice. As a result, future satellites will require sensitive millimeterwave low noise receivers, high power high efficiency linear power transmitters, and on-board switching network capable of moving data at rates of multi-gigabits per second.

II. SATELLITE COMMUNICATIONS SYSTEM

A simplified, generic block diagram of the payload of the next generation of satellite communications systems is shown in Fig. 2. In only the last 5 years due to the demand for bandwidth, the up and down links have moved from C-band through Ku-band and now to K/Ka-band. In the future as the bandwidth demand continues to escalate, the carrier frequencies will migrate to even higher bands. In this paper, we discuss the tradeoffs of different technologies on the three most important subsystems of this block diagram: (a) low noise devices for the front-end electronics, (b) high power output amplifiers for the transmitters, and (c) high speed analog/digital circuits for beamforming, signal processing and routing.

A. LOW NOISE RECEIVERS

Since the mid-80's, significant progress has been made in developing ultra-low noise device technologies. Initially, the GaAs MESFET technology was optimized resulting in an MBE grown, sub-quarter micron gate-length device with an f_t of 100 GHz. The millimeter wave, low-noise performance was further enhanced by the development of the pseudomorphic GaAs pHEMT. In the early 90's, the InP-based HEMT technology demonstrated the highest cutoff frequency of any three terminal device [1], resulting in still further reduction in noise figure. Low noise MMIC amplifiers utilizing either GaAs- or InP-based HEMTs have demonstrated outstanding performance over the entire microwave/millimeter wave frequency range as shown by the results plotted in Fig. 3, showing the noise figure vs. frequency for GaAs- and InP-based MMIC LNAs. Efforts in these technologies are being focused on (1) increasing complexity while reducing cost, (2) reducing power consumption, (3) combining device types i.e., HEMTs and HBTs to increase functionality and performance, and (4) developing device technologies for sub-millimeter wave applications.

In order to increase functionality, technology with both HEMTs and HBTs integrated monolithically in the same IC is being developed. Initial results for an InP-based pin/HEMT/HBT monolithic integrated optoelectronic receiver are shown in Figure 4. The receiver operated up to 7 Gb/s with 4 GHz of bandwidth. At 2.5 Gb/s and a sensitivity of –24.7 dbm, it achieves a Bit Error Rate (BIT) of 10^{-9} [2].

In the future, more bandwidth will be required to handle the rapid increase in information transfer. To achieve the bandwidth, carrier frequencies will be pushed to sub-millimeter wave frequencies. Optimization of the InP-based HEMT for sub millimeter wave operations resulted in a D-band MMIC amplifier shown in Figure 6. This MMIC exhibits 30 dB of gain at 140 GHz [3].

B. HIGH POWER TRANSMITTERS

The biggest challenge for power devices for satellite communications is achieving the desired high power added efficiencies (PAE) with linearity. At microwave frequencies, L through X band, the GaAs MESFET and pHEMT are the solid state device technologies challenging the TWTA. At these frequencies, the TWTA with linearizers has Po > 100 W with 50%-65% PAE. It is very difficult for SSPAs to achieve these performance levels; however other factors such as cost, weight, reliability, and beam forming/steering support the SSPA approach. The state of the art for Po and PAE of discrete power devices and hybrid amplifiers is rapidly advancing at K-band as shown in Fig. 6. The PAE of MMICs (not shown) is approximately 10 to 15% points lower than the PAE of discrete devices or hybrid amplifiers.

To further increase the output power of SSPAs, new materials such as SiC and GaN are being developed. The SiC MESFET has demonstrated outstanding performance, Po, from UHF to X-band. Because of its lower mobility and cutoff frequencies, however, the SiC MESFET will be limited to frequencies of X-band and below. The newer but less mature GaN MODFET has demonstrated K-band performance with small signal RF parameters similar to the GaAs pHEMT as shown in Fig. 7. Though this technology appears to be extremely promising with the combination of high breakdown voltage (100 V) with high f_t and f_{MAX} a great deal of fundamental work with respect to thermal dissipation and reliability needs to be performed before this technology can be considered for satellite applications.

For carrier link frequencies above K-band, an InP-based device is required to achieve the necessary power performance. The standard InP-based HEMT has demonstrated excellent PAE at V-band but had high gate leakage due to its low Schottky barrier. A variation of the InP-based HEMT is being developed utilizing improved Schottky-barrier layer, which has the potential of producing watts/device at W-band with excellent PAE [4].

C. HIGH PERFORMANCE ANALOG/DIGITAL ICS

The signal processing being proposed for future communications satellites is a much bigger challenge than the low noise or power requirements discussed above. In order to improve system performance and reduce weight and size, all of the beamforming, routing and signal processing should be performed in digital, not analog. System designers want to digitize the incoming signal as soon as possible behind the low noise receivers. Every down conversion adds filters, weight, power dissipation and system complexity. Digitizing, routing and re-transmitting the signal for each spot beam will require significant advances in CMOS, SiGe bipolar and III-V IC technologies, as well as signal processing architectures and power conditioning to meet the cost, weight, and power consumption objectives.

High speed A/D converters (ADCs) are a key to achieve the above requirements. Many different approaches are being attempted to enhance the ADC performance such as delta-sigma architecture, resonant tunneling diodes, optical sampling, and super conducting devices. Today's state-of-the-art ADC results are summarized in Fig. 8 [5].

The delta-sigma architecture is a very promising approach for direct digitizing an RF signal, but requires a very fast device technology that can over sample the signal at a much higher frequency than the carrier. Thus in order to develop a 10GHz A/D, the signal must be sampled at several octaves above. Techniques have been developed to reduce the stringent requirements on the technology by increasing the complexity of the front-end of the A/D and by using a bandpass A/D. Delta-sigma A/Ds with >10-15 bits resolution over a small to modest bandwidth at 10 GHz are being developed.

By incorporating InP resonant tunneling diodes with InP-based heterojunction bipolar transistors (HBTs), it might be possible to significantly increase the speed and lower the power of the A/Ds. Presently a DARPA program is attempting to demonstrate a 4-bit, 20 GS/s A/D converter in InP-based RTD/HBT technology [6].

The most serious constraint limiting higher performance A/D converters is the jitter in the clock signal being distributed to the IC. Optical techniques with extremely fast optical pulses are being investigated to reduce jitter. A program is being performed to demonstrate a 4-bit, 100 GS/s A/D converter by this technique [7].

Today, one of the biggest contributors to weight and size is the bandpass filters required in the down conversion between the low noise receivers and the A/D converters. Recent advances in micro-machining have opened up a new approach to high Q, small filters to be used as part of the down conversion circuitry. By utilizing IC processing techniques, filters that are less than one wavelength in dimension are possible. In the future, these filters will be monolithically integrated into the low noise MMICs. In order to achieve the overall system requirements of future systems, a monolithic low noise receiver, bandpass filters with mixers, and the A/D converter with DEMUXs will be on a single chip.

Other high performance ICs required include high performance MUX/DEMUXs to form parallel and serial data streams into and out of the FFTs and DACs for transmission of an analog signal back to earth. The challenge for this IC technology is high speed with low power dissipation at LSI complexities. The leading technology for this application is SiGe HBTs which have demonstrated both the speed and complexities required. SiGe digitals ICs have demonstrated operation at 23 GHz [8] and will extend into the low millimeter wave frequency range. As the carrier link frequencies move up to the millimeter wave range, the high speed InP-based HBT ICs will increase in complexity in order to interface to SiGe ICs which are interfacing to Si CMOS FFTs.

The heart of the digital signal processing are the FFTs which are very large complexity (100-500K gates) ICs. Because of the complexity of the FFTs, an extremely low power, high speed IC technology is required. The only reasonable choice for this technology is Si CMOS. Currently though, the projected power levels are too high to accommodate the complexity required for this function. Fig. 9 [9] shows the speed power product for high performance IC technologies along with the projected required speed power product.

In order to achieve the projected 100X reduction in speed power product required for future communications satellites, the scaling of power supply voltages, system level power management, and architecture design issues must be addressed. Powering down vs. lower speed processing during low capacity times and pipelining vs. paralleling architectures and algorithms to reduce computational complexity are all issues being addressed [10].

III. CONCLUSION

Today, a family of satellites, which can handle the rapidly increasing demand for voice, video and data transmission around the globe, is being developed. For these satellites, the performance requirements coupled with the cost targets for microwave and millimeter wave low noise receivers, high power high efficiency linear transmitters, and ultra low power high bandwidth switching, routing and signal processing ICs are extremely aggressive. In the next 10 years, the demand for more bandwidth will push the carrier link frequencies even higher and the performance and cost requirements will require an order of magnitude improvement.

IV. ACKNOWLEDGMENT

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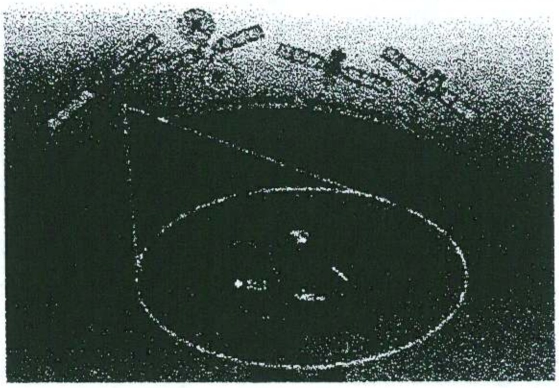
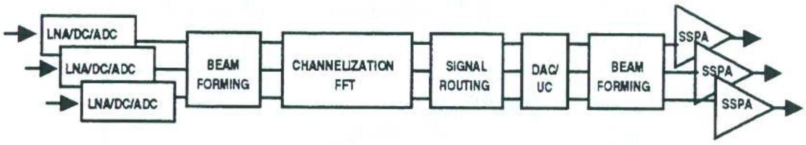


Fig. 1. Wireless communication network.



LNA/DOWN-CONVERTER	MODULATOR	DIGITAL PROCESSOR (FFT)	SWITCH	SSPA
FREQ:Ku-TO Ka-BAND NF: < 5 - 6 dB BW: > 500 MHz GAIN: > 30 dB	FREQ:Ku-TO Ka-BAND PHASE RES: < 2 DEG AMP RES: < 0.1 dB	CLOCK: > 2 GHz BW: > 500 MHz POWER:< 0.1 uW/GATE-MHz COMPLEXITY > 150K Gates	BW: > 1 Gb/s I/O: > 32 x 32 LOSS: < 0.2 dB	FREQ:Ku-TO Ka-BAND BW: > 500 MHz FLATNESS: < 0.1 dB POWER: > 2 W EFFICENCY: > 50-65%
A/D CONVERTER				
CONV FREQ: > 1 Ge/s RES: > 6 BITS				

Fig. 2. Satellite communication system.

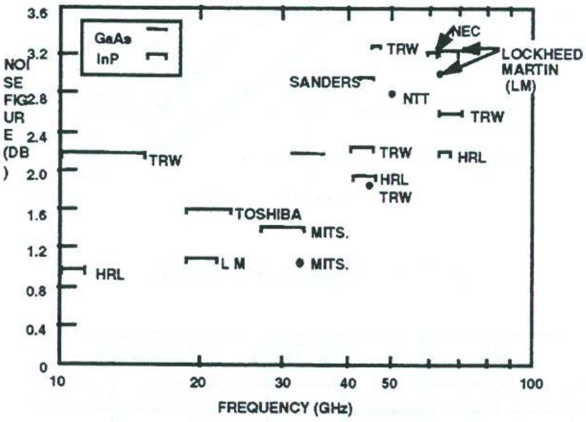


Fig. 3. Low noise MMIC performance.

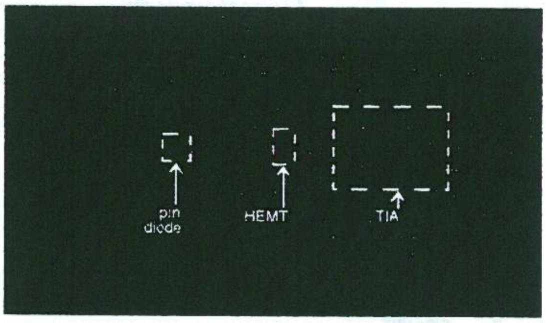


Fig. 4. High sensitivity P-I-N HEMT/HBT integrated optoelectronic receiver.

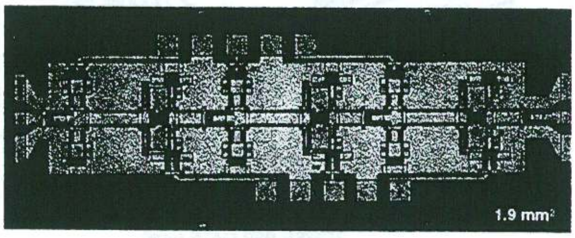


Fig. 5. D-band high gain MMIC amplifer.

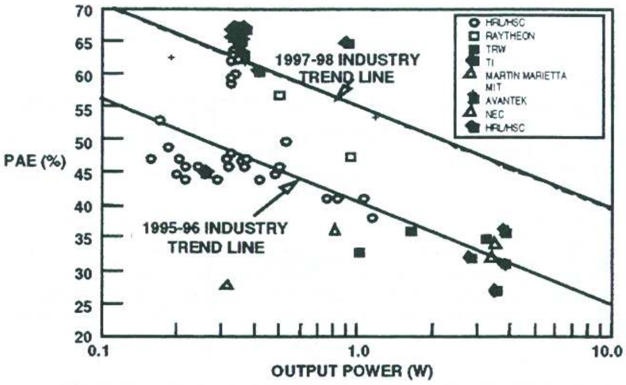


Fig. 6. K-band discrete power device performance current industry trends.

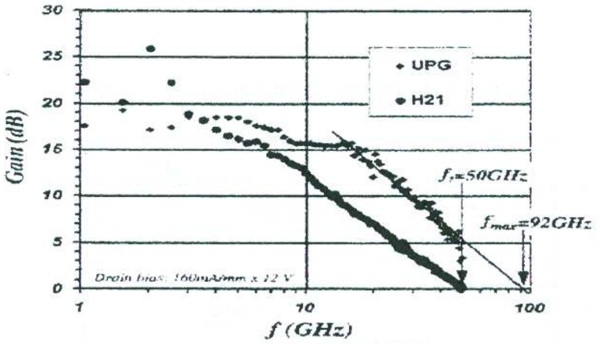


Fig. 7. GaN power MODFET.

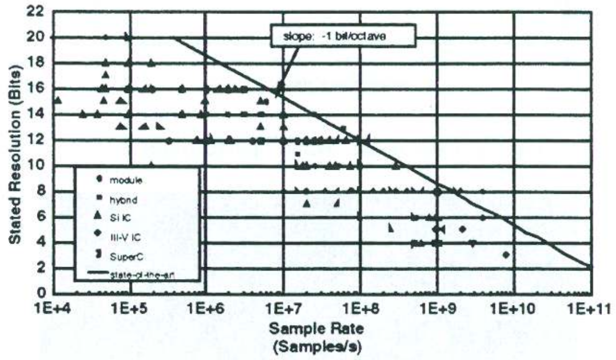


Fig. 8. Analog-to-digital converter data: stated resolution.

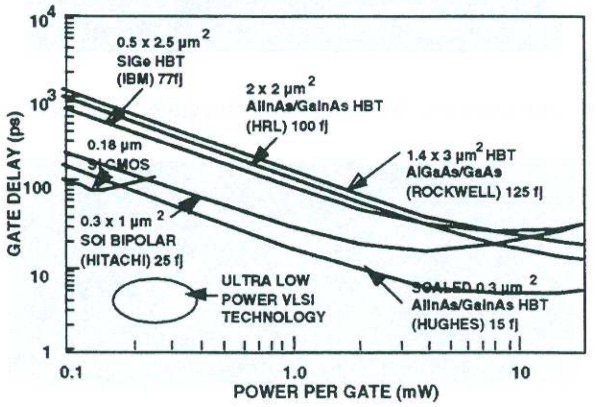


Fig. 9. Low power IC technology.