Practical Application of GaAs MMIC Technology to Next-Generation 20 / 30 GHz Data Communication Systems

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ABSTRACT

Each year GaAs MMIC technology finds greater application in high volume, low-cost telecommunications systems. Cellular and PCS front-end chip-sets currently form the bulk of commercial GaAs MMIC products, but next generation systems now in design will require two-way data communications at 20 and 30 GHz. Infrastructure will be developed for both terrestrial (ground terminal) as well as space-based (satellite) interfaces for these new systems.

This paper presents an overview of some of the GaAs MMIC chip-sets currently being designed to meet the requirements of these new 20 / 30 GHz systems, and examples are presented outlining some of the MMIC performance that has been achieved to date in prototype efforts. This paper also describes how GaAs MMIC technology might be packaged for integration with transmit and receive sub-systems. In some cases options are presented, and how these options might affect the resulting front-end designs are discussed.

Finally, the challenges facing the technology implementation are outlined, and where possible, efforts aimed at overcoming the limitations of the technology are presented as practical solutions which could be available as production methods by the time these new systems are ready for high-volume production.

EXPANDING THE CONCEPT:

I. TRANSCEIVER COMPONENTS

Whether a transmit or receive function resides in a satellite system or a ground-based terminal, the critical MMIC components at 20 and 30 GHz include the receiver Low-Noise Amplifier, the transmitter Driver and Power Amplifiers, and frequency up-and-down converters. Figure 1 shows the block-diagram of an example dual-polarization (dual-channel) 29 GHz ground-terminal transmit function. A similar topology would follow for the dual-channel 19 GHz receiver.

Both satellite and base-station applications will employ opposing frequency plans for full-duplex operation with ground-terminals and / or multi-point terminals, thus MMIC transmitter and receiver components will be required at both frequencies. The following sections present examples of MMIC chip-set development efforts that are aimed at both ends of the link.

II. LOW-NOISE AMPLIFIERS

Figure 2 shows measured data for a prototype MMIC Low-Noise Amplifier for a 29 GHz base-station or satellite receiver application. This chip was built using 0.25μm pHEMT technology, and the measured performance demonstrates that existing MMIC-based pHEMT technology is capable of meeting the system requirements at 29 GHz.

A similar LNA will be required at 20 GHz for ground-station receivers. Figure 3 shows a photograph of a 20 GHz MMIC LNA which provides > 25 dB of gain at 20 GHz, also constructed using 0.25μm pHEMT technology.

Preliminary measurements indicate that the MMIC LNA of Figure 3 yields a Noise Figure of approximately 2.5 dB. Efforts are also under way to design MMIC Low-Noise Amplifiers using Raytheon's 0.15µm (gate-length) process, which is expected to be a fully qualified production process by the end of 1998. Preliminary measurements show that the 0.15µm gate-length yields < 2.0 dB Noise Figure at 29 GHz.

In addition, tests are currently in progress in evaluating a new metamorphic HEMT process at Raytheon. Early tests show that this "InP-on-GaAs" manufacturing-compatible structure is yielding F_{min} of approximately 1.1 dB at 29 GHz with an associated gain of 9.5 dB as shown in Figure 4. This technology should allow for the design of a ≈ 1.7 dB MMIC LNA at 29 GHz. Except for the starting material, this new process will be identical to the existing 0.15µm pHEMT process, thus m-HEMT technology should provide a viable vehicle in providing good manufacturing margin for sub 2 dB Noise Figure amplifiers.

II. POWER AMPLIFIERS

Figure 5 shows a photograph of a first-generation 29 GHz MMIC power amplifier that might be used in a ground-terminal or multi-point transmit application. Measurements on the device shown in Figure 5 show that the three-stage amplifier yields 20 dB of small-signal gain and delivers 900mW of saturated power at 29 GHz. Recent design improvements in a similar design have yielded over 1.5 Watts at 44 GHz, and design efforts are currently under way to duplicate that performance at both 19 and 29 GHz.

As a proof of concept, Figure 6 shows the measured performance of an 18-22 GHz two-stage MMIC amplifier which delivers > 1.2 Watts of saturated output power with an associated gain of approximately 15 dB and a maximum power-added efficiency (PAE) of 35%. Also, Figure 7 shows a 37-40 GHz three-stage MMIC amplifier with a topology similar to that shown in Figure 5 which delivers over one Watt of saturated RF power across the band with an associated gain of approximately 15 dB. These results demonstrate that achieving > 1 Watt of RF power at 29 GHz as well is will be a matter of scaling existing designs.

III. FREQUENCY CONVERTERS

The success of MMIC-based Ku-Band down converters for direct broadcast satellite (DBS) television receiver systems demonstrates that GaAs MMIC technology can be successfully integrated with high volume, low-cost products. Design efforts are currently under way to prove that many of the same techniques that have been so successful for DBS applications can be employed at 20 and 30 GHz simply by employing pHEMT devices in proven design topologies.

Figure 8 shows the block diagram of a 30 GHz image-reject (I/Q) mixer that was fabricated as a single MMIC chip. Figure 9 shows a photograph of the completed MMIC design. [*Note: This was a first-prototype design, thus the chip layout is large and contains several "contingency" components which would be removed in a final design.*] The chip shown in Figure 9 was fabricated using Raytheon's 0.15µm pHEMT process, but this circuit would work nearly as well using a more standard 0.25µm pHEMT process, especially at 20 GHz. The chip shown in Figure 9 demonstrates a measured conversion gain of 7 dB for an RF input signal of -30 dBm at 29 GHz and IF output frequency at 1.1 GHz.

The components within the I/Q mixer of Figures 8 and 9 might also be used independently in simpler topologies. For example, one of the cascode mixer cells could be used either as an up-converter in a transmitter chain or as a low-cost receiver down-converter. In addition, the LO buffer amplifier might be used as a stand-alone MMIC gain-block in a receiver, or as a transmitter pre-driver. The intent with this initial design was to develop the more sophisticated I/Q mixer function so that subsets of this design could be easily applied to new designs.

There are distinct advantages in realizing the mixer up-and-down conversion elements with discrete diodes rather than with MMIC-based FET components. On the other hand, the advantages of reduced LO drive and the inherent balance between mixer ports that is routinely achieved in monolithic circuits make MMIC solutions very attractive in low-cost, high-volume approaches.

The advantages demonstrated by DBS down-converter chips in commercial LMB modules (as compared to competing discrete solutions) will be magnified in 20 and 30 GHz systems primarily because; (1) the higher frequencies will make discrete assembly more difficult, (2) transceiver systems are more complex (than receive-only systems) and parts count will be significantly higher with discrete approaches, and (3) the transmit power requirement in particular will force MMIC solutions in any practical approach.

Some 20 / 30 GHz systems may allow for the use of simple single-balanced receiver components, others may require the I/Q approach of Figure 8 in an image-reject topology. In either case, the building blocks for MMIC up-and-down converters are here today, and development efforts continue.

IV. PACKAGING

While MMIC chip-sets are being developed to support the needs of transmit and receive functions for the new 20 / 30 GHz systems, practical low-cost packaging methods must be developed as well, particularly for the high-volume ground-terminal business. The plastic leaded packages used in Ka-Band DBS and LNB applications will not function at 20 and 30 GHz, but efforts continue to develop a practical package that can be used in an equivalent manner.

One of the more promising areas is Low-Temperature Co-fired Ceramic package with a Metal Base, or LTCC-M technology. Figue10 shows a photograph of an LTCC-M package which exhibits 0.3 dB insertion loss per transition at 40 GHz, 16 dB return loss at the worst point and no resonances across the band. The LTCC-M package can be adjusted in size to accommodate any chip size, or a number of chips could be placed in a larger package as a subsystem, isolation requirements permitting. Once the tooling is manufactured for a particular LTCC-M package, recurring manufacturing costs can be quite low. The goal of the development effort for the package shown in Figure 10 was to deliver a flexible product (in terms of sizing) that would sell for less than $5 (U.S.) in high volume.

In the case of a front-end LNA (receiver) interface or a high-power transmit interface, the 0.2 to 0.3 dB transition loss of the LTCC-M package is still too much, and a lower-loss package interface is required. Figure 11 shows an approach that can be employed in low-cost front-end modules that uses a waveguide interface which typically offers < 0.1 dB transition loss when properly adjusted. The module shown in Figure 11 is actually more of a "chip test module", but the technique is valid for any MMIC based subsystem. The package (or "modulette") shown in Figure 11 can be configured with any combination of coaxial or waveguide interfaces on either end as desired. The module wall contains hermetic feedthrough pins which can interface to either medium. A waveguide launch is created by inserting a sleeve over the feedthrough pin and placing a waveguide "bridge" and backshort over the pin. It is a simple matter to convert the module interface to two coaxial connectors, two waveguide launches, simple feedthrough pins, or any mixture thereof.

CONCLUSIONS

Satellite, base-station and ground-terminal system manufacturers are presently defining the next generation high-capacity data systems of the future. A key ingredient in all of these systems will be the MMIC-based transmit and receive front-end components. These systems will be novel, in that they will by necessity bring together requirements for high performance, practical high-volume manufacturing techniques, and low-cost.

This paper has shown that the GaAs pHEMT MMIC technology in use today is capable of providing the required performance, and that design efforts are already under way to provide chip-sets. Clearly there will be improvements in the technology as we move toward production requirements, and those improvements will no doubt be used to buttress manufacturing margins as these designs move toward high-volume production.

Many other aspects of the LNA, power amplifier and frequency converter designs must also be optimized for these future data system applications. Parameters such as linearity (distortion products), power added efficiency, physical size (cost), and DC power consumption are very important in various aspects of these systems. As design efforts continue, we must be constantly vigilant in addressing all of the known requirements. As an industry, we must also build upon our knowledge and experience gained through the development of cellular and PCS infrastructure, and to anticipate some of the key requirements which in all probability have not yet be specified -- but will be as systems begin in operation.

ACKNOWLEDGMENTS

The author gratefully acknowledges Bob Street of Dielectric Laboratories Inc. for the use of the LTCC-M package photo as an example.

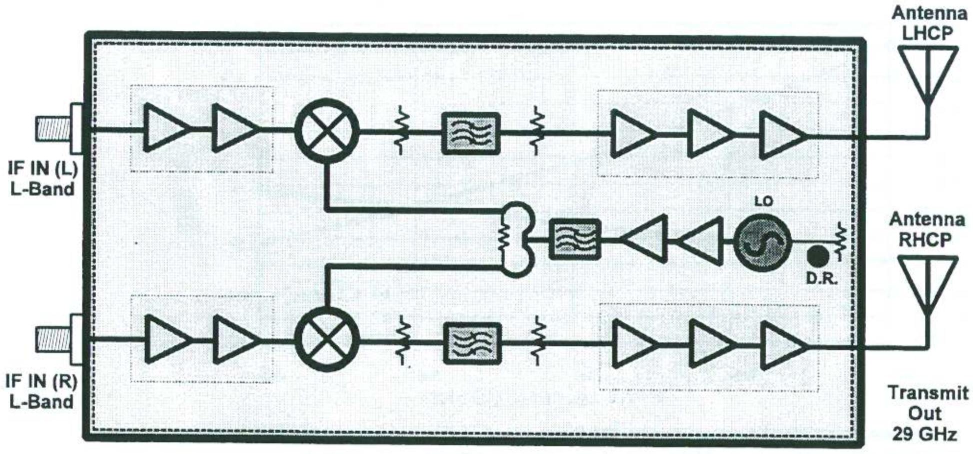


Figure 1: An Example dual-Polarization 29 GHz Transmitter for a Ground Terminal.

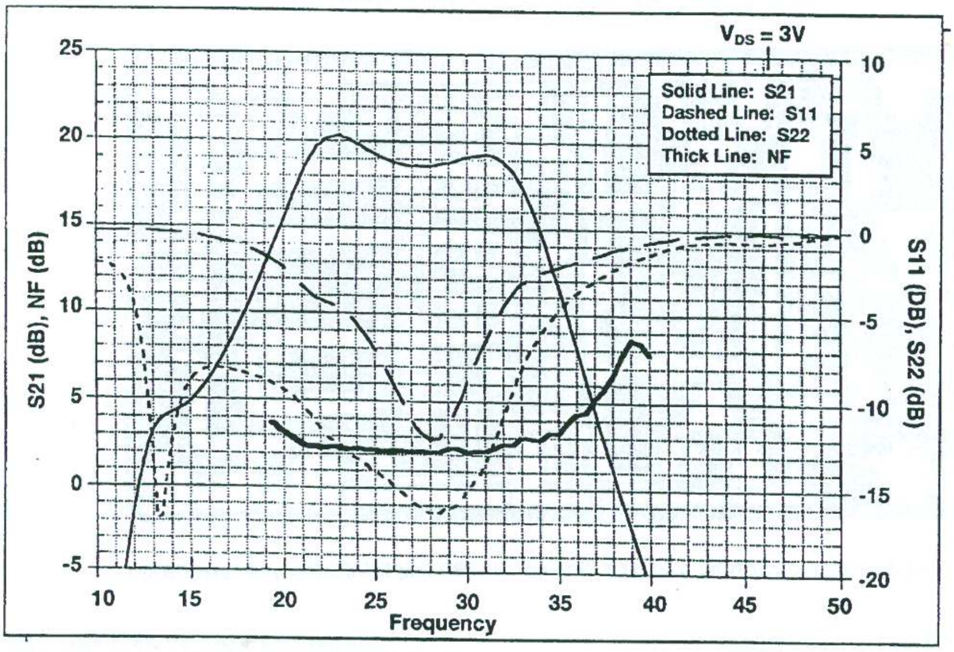


Figure 2: Measured Gain and Noise-Figure Performance for a 29 GHz MMIC LNA.

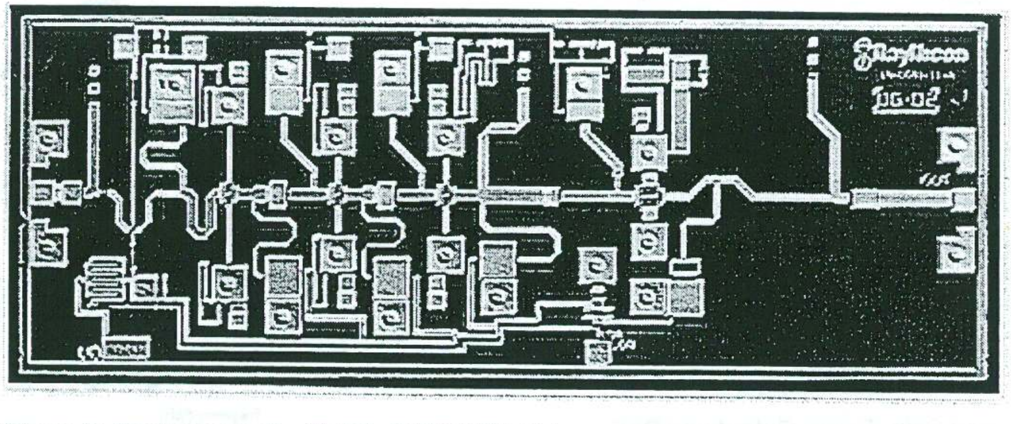
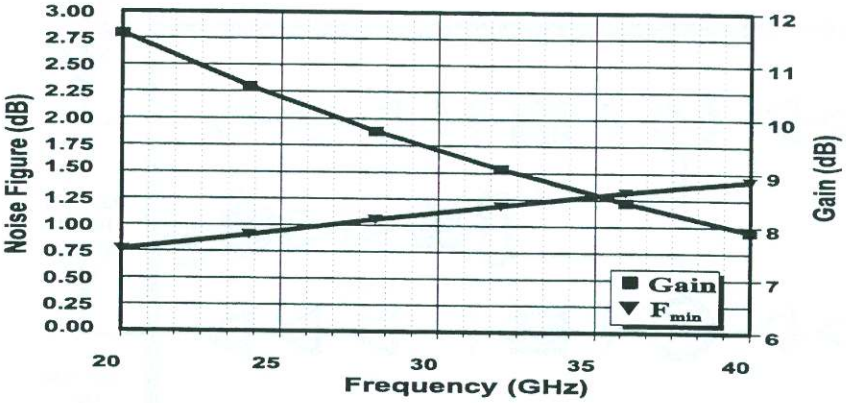


Figure 3: Photograph of a 20 GHz MMIC LNA Chip.



- Measured Gain and Fmin Data for a 0.15 x 100um MHEMT
- Bias Conditions: Vds = 1.0 V; Ids = 15mA; T = 25 C.
- Device Topology: Coplanar Device on a 4-mil GaAs

Figure 4: Measured Gain and F_{MIN} for a 0.15 x 100µm mHEMT Device.

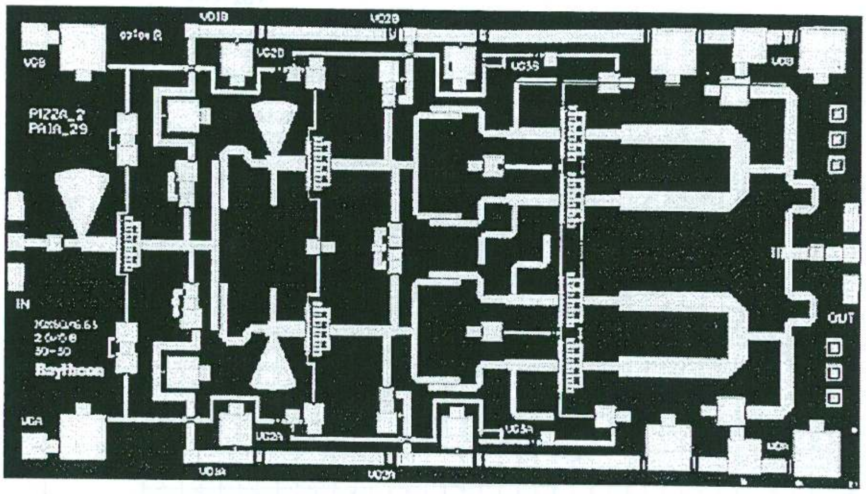


Figure 5: Photograph of a First-Generation 29 GHz MMIC Power Amplifier.

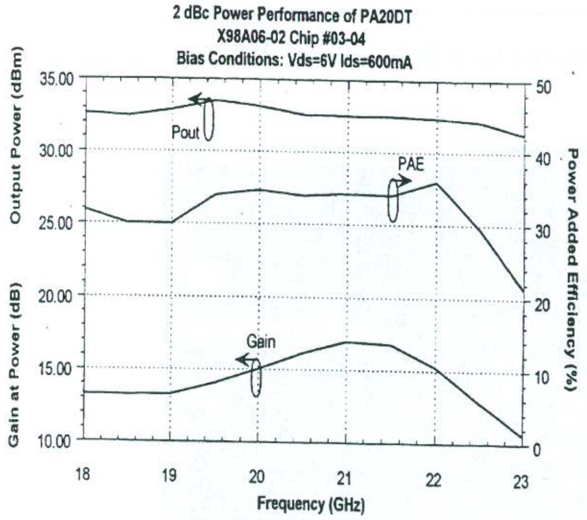

2 dBc Power Performance of PA20DT
X98A06-02 Chip #03-04
Bias Conditions: Vds=6V Ids=600mA

Figure 6: Measured Gain, Power Output and PAE For an 18-22 GHz 2-Stage MMIC Power Amplifier.

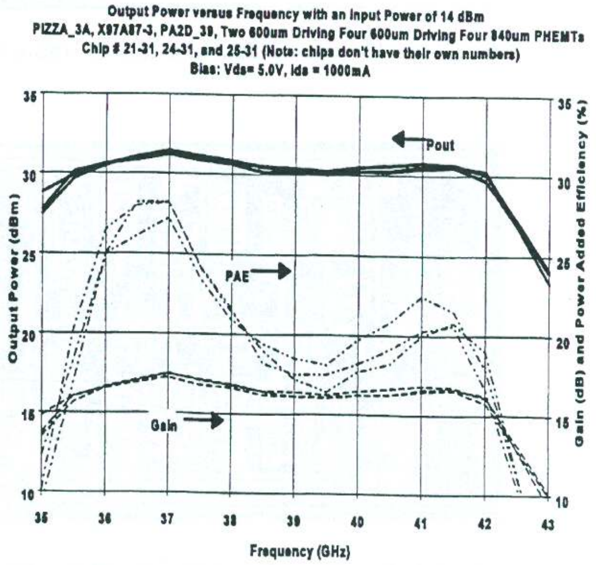

Output Power versus Frequency with an Input Power of 14 dBm
PIZZA_3A, X97A87-3, PA2D_39, Two 600um Driving Four 600um Driving Four 840um PHEMTs
Chip # 21-31, 24-31, and 25-31 (Note: chips don't have their own numbers)
Bias: Vds= 5.0V, Ids = 1000mA

Figure 7: Measured Gain and Power Output for a 37-40 GHz 3-Stage MMIC Power Amplifier.

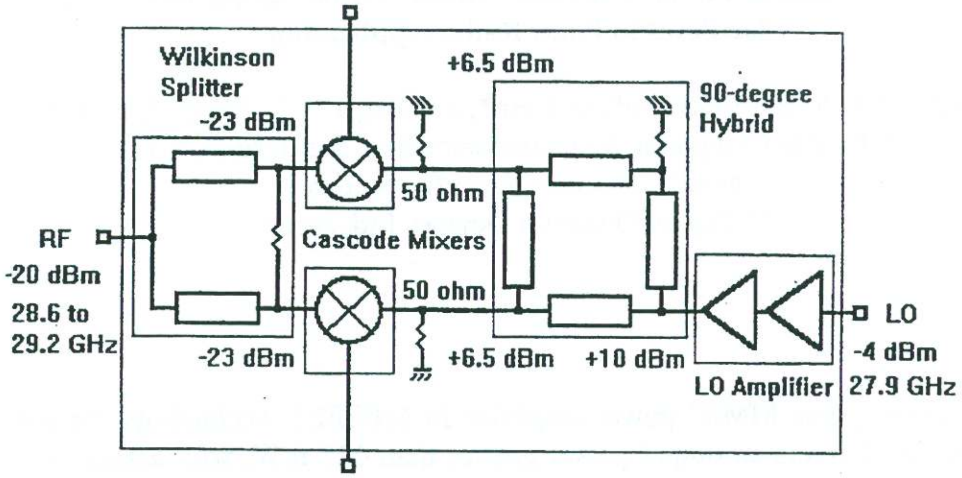


Figure 8: Block Diagram of an Image-Reject (I/Q) Mixer for a 29 GHz Receiver.

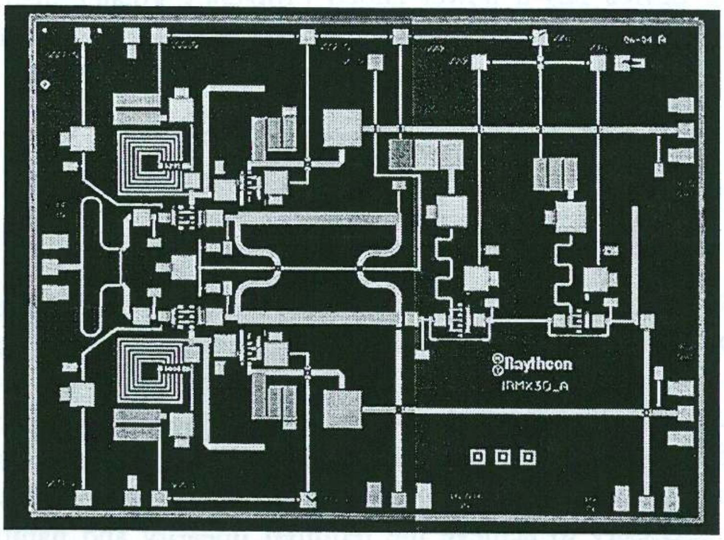


Figure 9: Photograph of the Completed MMIC I/Q Mixer for a 29 GHz Receiver.

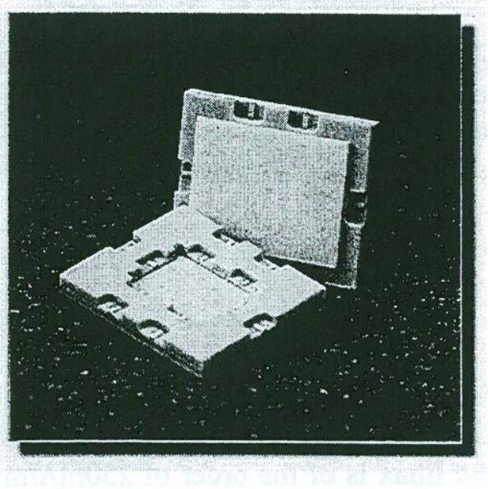
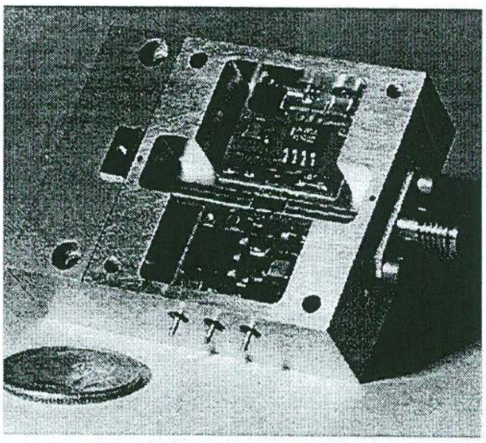


Figure 10: Photograph of a Low-Cost
LTCC-M Package Suitable
For mm-Wave Applications.



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