Performance evaluation of submicron channel GaN vertical transistors

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An electrical and thermal study of submicron GaN permeable base transistors is presented. Carrier transport in the intrinsic finger is studied with a drift-diffusion model, validated against ensemble Monte Carlo simulation. The effects of geometrical scaling are evaluated, in order to optimize the performance of the intrinsic device. Non-isothermal analysis of the complete multi-finger structure demonstrates that, for optimum performance, the heat sink must be placed on the top of the device.

INTRODUCTION

Although high performance GaN heterojunction FETs (HFETs) have been already demonstrated in several laboratories (see e.g. [1, 2, 3]), the relative immaturity of the manufacturing process of epitaxial films in III-N semiconductors remains a major obstacle to be overcome towards the realization of reliable planar transistors with reproducible properties. A promising alternative to FETs is offered by vertical devices, such as Permeable Base Transistors (PBTs, see Fig. 1), where the current flow along the vertical channel is controlled by a recessed or buried Schottky base contact. In fact, in wurtzite-phase nitride semiconductors vertical transport is less affected by the presence of defects, resulting in experimental values of bulk electron mobility usually higher along the vertical axis than for in-plane transport [4]. Moreover, thanks to the particular structure of PBTs, it is possible to obtain MESFET-equivalent gate lengths significantly smaller than current HFET gate linewidths; PBT scaling-down is limited only by the ability to control the thickness of the base contact metallization. Thus, PBTs potentially are competitive devices for the lower microwave range, typically X-band. The simplicity of the PBT structure allows for a relatively inexpensive fabrication process and provides the robustness required for power microwave applications; at the same time, the use of GaN will offer significant performance improvement over 4H-SiC vertical transistors. The present work extends the first performance evaluation of submicron GaN PBTs presented in [5]. The effects of scaling of the intrinsic finger (Fig. 1b) are studied with a drift-diffusion (DD) transport model, validated against ensemble Monte Carlo (EMC). The electro-thermal simulation of a multi-finger PBT (Fig. 1a) is performed on the complete structure, in order to assess the best strategy for heat sinking.

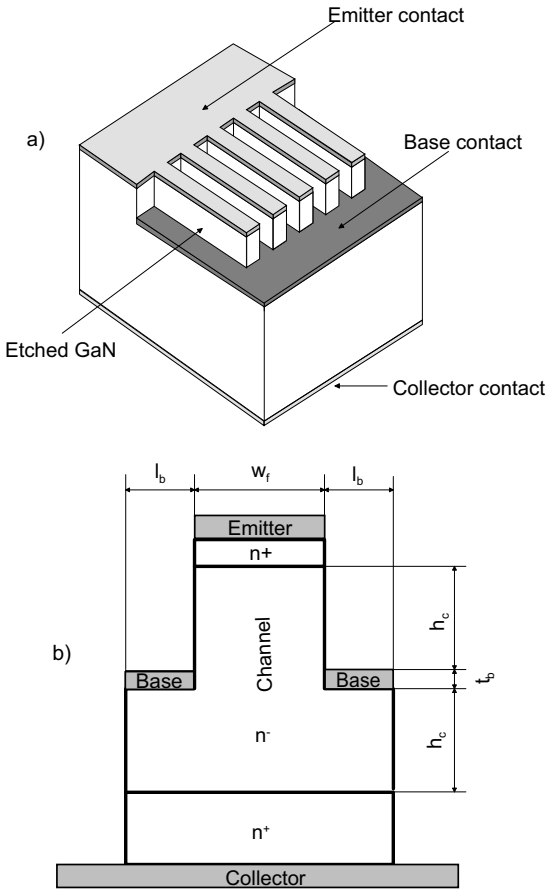

Figure 1: Layout of the simulated multi-fingered PBT structure and of the intrinsic region.

MODEL

Our EMC and DD codes are discussed in [5]. In addition to isothermal transport modeling, the assessment of the performances of power microwave devices requires the inclusion of thermal effects, since the temperature distribution can influence significantly the electrical behavior. In order to account for thermal effects in semiconductor devices, transport equations have to be solved self-consistently with the heat flow equation [6]:

$$C\frac{\partial T_L}{\partial t} = \nabla \cdot (\kappa \nabla T_L) + H \qquad (1)$$

where κ is the thermal conductivity, $C = \rho\, c$ is the heat capacitance, ρ is the specific mass density and c is the specific heat of the material. In general, κ and C are temperature dependent. Since we do not consider here transient effects, the temperature dependence of C can be neglected. For thermal conductivity, the simple power law model $\kappa(T) = \kappa_{300}/\left(T/300\right)^{1.5}$ is commonly used [6]. The experimental value of κ at 300 K for GaN is about 1.5 W/cm [7, 8]. The terms H and T_L denote the locally generated heat and the local lattice temperature. For the heat generation term, the following model has been used [6]:

$$H = \left[\frac{\left|\vec{J_n}\right|^2}{q\mu_n n} + \frac{\left|\vec{J_p}\right|^2}{q\mu_p p}\right] - T_L\left(\vec{J_n}\nabla P_n + \vec{J_p}\nabla P_p\right) + \\ + q(R-G)\left[T_L\left(P_p - P_n\right) + \phi_p - \phi_n\right] \tag{2}$$

The first term on the RHS of (2) represents Joule heat dissipation; the second term is the contribution from the Peltier and Thomson effects; the last term is the heating/cooling determined by carrier generation and recombination. When the heat flow equation (1) is included in DD simulation, the DD current equations have to be supplemented by additional terms:

$$\begin{aligned} \vec{J_n} &= -q\mu_n n\left(\nabla\phi_n + P_n\nabla T_L\right) \\ \vec{J_p} &= -q\mu_p p\left(\nabla\phi_p + P_p\nabla T_L\right). \end{aligned} \tag{3}$$

The absolute thermoelectric power for electrons and holes, P_n and P_p, are determined as follows [9]:

$$\begin{aligned} P_n &= \frac{k_B}{q}\left[\ln\frac{n}{N_c} - \left(\frac{5}{2} + \nu_n\right)\right] \\ P_p &= \frac{k_B}{q}\left[\ln\frac{p}{N_v} - \left(\frac{5}{2} + \nu_p\right)\right] \end{aligned} \tag{4}$$

where k_B is the Boltzmann constant; ν_n and ν_p describe the average energy dependence of the electron and hole momentum relaxation times as $\tau_n \approx E^{\nu_n}$, $\tau_p \approx E^{\nu_p}$, respectively. The lattice temperature dependence of the low field electron mobility is approximated as:

$$\mu_0\left(T_L\right) = \mu_0\left(\frac{T_L}{300}\right)^{\alpha} \tag{5}$$

where μ_0 is the low field mobility at 300 K, and the value of α has been obtained from [10].

SIMULATION RESULTS

The DD model used for the scaling and electro-thermal analyses is based on transport parameters derived from EMC [10], and its validation has included comparisons with EMC device simulations. Fig. 2 reports the calculated $I-V$ characteristics of the intrinsic cell of a PBT ($w_f = 0.2\,\mu$m, $h_c = 0.2\,\mu$m, t_b=20 nm and $l_b = 0.1\,\mu$m) [5]; the agreement between EMC and DD is very good up to $V_{CE} \approx 10$ V. The discrepancies at higher collector-emitter voltages can be traced back to the electron nonlinear transport regime in the channel, and could be significantly reduced by replacing DD with an energy-balance analysis [5], though it would imply a relevant increase in simulation complexity and computational cost.

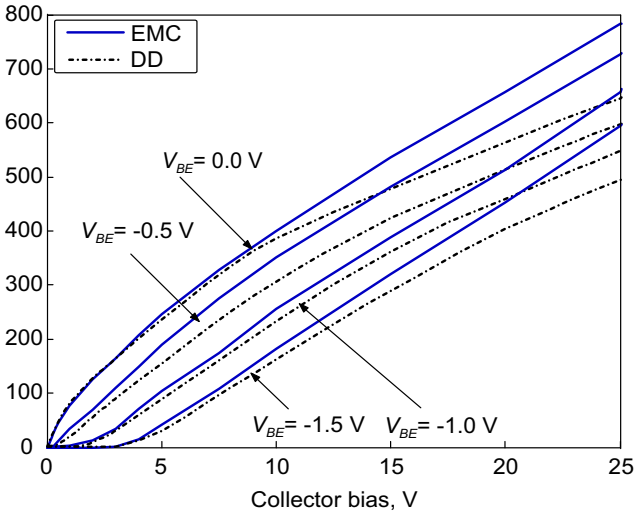

Figure 2: Calculated GaN PBT output characteristics: EMC (solid lines), DD (dash-dotted lines).

The dependence of the electrical characteristics of etched-emitter PBTs on the geometrical dimensions and doping concentrations has been studied with two different approaches. First, the finger width w_f has been changed by a factor K and the doping has been scaled accordingly to a factor $1/K^2$, in order to maintain the same depletion width at the middle of the device channel. The finger height and the metallization thickness have been kept constant, thus neglecting the two-dimensional nature of the base contact. The most important device parameters have been evaluated for w_f equal to 150 nm, 200 nm, 250 nm and 300 nm, while the other dimensions have been chosen as $h_c = 0.3\,\mu$m and $t_b = 70$ nm. As can be seen from Table 1, the cut-off frequency f_T decreases from 72 GHz for the smaller device down to 54 Ghz for the device with the larger finger width. The transconductance g_m presents the same trend. The smallest device has $g_m = 250$ mS/mm, which is comparable to the results obtained for conventional pHEMTs [11] and for the present generation of AlGaN/GaN HFETs [12]. The breakdown voltage for all these devices is estimated to be in excess of 80 V.

Second, also t_b has been scaled by a factor K, in order to take into account the two-dimensional nature of the base contact, and to evaluate at the same time the sensitivity of the device performances to the metallization thickness. From the values presented in Table 2, it is clear that the additional adjustment of the base thickness improves the device characteristics. It can

Table 1: Scaling effects on GaN PBTs with constant base thickness t_b

w_f, nm	150	200	250	300
N_D, 10^{16} cm^{-3}	8.9	5.0	3.2	2.2
t_b, nm			70	
g_m, mS/mm	250	208	172	152
$V_{\rm br}$, V	102	93	88	85
f_T, GHz	72	68	58	54

also be noticed that, even when the metal thickness is doubled, both g_m and f_T maintain values that are adequate for microwave amplifier applications.

Table 2: Scaling effects on GaN PBTs with variable base thickness t_b

w_f, nm	150	200	250	300
N_D, 10^{16} cm^{-3}	10.7	6.0	3.8	2.7
t_b, nm	60	80	100	120
g_m, mS/mm	307	256	228	203
$V_{\rm br}$, V	102	93	77	74
f_T, GHz	82	72	63	56

In order to investigate thermal effects on device performances and to study alternative cooling strategies, we considered a realistic multi-finger device structure composed of eight unit cells (each with $w_f = 0.2\,\mu$m, $h_c = 0.3\,\mu$m, t_b=70 nm, and base length $l_b = 0.1\,\mu$m) and having the base contact in a deep side etch. The thermal boundary conditions were set by placing a heat sink on the top or at the bottom of the device. The temperature distributions corresponding to these two cases are shown in Fig. 3 and Fig. 4 for a working point of $V_{CE} = 40$ V and $V_{BE} = 0$ V. When the heat sink is placed on the device top (for instance by using flip-chip bonding) the fingers are isothermal and share equally the total device current. On the contrary, if the heat sink is placed at the bottom, the cooling is much less efficient: the maximum device temperature is more than three times higher than in the former cooling configuration, and additionally a 10 % difference in temperature between the finger at the periphery and the central one is predicted. These combined effects have an obvious substantial impact on the device lifetime and reliability.

CONCLUSIONS

We have presented an analysis of submicron GaN PBTs having, as its main goal, the global structure optimization from the point of view of geometrical scaling and thermal effects. Electro-thermal simulations

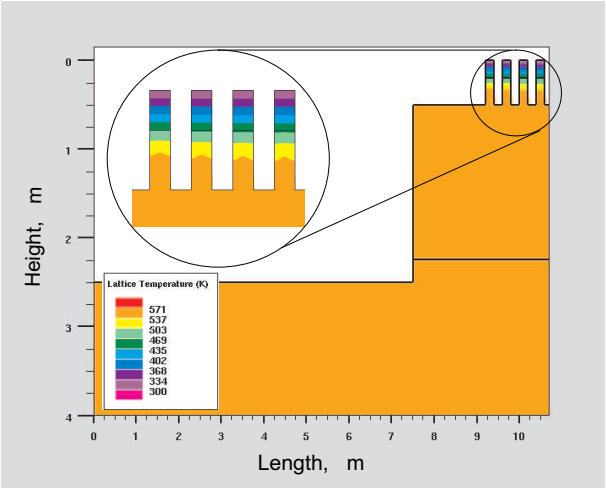

Figure 3: Lattice temperature distribution when the heat sink (at $T = 300$ K) is placed on the top of the device, at $V_{BE} = 0$ V and $V_{CE} = 40$ V.

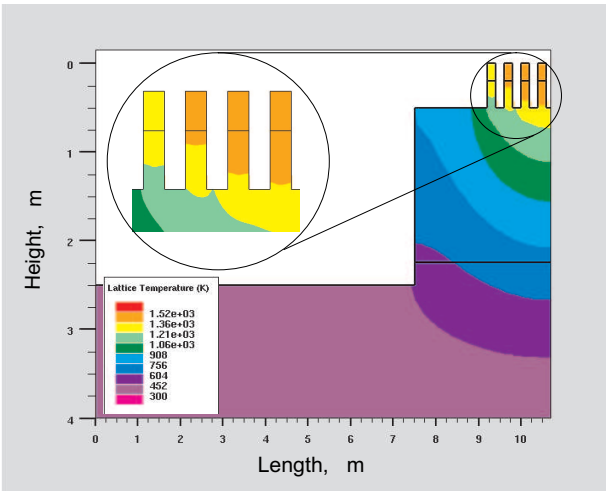

Figure 4: Lattice temperature distribution when the heat sink (at $T = 300$ K) is placed at the bottom of the device, at $V_{BE} = 0$ V and $V_{CE} = 40$ V.

have shown that, in order to obtain optimum performance, heat sinking has to be performed from the top of the device. Further investigations are being carried out to evaluate the breakdown voltage with a full band EMC simulator, and to fabricate the presented device structure.

ACKNOWLEDGEMENTS. This research was partially funded by BAE SYSTEMS through contract 4046-5 and by CNR (Italian National Research Council) through the MADESS II project. V. Camarchia was partially supported by a scolarship provided by Fondazione Sanpaolo. The authors would like to thank Prof. T. Moustakas, Dr. M. Wraback, Dr. D. Rathman, Prof. F. Bonani, Dr. S. Donati Guerrieri, and Prof. H.-E. Nilsson for useful discussions.

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