Effects of Self-Heating on Parameter Extraction for GaInP/GaAs HBT Nonlinear Models

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Abstract

This paper addresses the issues involved in developing a large-signal heterojunction bipolar transistor (HBT) model with particular emphasis on the role self-heating plays in the parameter extraction process. Starting from a physical analysis of the device, a novel, equivalent-circuit DC model is proposed which models both base and collector currents separately. However self-heating will play a large role in any measurements used in any associated parameter extraction technique developed in conjunction with the model. Therefore a thermal sub-circuit representing the device is first created both from measurements and knowledge of the transistor's physical properties. All DC parameters are then extracted from forward and reverse Gummel plots taken at several ambient temperatures which have had the effects of self-heating removed using a novel "thermal de-embedding" technique. S-parameter measurements made from 45MHz to 20GHz allow for determination of the model's dynamic elements to complete the large signal model. Finally, for verification purposes, DC output characteristics and several single-tone power sweep measured results are given which show good agreement with simulated behaviour.

DC Model Development

Almost all equivalent-circuit nonlinear models offered for GaAs based HBTs to date have been heavily based upon the original Gummel-Poon (GP) [2] model of the bipolar junction transistor dating from almost thirty years ago. This, in turn, based itself on Ebers-Moll (EM) [3] concepts such as constant Ic/Ib ratio in the medium current region. Unfortunately, the HBT normally demonstrates quite different behaviour in its Gummel plot (Fig2) compared to a BJT in its low, medium and high current regimes. Using Anderson's [1] energy band model for a HBT, an analysis of the physics of the abrupt junction HBT modeled in this work derives equations similar in form to those of EM:

$$J_E = -C_{E1}\left(\exp\left(\frac{V_{BE}}{nV_T}\right)-1\right)+C_{E2}\left(\exp\left(\frac{V_{BC}}{nV_T}\right)-1\right)$$
$$J_C = C_{C1}\left(\exp\left(\frac{V_{BE}}{nV_T}\right)-1\right)-C_{C2}\left(\exp\left(\frac{V_{BC}}{nV_T}\right)-1\right) \quad (1)$$

where: , for example,

$$C_{C1} \propto \exp\left(-V_{BE}/V_T\right) \quad (2)$$

Since both the saturation currents and the ideality factors (n) can be shown to depend on the BE junction voltage rather than Vce, the current gain of the device will clearly be a function of Vbe even in the medium current region. Therefore the concept of a constant current gain is redundant and an equivalent circuit which separately models both Ib and Ic may be presented as in Fig1. Each current's curve is split into three regions. At low currents D2 models the "leakage currents" made up of recombinations at the emitter-base junction interface due to the large concentration of surface states existing at the junction surface. This is particularly the case for GaInP where there is often lattice mismatching with the GaAs at the emitter-base. Collector current is also affected due to its nonuniform dependence on the base current. D1 models the medium current

region for the base current and this is extended to the high - current region using a linear, series resistor (R1 in Fig1) whose purpose is to change the ideality factor of D1 by effectively altering Vbe_internal. It should be noted that the placement of this resistor is directly from the authors' analysis resulting in equation (2), however physically this resistor reflects the drop in Vbe-internal due to intrinsic base and emitter resistances which manifests itself at larger currents.

Thermal Modelling and Parameter Extraction

The transistor under test had 6 emitters of 2X40um in a fishbone arrangement and, while not a very large device, it was vital to first achieve a good thermal model - not only for device simulations but also before the remainder of the parameter extraction process could take place. A single-pole thermal model was chosen as suitable for a HBT of this size and the thermal resistance (Rth) was calculated using Fox and Lee's [4] formulae and the Brice [5] relationship for the conductivity of GaAs as a function of doping. Measurements of the device itself using a technique similar to that of Dawson[6] involved using the base-emitter voltage as an internal device "thermometer". The procedure was carried out at several ambient temperatures and using Brice, the Rth nonlinear dependence on temperature may be written as:

$$R_{TH}(T,T_O) = R_{TH}(T_O).\left(\frac{T}{T_O}\right)^{1.2} \tag{3}$$

Both calculations and measurements were found to be in good agreement giving respectively an Rth of 188 and 176 C/W at an internal device temperature of 50C. Fig2 illustrates the change of thermal resistance with temperature. The thermal capacitance used in the model Cth was estimated from the thermal time constant of the device.

With a device thermal time constant of the order of 1ms, it can be extremely difficult to measure accurately DC Gummel plots using pulses as the transistor and surrounding substrate are repeatedly being heated and cooled. However in this paper, the measurements are made at continuous bias and self-heating effects (which predominate at high currents) are "accounted for" in the resulting data using the thermal sub-model and a knowledge of how the ideality factor and saturation current changes with temperature. The latter is measured by stepping the ambient temperature in a region of the Gummel plot where self-heating is non-evident (i.e. the medium current region). While a simple polynomial expression is suitable for the ideality factor, the saturation current requires an expression of the form:

$$I_{ST} = I_{STO}\exp\left(\frac{1}{T_O} - \frac{1}{T_O + T}\right)T_S \tag{4}$$

Knowing the power dissipated in the device at each bias step, the device temperature can be found from the thermal submodel. When used in equations (4) and (5) an "ideal" curve including self-heating may be plotted and the series resistances found from the deviations of the measurements from the "ideal curve". Thus the standard parameters of D1, D2 were found from the low and medium currents respectively. To complete the DC extraction D3 was extracted from a reverse Gummel plot and was found to be largely independent of temperature. The output characteristics of the transistor are shown in Fig4 in order to verify the model and extraction of the DC parameters.

To extend the model to account for dynamic effects, the junction capacitances were added to the DC model using a simple optimisation procedure. The HBT scattering parameters were measured using a HP85107C vector network analyser at several bias points distributed over the forward active DC output characteristics. Due to the complexity of the DC model it frequently proves difficult to obtain good fits at low Vce voltages and so this region was lightly weighted during the optimisation process. Typical fits for the S-parameters may be seen in Fig5.

Verification of the nonlinear model took the form of power sweep measurements using a 2GHz input tone to generate and compare with simulation the 2nd and 3rd harmonics for the device in common emitter mode.

Conclusions

A novel HBT nonlinear model is presented together with an associated parameter extraction technique for use with GaInP / GaAs transistors. An emphasis is placed upon the DC modelling of the device, in particular in relation to self-heating which often is ignored in deriving parameters and which thus leads to large errors and unrealistic results. Verification of these methods is in two parts: firstly the DC output characteristics may be accurately predicted and secondly the model can also be used for large signal simulations.

References

[1] R.L Anderson, "Experiments on Ge-GaAs heterojunctions", Solid-State Electron., vol5, p341-51, 1962.

[2] H.K Gummel and H.C Poon, "An integral charge control model of bipolar transistors", Bell Syst. Tech. J49, p827-52, 1970.

[3] J.J. Ebers and M.L. Moll, "Large signal behaviour of junction transistors", Proc. IRE, vol42, p1761-72, 1954.

[4] R.M Fox, S. Lee, "Scalable small-signal model for BJT self-heating", IEEE Electron Device Letters, vol12, no12, p649-51, 1991.

[5] J.C Brice, "Properties of GaAs", EMIS data review, London: INSPEC, 1990.

[6] D.E Dawson, "CW Measurement of HBT Thermal Resistance", IEEE Trans. Electron Devices, vol39, no10, Oct 1992.

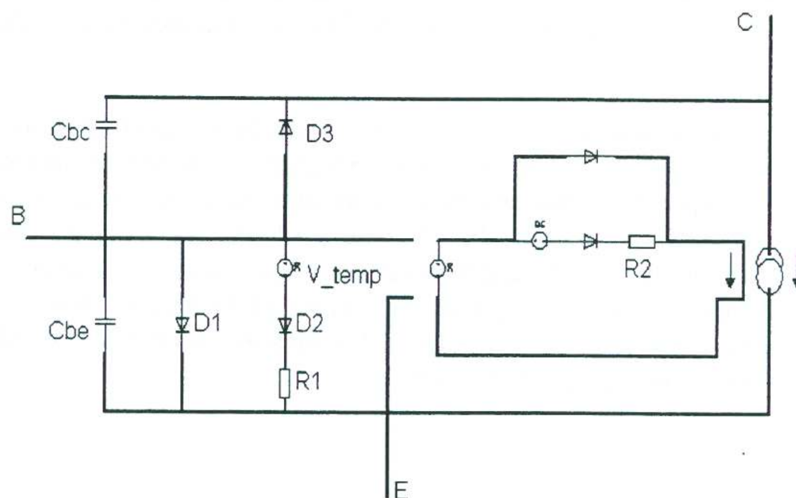

Fig1: Nonlinear HBT model schematic

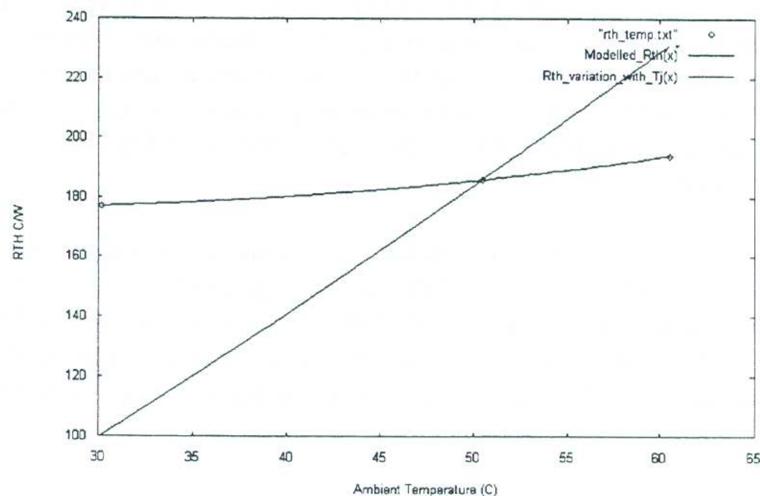

Fig2: Thermal Resistance vs Temperature

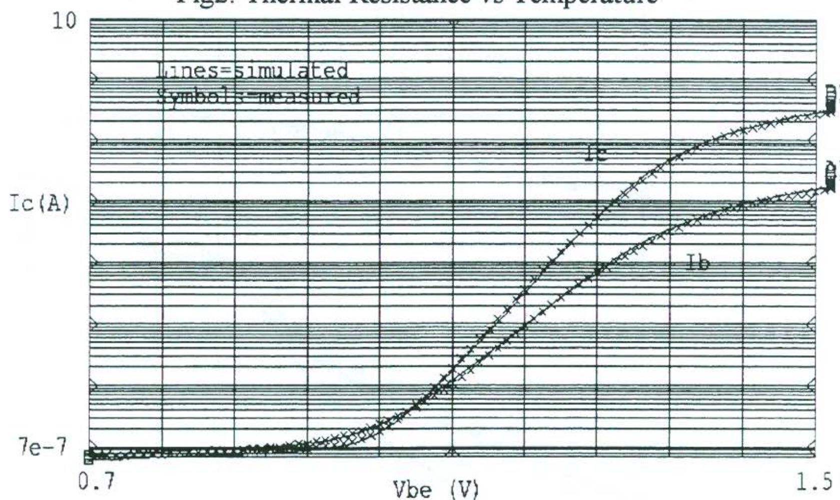

Fig3: HBT Gummel Plot

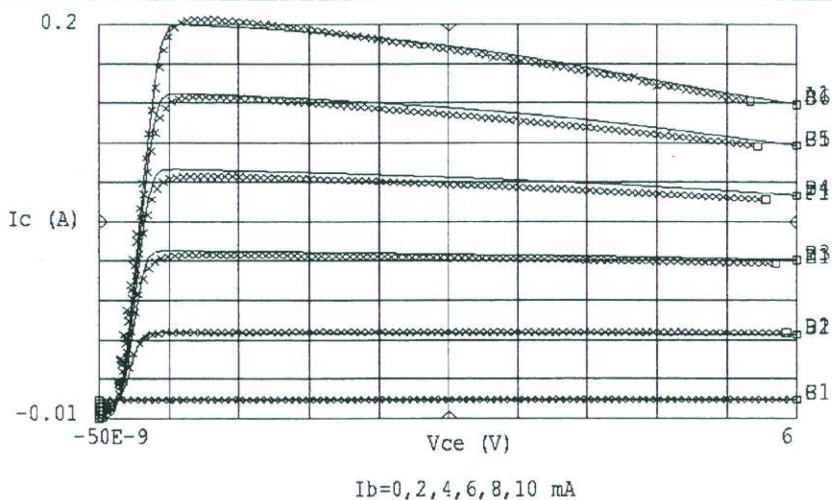

Fig4:Output Characteristics: Measured and Simulated

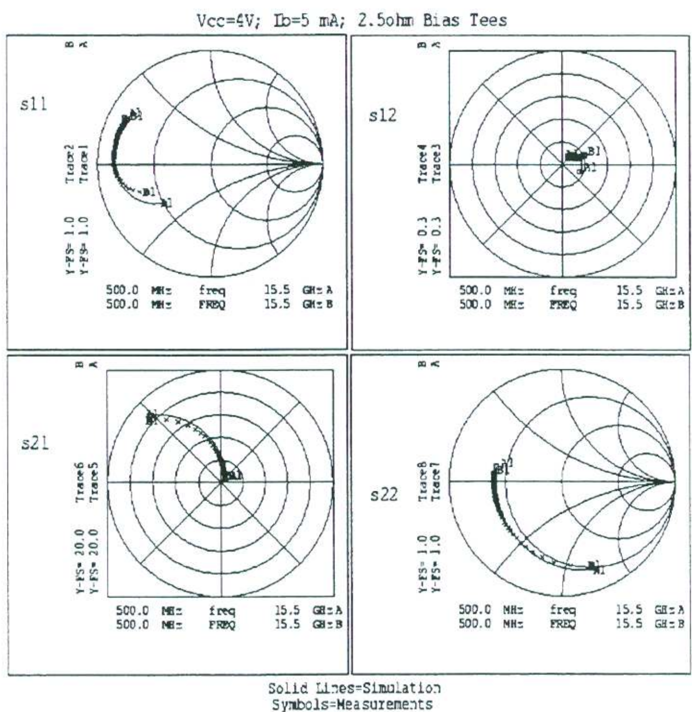

Fig5: Scattering Parameters

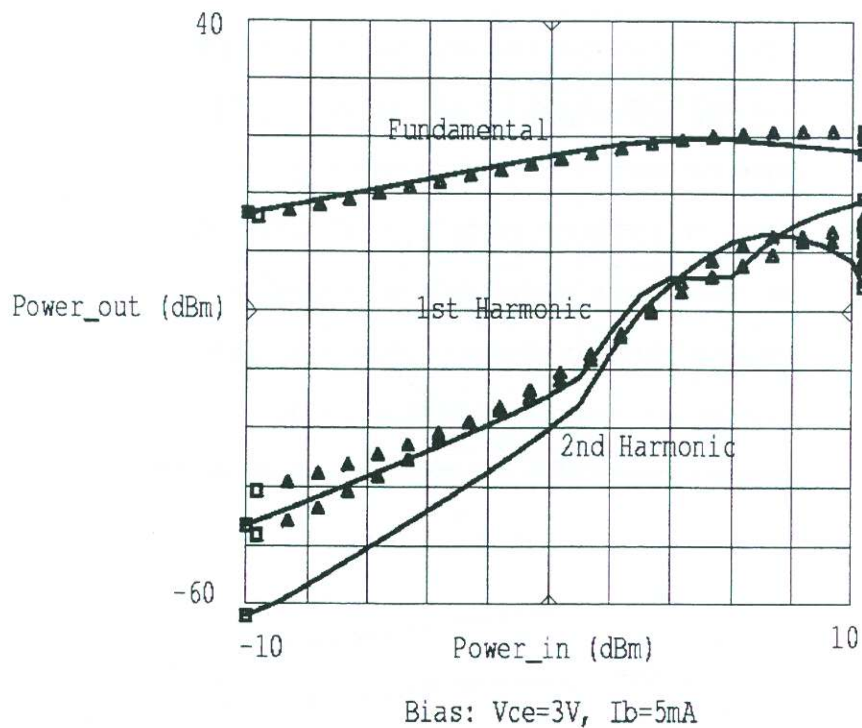

Fig6: Power Sweep Measurement at 2GHz