An Advanced GaAs/InGaP HBT MMIC Process

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Abstract

An advanced, general purpose GaAs/InGaP HBT process has been developed at GEC Marconi Materials Technology Ltd. (GMMT). A range of digital and analogue circuit functions has been successfully implemented, demonstrating the capability of the process to provide high linearity and broadband circuits for communications applications. IP_3-P_{1dB} figures of up to 11.3dB have been measured and high density, high speed digital circuits have also been demonstrated with frequency divider toggle rates of over 16GHz. GMMT are also developing a variant of the process with improved breakdown voltage specifically for power applications.

This paper gives an overview of the process technology and of demonstrated circuit performance. Results of accelerated lifetests are also presented.

Introduction

GMMT's HBT process technology has been developed alongside its HEMT (H40) and MESFET (F20) MMIC processes, with most of the process stages to define the passive components common to all. Two HBT process variants have been developed in parallel, the standard process which is aimed at small signal and digital applications and has a breakdown voltage (BV_{CEO}) of 11V, with an f_T and f_{MAX} of greater than 50GHz, and the power variant, aimed at high frequency (C, X and K band) broadband power applications which has a breakdown voltage of greater than 23V.

GMMT's HBT Technology

GMMT's GaAs/InGaP HBT technology is based on a GaAs semi-insulating substrate using ion implantation to provide device to device isolation. GaInP is used as the emitter material to provide the heterojunction between emitter and base. This is preferred to AlGaAs which is used by the majority of HBT manufacturers, due to its superior semiconductor properties and ease of manufacturing. Passive components include a dual nichrome thin film resistor process producing both 20Ω/sq and 200Ω/sq resistors, spiral inductors and MIM capacitors. A schematic cross section of a GaInP/GaAs HBT is shown in figure 1. Beta values are typically in the range 100-150 for normal operating currents, and the standard emitter width is 2μm.

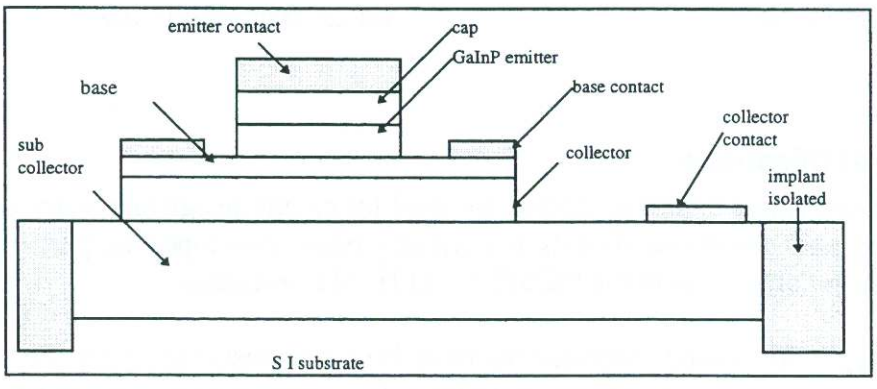

Figure 1 Schematic Cross Section of a Heterojunction Bipolar Transistor

The standard process is aimed at small signal and digital applications over the frequency band DC-20GHz. Common emitter breakdown voltage is typically 11V with a saturation voltage of less than 1V which makes the process also suitable for medium power applications. The majority of circuit demonstrators, including all the digital circuits, have been manufactured using this process.

The power variant employs a similar process technology with minor changes to the material specification to yield an increased breakdown voltage of over 23V. Development of the process has included an assessment of the effect of thermal ballasting in order to reduce current collapse effects in multi-finger power devices. This is achieved by including a large resistor (several hundred Ohms) in series with the base of the device and a decoupling capacitor in parallel with the resistor to provide a short circuit RF path at high frequencies. Figure 2 shows measured I-V curves for an unballasted 4 finger 40μm device, showing thermal collapse occurring at a collector voltage of 7V and a current density of 25kA/cm^2. This phenomenon is brought about when a single finger takes all the device current due to thermal runaway effects[1][2]. The current gain of this 'hot finger' then drops significantly due to the negative temperature coefficient of β which leads to a significant drop in total device current as can be seen in figure 2. An increase in base current also follows, which leads to an increased DC voltage drop across the resistor and a reduced applied voltage across the base-emitter junction, which in turn reduces the collector current of that particular finger. Figure 3 shows measured I-V curves for an identical device to that in figure 2, with base ballasting resistors included. No thermal collapse is observed up to 10V V_{CE} at the same current density as for the unballasted device. The required passive components for this can be included on chip, although at low frequencies (<2GHz) the G_{MAX} of the device is limited due to the increasing impedance of the parallel resistor and capacitor. At X-band frequencies the size of capacitor required to decouple the resistor is relatively small so that it can be included as part of the device structure and be modelled as a single device, which is advantageous for circuit design accuracy.

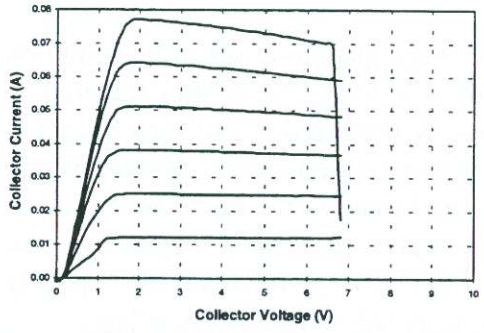

Figure 2 Measured I-V Curves for an Unballasted 4x40μm Multifinger Device

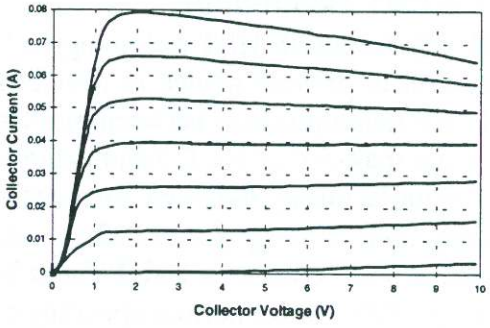

Figure 3 Measured I-V Curves for a Ballasted 4x40μm Multifinger Device

HBT Circuit Applications

Gummel Poon and linear hybrid pi models are used for circuit design and analysis. A range of scaleable linear and non-linear models is currently being developed as part of the GMMT foundry service in common with the MESFET and HEMT processes.

Many circuit types for various applications have been demonstrated using the HBT process. These include small signal and power amplifiers, log amps, mixers, oscillators, limiters and frequency dividers.

A range of medium power X band amplifiers with superior linearity has been designed and manufactured in order to demonstrate the advantages of HBT technology for X-band high linearity applications. Figure 4 shows a plot of the measured gain and return losses for a single stage amplifier. A P_{1dB} value of 20.7dBm was measured with a third order intermodulation product of 32.0dBm, giving a IP_3-P_{1dB} value of 11.3, and a power added efficiency of 35%. This was achieved at a bias of J_C=18.75kA/cm^2 and V_{CE}=5V for each finger of the two, 2x40µm emitter devices, giving an IP_3-P_{DC} figure of 5. A diagram of the chip layout is shown in figure 5.

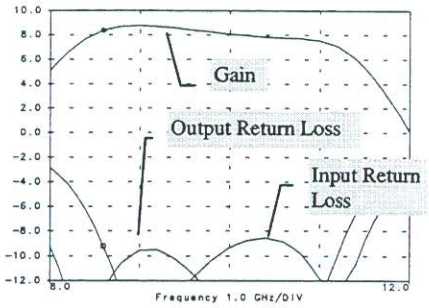

Figure 4 Gain and Return Losses for Medium Power High Linearity X -Band Amplifier

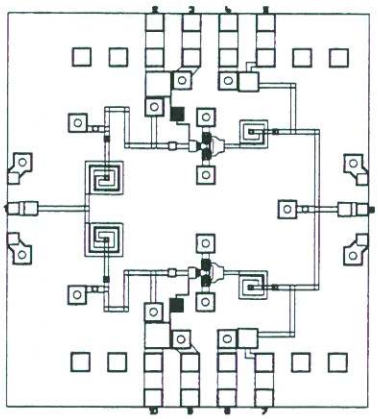

Figure 5 Chip layout for X-band amplifier

DC-3GHz Darlington amplifiers with a gain of 30dB and an output power of 21dBm have also been demonstrated[3] with noise figures of less than 3dB in band. The low frequency gain of the circuit is limited only by external decoupling capacitors. An application for such circuits as optical modulator drivers for 2.5Gb/s applications has been identified and evaluated. The circuit gives 5.4V_{P-P} output voltage swing across the band DC-3GHz, which exceeds the bandwidth capability of commercially available devices. The circuit is also useful as a 50Ω gain block in many low frequency wireless communications applications. The circuit chip area is less than 1mm^2 and uses through-GaAs vias to achieve backface grounding of the circuit. Figure 6 shows the gain of 20 such circuits across a wafer with a yield of 80%, showing the excellent uniformity of the process. Figure 7 shows the chip layout. This circuit is available as a GMMT standard product type P35-6100.

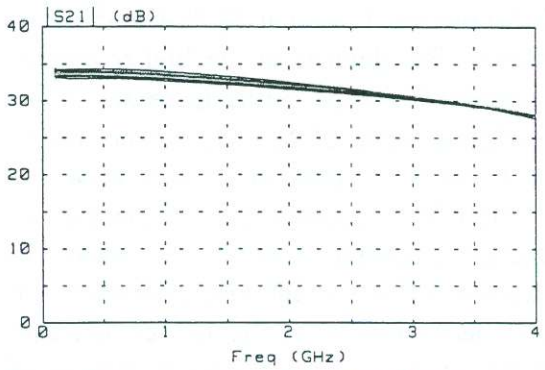

Figure 6 Measured Gain of 20 P35-6100 Darlington Amplifiers on a single wafer

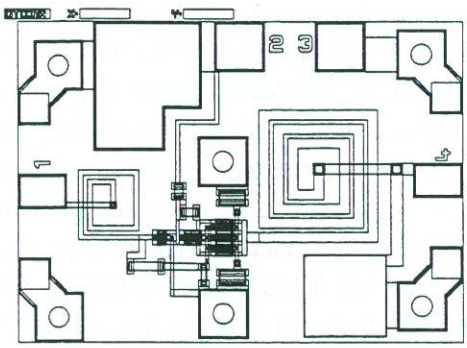

Figure 7 P35-6100 Chip Layout

Two new Darlington gain block amplifiers have been designed, aimed at DC - 3GHz and DC - 8GHz applications. These are 'vialess' circuits with a chip area of less than 0.2mm^2. The circuits also provide high IP3 values of +35dBm for an output power of +18dBm. Both circuits will be available as GMMT products type P35-6101 and P35-6102. These circuits are aimed at wireless communications applications and are biased from a single 5V supply.

Divide by 2 prescalers have been demonstrated with a maximum toggle frequency of over 16GHz and DC power consumption of 400mW. Figure 8 shows a wafer map of maximum toggle frequencies for a single divide by two circuit per array. Divide by 4 circuits have also been realised with a toggle frequency of up to 15GHz. Digital circuits with over 200 transistors have been realised in chip areas of less than 7mm^2, with good yields.

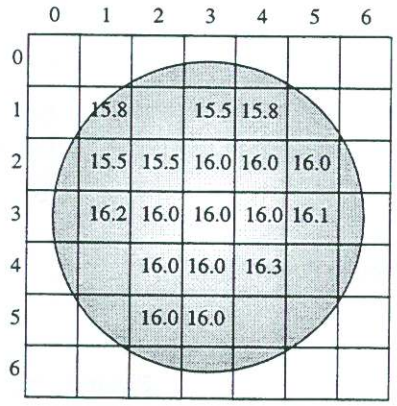

Figure 8 Maximum Toggle Frequencies of divide by 2 prescaler circuits across a single wafer

HBT Reliability

Accelerated lifetest work has been carried out to assess the relationship between the device junction temperature and device lifetime. Single finger devices biased at normal circuit operating currents and subjected to elevated temperature conditions were measured before and after testing. Feedback control was used to keep V_{CE} and I_C constant, and thermal modelling techniques were used to obtain the device junction temperature for a given ambient temperature and device bias. Devices from a single representative batch of wafers were split into four test groups consisting of devices at two oven temperatures, 115°C and 130°C, and two current densities, 12.5kA/cm^2 and 18.75kA/cm^2. All devices were biased at a voltage of 4V. Two temperatures were used in an effort to calculate an activation energy for any degradation mechanism involved. No failures have been recorded to date and after an initial increase in β (which is widely observed[4][5]), no degradation for devices at the lower current density was measured. Figures 9 and 10 show graphs of β vs time for devices biased at 12.5kA/cm^2 and at junction temperatures of 145°C and 160°C respectively. For devices at the higher current density of 18.75kA/cm^2 some degradation in β was observed after an initial increase. After 3000 hours of lifetest no device had degraded to its original value of β, therefore no device failures were recorded. Figures 11 and 12 show graphs of β vs time for devices biased at 18.75kA/cm^2 and at junction temperatures of 163°C and 178°C respectively. A measure of the increase in reaction rate due to the increased junction temperature of devices shown in figures 11 and 12 can be obtained by observing the increase in the average rate of degradation in β and using this value to calculate an activation energy based on the device junction temperatures. A value of 0.8eV was obtained using this method, which yields a lifetime of over 15 years for a device operating continuously at a junction temperature of 125°C. These

results show the process capability for device operation at higher current densities allowing the design of circuits for high power applications without compromising reliability.

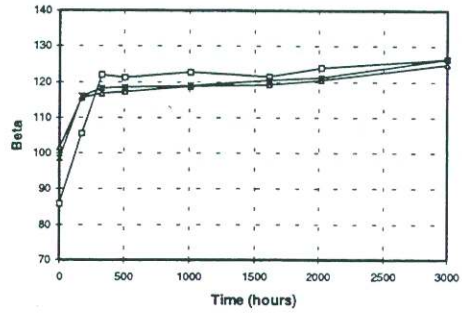

Figure 9 β vs time for devices at 145°C junction temperature and 12.5kA/cm^2

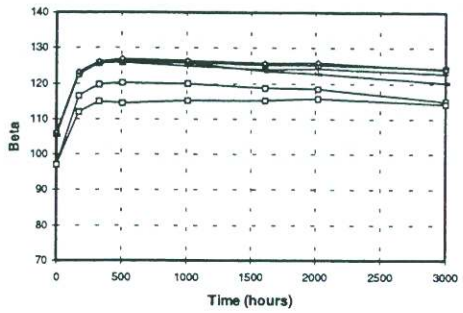

Figure 11 β vs time for devices at 163°C junction temperature and 18.75kA/cm^2

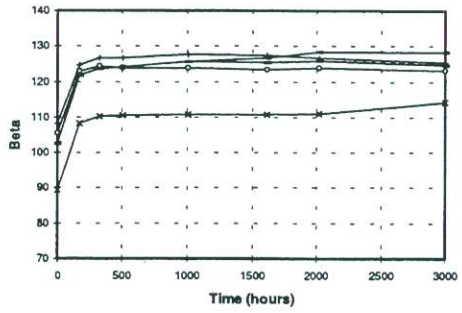

Figure 10 β vs time for devices at 160°C junction temperature and 12.5kA/cm^2

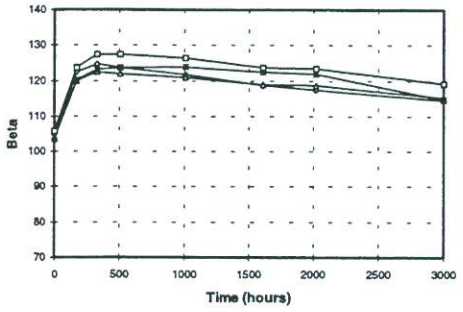

Figure 12 β vs time for devices at 178°C junction temperature and 18.75kA/cm^2

Conclusion

A GaAs/InGaP HBT MMIC process has been developed at GMMT. A wide range of circuit functions has been successfully implemented, demonstrating the advantages of the technology for high linearity, high efficiency applications, and also high density high speed digital applications. Device reliability has been assessed, and a lifetime of over 15 years for continuous operation at 18.75kA/cm^2 and a junction temperature of 125°C has been calculated.

Acknowledgements

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References

[1] W. Liu et al, "The Use of Base Ballasting to Prevent the Collapse of Current Gain in AlGaAs/GaAs Heterojunction Bipolar Transistors", 1996 IEEE Transactions on Electron Devices, Vol 43 No. 2, pp 245-251

[2] W. Liu, "Thermal Management to Avoid the Collapse of Current Gain in Power Heterojunction Bipolar Transistors", 1995 GaAs IC Symposium, pp147-150

[3] B. L. Nelson et al, "High Linearity :Low DC Power GaAs HBT Broadband Amplifiers to 11GHz", 1990 GaAs IC Symposium, pp79-82

[4] S. J. Prasad et al, "Reliability of Carbon Doped Base AlGaAs/GaAs HBTs as a function of Collector Current", 1993 Materials Research Society Symposium Proceedings pp609 - 614.

[5] J. Y. Chi et al, "Mechanism for the initial Current Gain Increase in Carbon Doped Heterostructure Bipolar Transistors", 1997 GaAs REL Workshop Proceedings pp7-12