Advanced GaAs MMIC Key Components for Telecommunication Modules

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The next generation of telecommunication modules will be more advanced and will definitely contain GaAs MMIC technology to achieve lightweight, low prices and expected reliability. The "point to point" communication links are in the moment the driving factor for these MMIC developments but will be followed by "point to multipoint" applications. The frequencies of interest are well known and the developments concentrate on Ku and Ka-band chips. To be successful in this market reliable, stable and inexpensive high performance technologies are needed. This paper describes MMICs, which have been developed in the recent past for these applications.

Figure 1 decribes the typical content of a telecommunication transceiver module with oscillator, receiver and transmitter chain. The frequency generation concept today uses normally oscillators below 10 GHz plus multipliers and digital dividers for two reasons. First the VCO has to be linked to a PLL and second the phase noise of the oscillator has to be as low as possible. VCO for frequencies up to 40 GHz have been already presented in sufficient quality **/1/**, the problem are frequency dividers for these frequencies with secure mode of operation and/or low DC-power consumption. Commercial available dividers/prescalers operate nowadays up to 12 GHz. Below this frequency limit GaAs based technologies are not the only choice. Nevertheless, all other MMICs within telco modules, as multipliers, mixers, upconverters, LNAs, buffer/driver amplifiers and power amplifiers, are a domain of GaAs. The task here is to find the optimum between requested module specification and MMIC specification. Module market numbers are often not so high, that absolutely specialised MMICs for one application only are the way to hit the cost frame. MMICs for different applications are envisaged. Up to now it seems, that mixers are too special, but the design of amplifiers can take this goal into account.

The frequency bands for communication according to ITU are well known and span from 7 GHz over 13, 15, 18, 23, 26, 28 to 38 GHz. Link budget calculations lead quickly to the following tasks:

- Output power has to be stabilised versus a wide temperature range,
- Output power has to be controlled versus a large power range
- Output power (depending on frequency band) has to be up to 1 Watt with good PAE

Two different amplifier types are therefore described in the following: Gain controllable driver amplifiers (DVGAs) and power amplifiers.

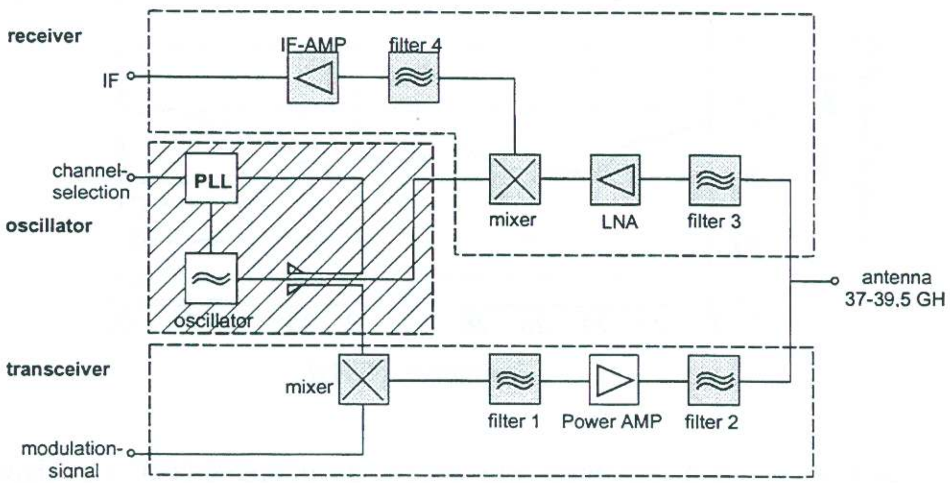

Figure 1: Principal block diagram of telecommunication module

Gain controllable driver amplifiers

Two different gain controlling elements are often used for DVGAs: Dual gate FETs /2/ or controllable attenuators. Dual gate amplifiers showed good performances and small chip sizes but due to the floating potential between the gates saturated output power is restricted compared to single gate FETs. This leads to linearity problems within the amplifier chains. For products addressed here reliability is a big issue! The status of dual gate FETs with respect to these points is not mature enough. Figure 2 shows a chip layout of a 20-40 GHz DVGA with integrated power attenuator (PAD), realised in UMS' quarter micron pseudomorphic HEMT technology (PH25).

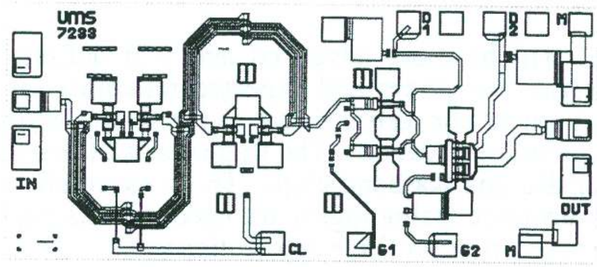

Figure 2: Layout of a 20-40 GHz DVGA (0.9mm x 2.06mm).

The PAD is a Lange coupler, where two of its ports are terminated by a cold FET and a 50 Ohm resistor each. If both cold FETs are "closed", the power will be divided towards these two FETs, reflected and appears at the fourth port. The attenuation is low, if the resistor of the Drain-Source path of the FETs is controlled towards lower values, more and more power vanishes within the 50 Ohm resistors and the insertion loss of the PAD increases. The size of the involved FETs has to be chosen so, that parasitic values, linearity and output power to be handled has to be taken into account. In this case, where the handling of up to 20 mW is foreseen, a gate periphery of 2 fingers à 30 µm have been chosen.

Figure 3a shows the small signal gain and return losses of this DVGA. A flat gain of 10dB is achieved for minimum attenuation. In addition the return losses are better than 10dB for the mounted device under all conditions, which is a result of the balanced configuration of the PAD and the unaffected S22 of the last stage of the amplifier. The measured results for the dynamic of the DVGA are shown in Fig. 3b for different frequencies. Obviously, over a voltage swing of 0.15V a variation of 20dB can be achieved. The small signal gain for different control states versus frequency are displayed in Fig. 3c. These results demonstrate that for a dynamic range of more than 20dB the gain remains flat versus frequency.

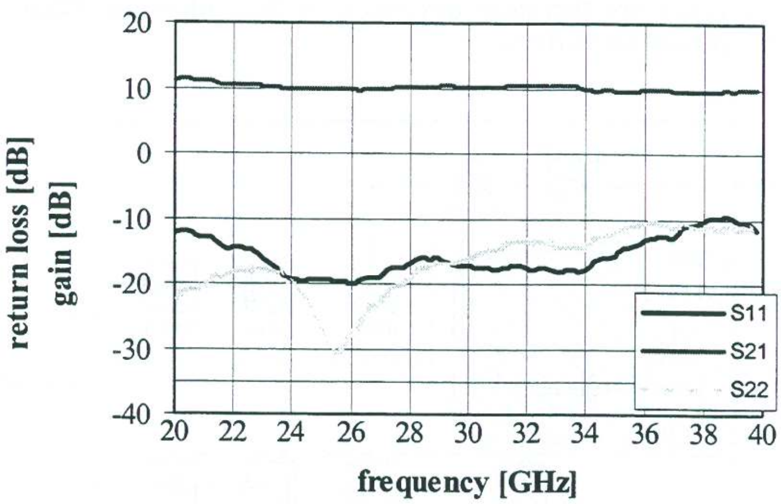

Figure 3a: Gain and return loss at maximum gain state of the mounted DVGA as shown in Fig.2.

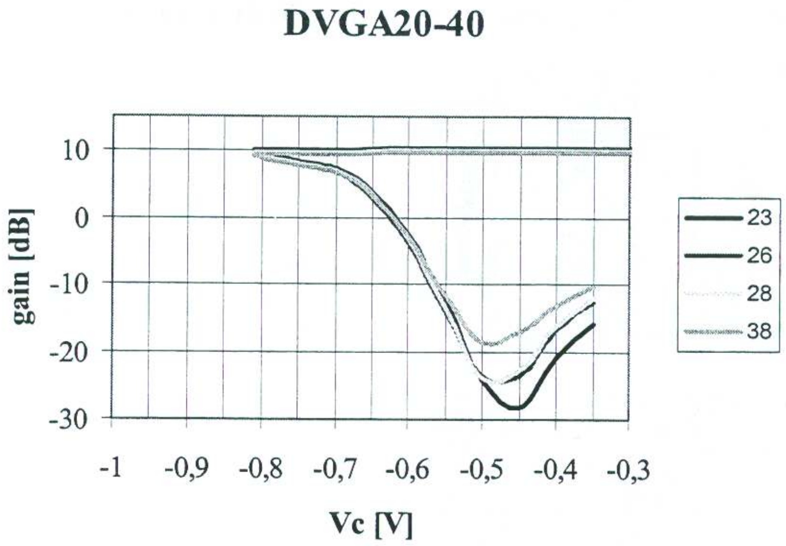

Figure 3b: Gain vs. control voltage at different frequencies for the DVGA as shown in Fig.2.

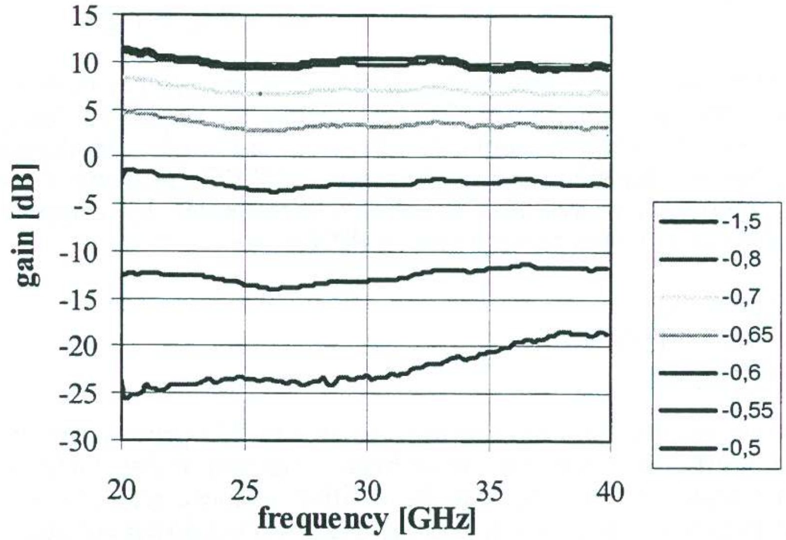

Figure 3c: Small signal gain vs. frequency for different control voltages applied to DVGA (Fig.2).

Gain controllable power amplifiers (PVGA)

For typical point-to-point radio links output power requirements are around 100-200mW. Such demands are best fitted to 0.25μm-gate length pseudomorphic HEMT technology such as the PH25-technology of UMS. Based on this process exhibiting a transition frequency of 80GHz and a specific power capability of 250mW per 1mm of gate periphery several medium power amplifiers have been designed for different Ka-Band applications. Following the customer demands for controllable output power the concept as already been presented for the DVGA has also been extended to such an PVGA.

Fig. 4 shows the layout for such a circuit consisting of the attenuator at the input being followed by a 4-stage amplifier. With respect to the output power requirements the last two stages are designed in a balanced configuration with the classical benefits of increased output power and optimized output return losses. The overall chip size is 4.5 mm^2. Measurement results for this circuit are presented in Fig. 5, indicating that this MMIC is designed for the well-known communication bands between 18GHz and 30GHz. A dynamic of more than 20dB is achieved.

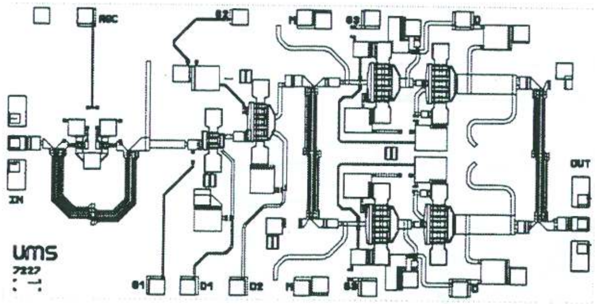

Figure 4: Layout of a four-stage Ka-Band PVGA based on 0.25µm P-HEMT (1.5mm x 3mm).

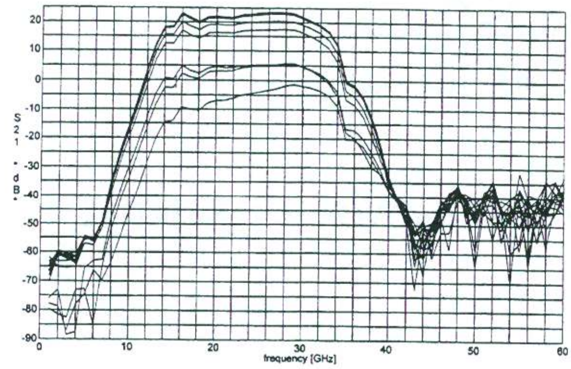

Figure 5: Measurement results for the controllable Ka-band power amplifier according to Fig. 4.

Compared to point-to-point communication applications the typical power demands for point-to-multipoint radios increase significantly. Typical values as requested today are in the range of 0.5-2 Watt. Following the market demands of minimum costs the design target of minimum chip-size requires the development and application of MMICs utilising a specific power P-HEMT technology. Such a process is available at UMS characterised by a typical power capability of 700mW/mm. Key features of this process named PPH25 are

- 0.25µm gate length
- double side doped channel
- double recess.

Typical measurement results for a 8x100µm transistor in this process are shown in Fig. 6. Output power, power added efficiency and gain have been measured at f=12GHz. With a drain voltage of 6V a PAE of more than 50% is achieved. In addition to these results it is worth noting that this process exhibits a transition frequency f_T = 65GHz and a breakdown voltage of more than 10V.

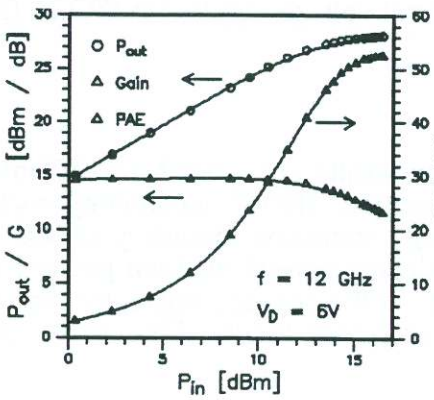

Figure 6: Power measurements applied to a PPH25-device with a gate width of 8*100 µm (f = 12GHz, V_D = 6V and V_{GS} = -0,15V).

Based on this process a 22-26GHz high power amplifier (HPA) has been developed. The design target has been to achieve a gain of 17dB and an output power of 0.5W. The layout of the circuit is shown in Fig. 7 reflecting the details of the architecture of the 2-stage design. The total chip-size is 7.7mm^2.

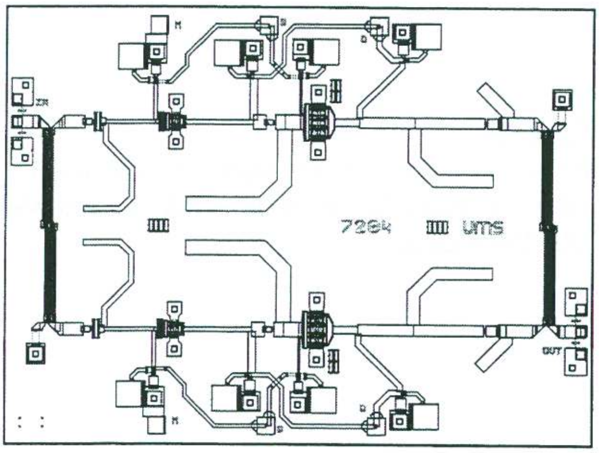

Figure 7: Layout of the 0.5W-amplifier for 22-26GHz point-to-multipoint communication.

The measurement results for this HPA are presented in the following.

Fig. 8a shows gain and return losses vs. frequencies indicating clearly that this circuit is designed and optimised for the demands coming from point-to-multipoint applications in the frequency range between 22GHz and 26GHz. A small signal gain of 17±1dB has been achieved. Input and output return losses are better than -16dB, thanks to the applied balanced concept. In addition Fig. 8b presents the measured results for the power performance of this MMIC. A 1dB compression point of P_{1dB} = 24dBm has been measured, accompanied by a saturated output power close 26dBm. Moreover, the measured results for the 3rd order intermodulation are also depicted in this diagram. This is due to the fact that the IP3 and IM3 are key specifications for minimised bit error rates (BERs) as required in such point-to multipoint communication links. The chip photo is shown in Fig. 8c.

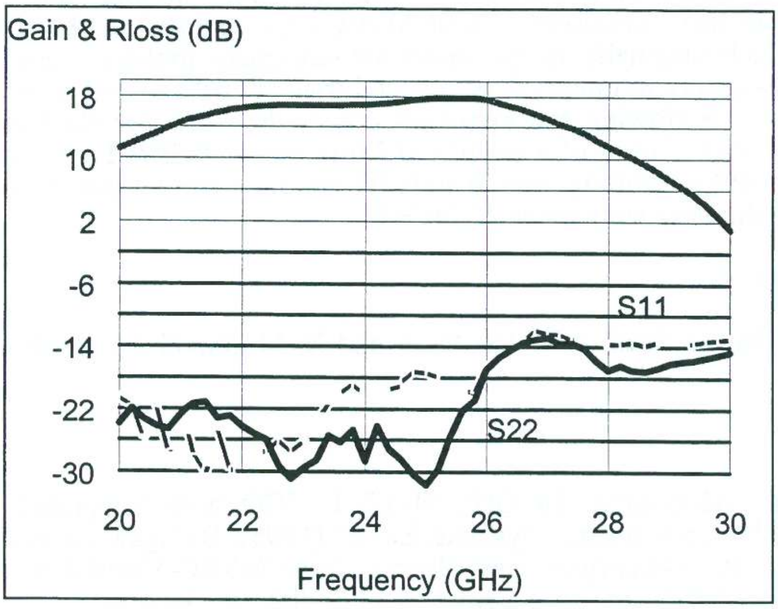

Figure 8a: Measurement results for the small signal performance of the HPA in PPH25-technology.

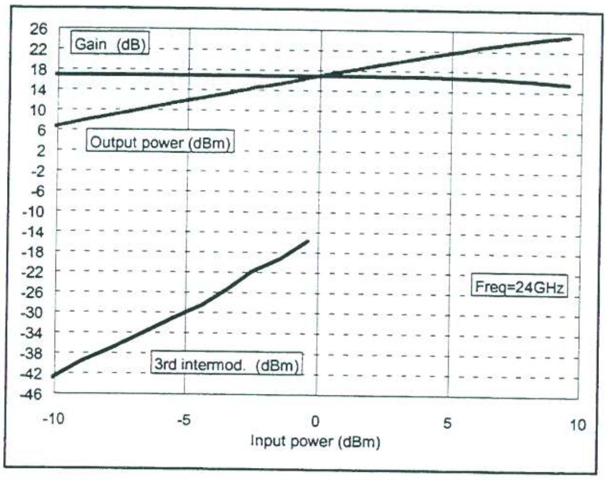

Figure 8b:
Measurement results for output power and 3[rd] order intermodulation of the HPA utilising the PPH25-process.

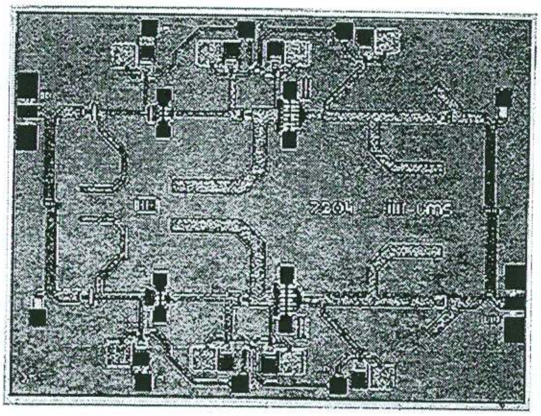

Figure 8c: Chip photo of the 22-26GHz HPA according to the layout as shown in Fig. 7. The MMIC has been realised in the PPH25-process of UMS resulting in a chip size of 7.7mm^2.

Conclusions

Several MMICs for applications from Ku- to Ka-Band point-to-point and point-to multipoint radios have been presented. Based on a specific attenuator concept, variable gain amplifiers for low and medium power have been discussed. These MMICs are realised in the same 0.25µm PHEMT process (PH25) which originally is optimised for extremely low-noise performance. Hence this demonstrates the feasibility to integrate receive and transmit path to end up with a one-chip "highly integrated front-end". Following the increased power demands for Ka-band point-to-multipoint communications the capabilities of a specific 0.25µm power PHEMT-process (PPH25) have been demonstrated by a HPA exhibiting more than 0.5W saturated output power and a 1dB compression point of 24dBm for the frequency range 22-26GHz.

Acknowledgements

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