Analysis of extrinsic element influence on the power performances of HEMT's in the Ka-Band

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Abstract

This paper provides an experimental microwave analysis of performance decrease of interdigitated HEMT's in millimeter wave range as the total gate width increases. The source inductance has been identified as the main reason of the power density decrease for large gate periphery devices. These behaviour has been checked by large signal measurements in Ka band.

Introduction

Solid state power amplifiers employing HEMT's provide a combination of electrical performance, reliability, small size and low cost superior to that of travelling wave tube technology. However for Ka band and upper, most of the results published to date have been obtained for small gate width, and hence output power levels have been relatively low. At our knowledge, the most higher development for power application is 1800 µm in Q band [1], but with very impressive technological sophistication, which cannot be easily developed in the frame of an industrial production.

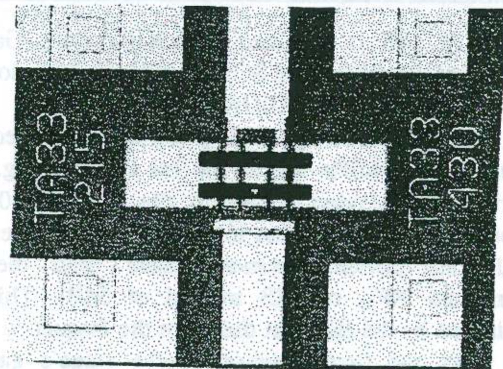
The power density decrease at high frequency is essentially due to the attenuation along each gate fingers [2], the phase variation between the different gate fingers and of course the ever-increasing influence of the parasitic effects.

We propose in this contribution to analyse very precisely the influence of parasitic effects on the power performances in Ka band, with a usual technology. In order to understand the main limitation and to find a good arrangement between power level and microwave performances. For all that, in a first time, an accurate extrinsic elements determination will be realised versus the total gate width. In a second time the devices performances will be determined and their evolutions will be linked with the extrinsic elements behaviour. Finally power measurements will be realised to confirm these previous investigations.

Device description

The devices used in this work are pseudomorphic 0.25 µm T shape gate heterostructure FET realised at THOMSON-TCS. The epilayer consists of a AlGaAs/InGaAs/GaAs heterojunction structure with a single doping plane in the AlGaAs layer ($\delta = 5.10^{12}$ atm cm^{-2}). Four unit gate width are studied (30, 50, 75 and 100 µm) with 2, 4, 6 and 8 gate fingers in parallel giving 16 different devices.

The different source pads are interconnected with air bridge and their grounding is realised with two via holes placed at each extremity of the device.
A single bridge is used when the unit gate width is 30 or 50 µm, and two parallel bridges when the unit gate width is 75 or 100 µm. Picture 1 is a photograph of a 4x75 µm device.



Picture 1: Presentation of a study device

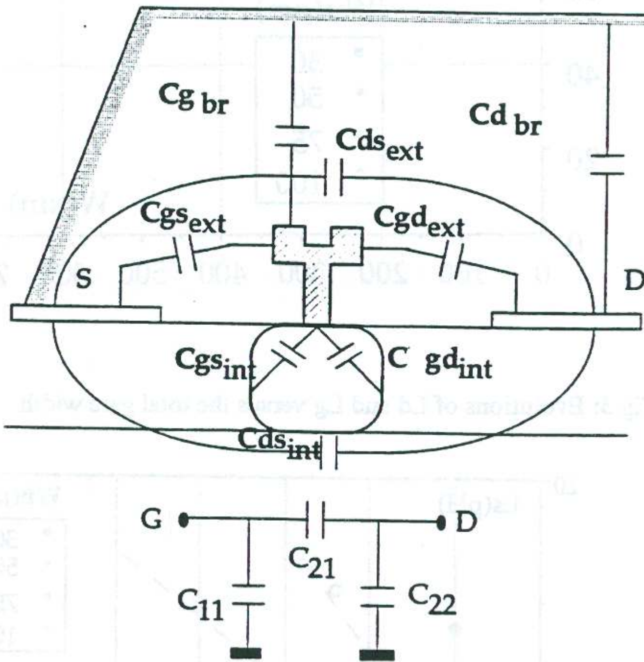
The main DC characteristics of the devices are a drain current density of 650 mA/mm at $V_{gs} = 0.5$ V, and a diode reverse breakdown voltage of 7.5 V at 1 mA/mm of gate current.

The extrinsic capacitances

The microwave characteristics of the devices were determined from S parameter measurements, performed with a HP 85107 network analyser and a Picoprobe system at frequencies from 1-40 GHz. These capacitances have been determined by using the classical Dambrine method [3]. The devices are biased at Vds = 0 V and Vgs < $V_{pinch\ off}$ (cold FET). In this condition, it is possible to consider the electrical equivalent scheme composed of three capacitances at low frequencies (under 20 GHz). These extrinsic capacitances could be located at different places of the device as shown in ("Fig. 1").

- Cgs_{ext} is the electrostatic capacitance between gate and source
- Cgd_{ext} is the electrostatic capacitance between gate and drain
- Cg_{br} is the electrostatic capacitance between bridge and gate
- Cd_{br} is the electrostatic capacitance between bridge and drain

- Cds_{ext} is the capacitance between drain and source, in the air and Cds_{int} is the residual capacitance in the semiconductor
- Cgd_{int} and Cgs_{int} are the residual gate/drain and gate/source capacitances in the semiconductor respectively
- Cpg and Cpd represent the access pads of gate and drain, and are not shown in "Fig. 1". They are included in the total extrinsic capacitances.



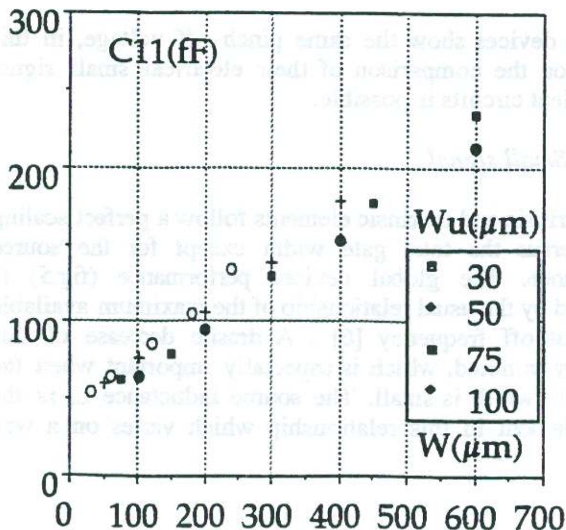
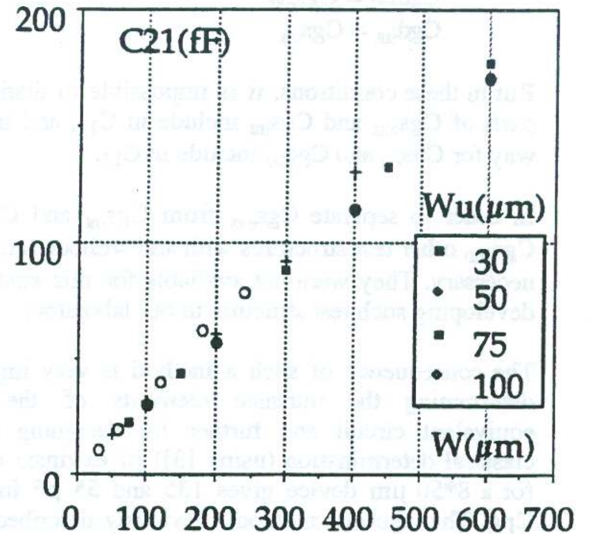


Fig1: Localisation of the extrinsic capacitances

All the capacitances are directly function of the total gate width, excepted Cpg and Cpd that are constant. It is more convenient to use a classical π-scheme with only three capacitances and the following equations can be written :

$$C_{11}(W) = Cpg + Cgs_{ext}(W) + Cgs_{int}(W) + Cg_{br}(W)$$
$$C_{12}(W) = C_{21}(W) = Cgd_{ext}(W) + Cgd_{int}(W)$$
$$C_{22}(W) = Cpd + Cds_{ext}(W) + Cds_{int}(W) + Cd_{br}(W)$$

The S-parameter measurements are transformed in [Y] parameters, "Fig. 2 " represents the capacitances C_{11}, C_{21} and C_{22} evolutions versus the total gate width.



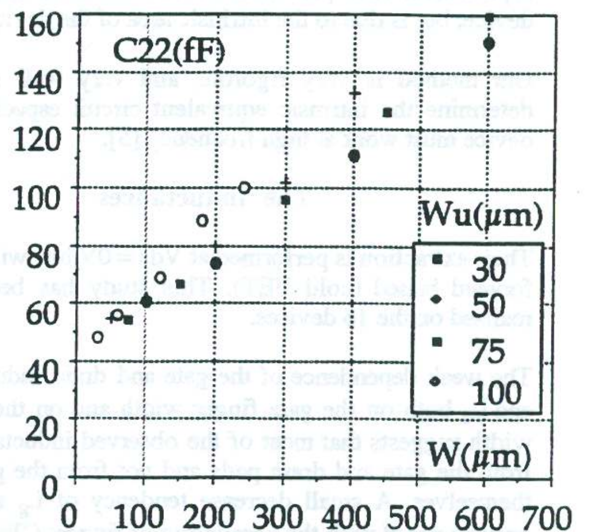


Fig 2: Evolution of the capacitances versus the total gate width

Cpd and Cpg can be immediately determined extrapolating C_{11} and C_{22} at W=0. The value of each pad is 45 fF. The two capacitances Cg_{br} and Cd_{br} can be neglected. The bridge is 6 µm high and it has been theoretically calculated that Cd_{br} = 0.6 fF/drain finger. This value is lower for Cg_{br} seeing that the facing areas are smaller. Moreover several studies have been realised in our lab with different bridge heights and widths. This allows us to note that C_{11} and C_{22} remain constant whatever the bridge width if the height is equal to 6 µm [4].

From previous considerations and from values of C_{11} and C_{21}, we obtain :

$$Cgd_{ext}(W) + Cgd_{int}(W) = Cgs_{ext}(W) + Cgs_{int}(W)$$

As the gate is centred in the recess, the two following equations are verified (SEM photograph of THOMSON):

$Cgd_{ext} = Cgs_{ext}$
$Cgd_{int} = Cgs_{int}$

But in these conditions, it is impossible to distinguish the parts of Cgs_{ext} and Cgs_{int} include in C_{11}, and in the same way for Cgs_{ext} and Cgd_{int} include in C_{12}.

In order to separate Cgs_{ext} from Cgs_{int} and Cgd_{ext} from Cgd_{int}, other test structures with and without active area are necessary. They were not available for this study. We are developing such test structure in our laboratory.

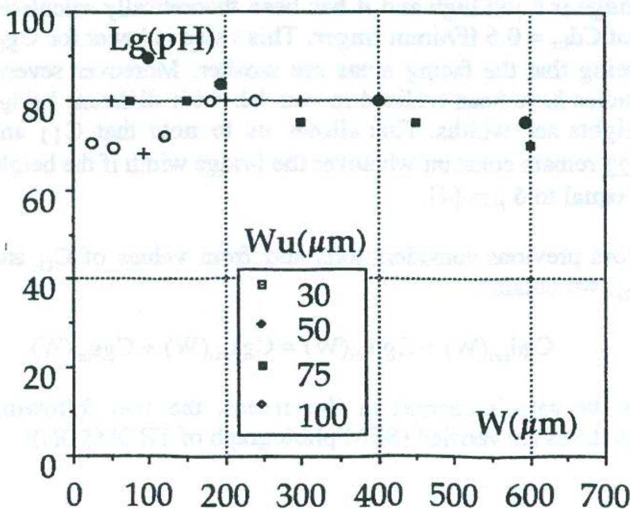
The consequence of such a method is very important for determining the intrinsic elements of the electrical equivalent circuit and further for designing MMIC. A classical determination (using [3]) of extrinsic capacitance for a 8*50 µm device gives 135 and 55 pF for Cpd and Cpg. The rigorous method (previously described) indicates that pads only have capacitances of 45 fF, and the remaining part must be considered as intrinsic-extrinsic capacitance. This part does not translate an access to the device, but is due to the intrinsic area of the device.

Our method is very rigorous and very well suitable to determine the intrinsic equivalent circuit especially if the device must work at high frequency [5].

The inductances

Their extraction is performed at Vds = 0V but with the gate forward biased (cold FET). This study has been equally realised on the 16 devices.

The weak dependence of the gate and drain inductances L_g and L_d both on the gate finger width and on the total gate width suggests that most of the observed inductance comes from the gate and drain pads and not from the gate fingers themselves. A small decrease tendency of L_g and L_d can only be noted with the paralleling of fingers ("Fig. 3"). The most important effect comes from the source inductance L_s. In this case, L_s varies nearly linearly versus the total gate width, with a slope which increases when the unit gate finger decreases ("Fig. 4"). This behaviour indicates that Ls has to be associated with the inductance presented by the air bridge ribbon and, in first approximation, is proportional to its total length. Even though the Ls value remains relatively small, its effect on microwave behaviour is not negligible, as we will see in the next part.



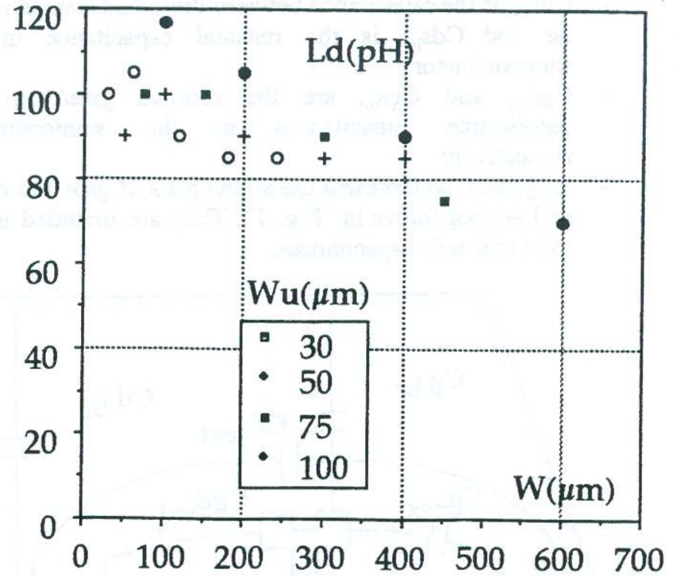


Fig 3: Evolutions of Ld and Lg versus the total gate width

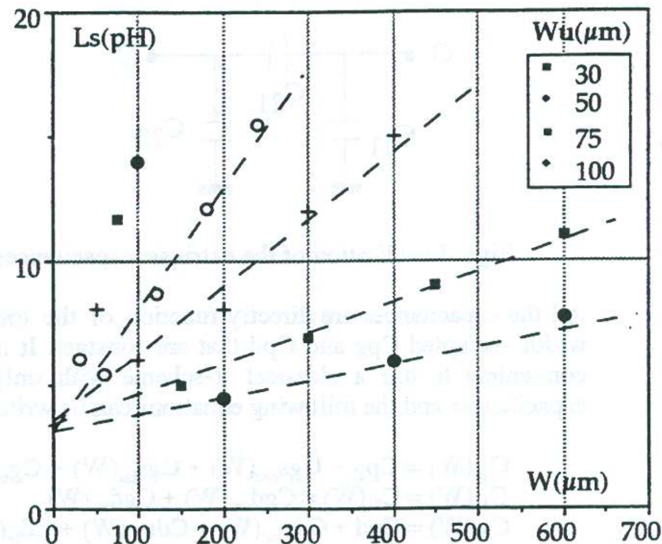


Fig 4: Evolution of Ls versus the total gate width

Device performances

All the devices show the same pinch off voltage, in this condition the comparison of their electrical small signal equivalent circuits is possible.

A. *Small signal*

The intrinsic and extrinsic elements follow a perfect scaling rule versus the total gate width except for the source inductance. The global devices performance (fig.5) is deduced by the usual relationship of the maximum available gain cut off frequency [6] . A drastic decrease of this quantity is noted, which is especially important when the unit gate width is small. The source inductance L_s is the only element in this relationship which varies on a way

opposite to the normal scaling rule. The decrease of Fmag is likely to be due to this element.

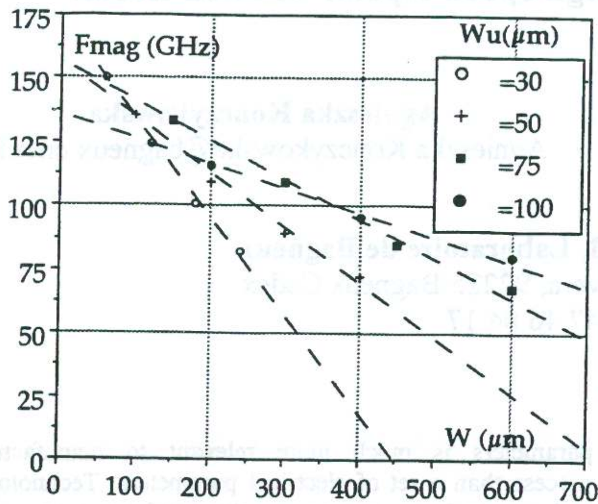


Fig 5: Evolution of the MAG versus the total gate width

B. Large signal

Large signal measurements have been performed at 30 GHz with an active load pull bench [7] in order to confirm previous observation in small signal.

Total gate width	Gain (dB)
2*50 μm	6.8
4*50 μm	6.3
8*50 μm	4.3

Table I

All the devices with a unit gate width of 50 μm have been measured. How we could expect (Tab 1) the power gain decreases (losses of 2 dB between a two and a eight fingers) when the number of fingers increases.

Conclusion

The influence of the source air bridge inductance has been analysed. It is clear that high development require to take into account very accurately this effect.

Moreover an accurate determination of the pad capacitance has been presented, which is very important for determining the intrinsic elements and further for designing MMICs, essentially if the operating frequency is high.

Acknowledgements

The authors would like to thank THOMSON TCS for providing the devices. This work has been supported by a European contract.

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