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Modified Kogge-Stone VLSI adder architecture for GaAs technology

Andrew Beaumont-Smith and Neil Burgess

Centre for GaAs VLSI Technology,
University of Adelaide,
Adelaide SA 5005
AUSTRALIA

Abstract

This paper describes a new VLSI adder architecture well-suited to digital GaAs VLSI technology. The architecture uses a relatively small amount of transistors while achieving very high speed. Simulation results indicate that in a 0.6μm E/D MESFET GaAs VLSI technology, a 32-bit addition would take less than 1ns with a power consumption of 280mW.

Introduction

VLSI adders in both silicon and gallium arsenide VLSI technologies constitute critically important elements in most digital integrated circuits. Almost invariably the requirement of the adder is that it is primarily fast and secondarily efficient in terms of transistor usage, power consumption, and chip area. Transistor packing density of gallium arsenide VLSI technology is lower than in silicon (5000 MESFET/mm^2 vs 10000 MOSFET/mm^2 for 0.6μm linewidths) and so the issue of efficiency is more significant for GaAs, given its raw speed advantage over silicon. GaAs VLSI technology does not permit dynamic logic design techniques such as the Manchester carry chain, widely used to accelerate silicon VLSI adders. Also, the main GaAs VLSI logic family - Direct-Coupled FET Logic (DCFL) - is particularly sensitive to fan-out loading of both gates and interconnect. Hence, the ideal GaAs VLSI adder should have low fan-out, short interconnecting wires, and yet achieve very high speed. The adder architecture presented in this paper meets all these criteria and illustrates that designing to a technology's strengths (and away from its weaknesses) leads to near-optimal solutions.

GaAs architectures for addition

Sarmiento et al [1] examined a variety of adder architectures from the perspective of GaAs VLSI implementation. They concluded that the Brent-Kung adder [2] is particularly suited to GaAs VLSI implementation owing to its low fan-out demands. However, there are some lengthy wires in the Brent-Kung adder, and a relatively large number of cell delays from input to output. The Kogge-Stone architecture (Fig. 1) replicates the Brent-Kung adder's most significant carry bit's binary tree for all the carry signals, thus reducing the number of cell delays between input and output but at the expense of many cells and lengthy interconnects. Han and Carlson [3] and Kowalczuk et al [4] have proposed alternatives to the Kogge-Stone adder that reduce the number of cells and the length of the interconnects at the expense of an extra cell delay. The Han-Carlson adder implements alternate columns of the Kogge-Stone adder ("radix-4 Kogge-Stone") with an extra row of cells to compute the odd-numbered carries from the even numbered carries (Fig. 2). Kowalczuk's adder quarters the lengths of the longest wires through a high-radix ripple scheme (Fig. 3). A simple combination of the two schemes leads to an architecture that has two more cell delays on the critical path than the Kogge-Stone adder (Fig. 4). Our architecture (Fig. 5) regains one cell delay by inserting four extra black cells at the m.s.b. end of the adder. A carry input has also been accommodated. This architecture has a low number of cell delays from input to output and relatively short interconnecting wires on the adder's critical paths. The number of cells is considerably reduced from 192 in the Kogge-Stone adder to 143, representing a saving of 25% in both area and power consumption.

Physical design

There are two aspects of the physical design that warrant discussion: the adder's layout, and the cells' design. The physical layout of the adder shown in Fig. 6 closely follows the schematic illustration of Fig. 5. The lengths of wires across the adder have been minimised by the combination of the Han-Carlson and Kowalczuk techniques so that they constitute equivalent fan-outs of less than 2 gates. (The wires travelling down the adder from the "p&g" cells to the bottom row of "grey" cells actually constitute fan-outs of over 3 gates.) A small number of buffers, consisting of a pair of DCFL inverters and indicated by triangles in Fig. 5, were included to reduce the fan-out loads along the critical path of the adder.

The four cells used in the adder implement the following logic expressions: the "p&g" cell implements $p_i = a_i \vee b_i$ ("carry propagate"), $g_i = a_i \wedge b_i$ ("carry generate"), and $h_i = a_i \oplus b_i$; the "black" cell implements $P_i^j = P_i^k \wedge P_{k-1}^j$ ("carry propagates from column j to column i") and $G_i^j = G_i^k \vee (P_i^k \wedge G_{k-1}^j)$ ("carry generated in column j propagates to column i"); the "grey" cell implements $G_i^j = G_i^k \vee (P_i^k \wedge G_{k-1}^j) = c_i$; the "sum" cell implements $c_{i-1} \oplus h_i = s_i$, the i^{th} sum output. In GaAs VLSI technology, only inverters, 2- and 3-input NOR gates, and wired-OR functions are available as high-speed primitives [1]. The four cell types were each designed using these gate primitives, which were sized for low power consumption. However, selected "p&g" and "grey" cells (identified in Fig. 5 by outline rings) were designed with SDCFL wired-OR outputs owing to their relatively large fan-outs.

Simulation results

The 32-bit adder was simulated in Vitesse's 0.6μm HGaAsIII VLSI technology using HSPICE. The delay of the adder in typical conditions was 980ps at 75°C. The adder has 1809 MESFET's in an area of 504μm × 596μm, achieving a density of 6022 MESFET's/mm^2. The power consumption was 280mW, giving merit figures of 0.27 mW/MHz and 0.39 μW/MHz/gate, only twice that of a recent 0.3μm BiCMOS 32-bit adder [6]. Our adder was submitted for fabrication earlier this year.

References

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[3] P.M. Kogge and H.S. Stone, "A parallel algorithm for the efficient solution of a general class of recurrence equations", *IEEE Transactions on Computers*, vol. 22, pp. 786-793, August 1973

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[5] T. Han and D.A. Carlson, "Fast area-efficient VLSI adders", Proc. 8th Symposium on Computer Arithmetic, pp. 49-56, Como, September 1987

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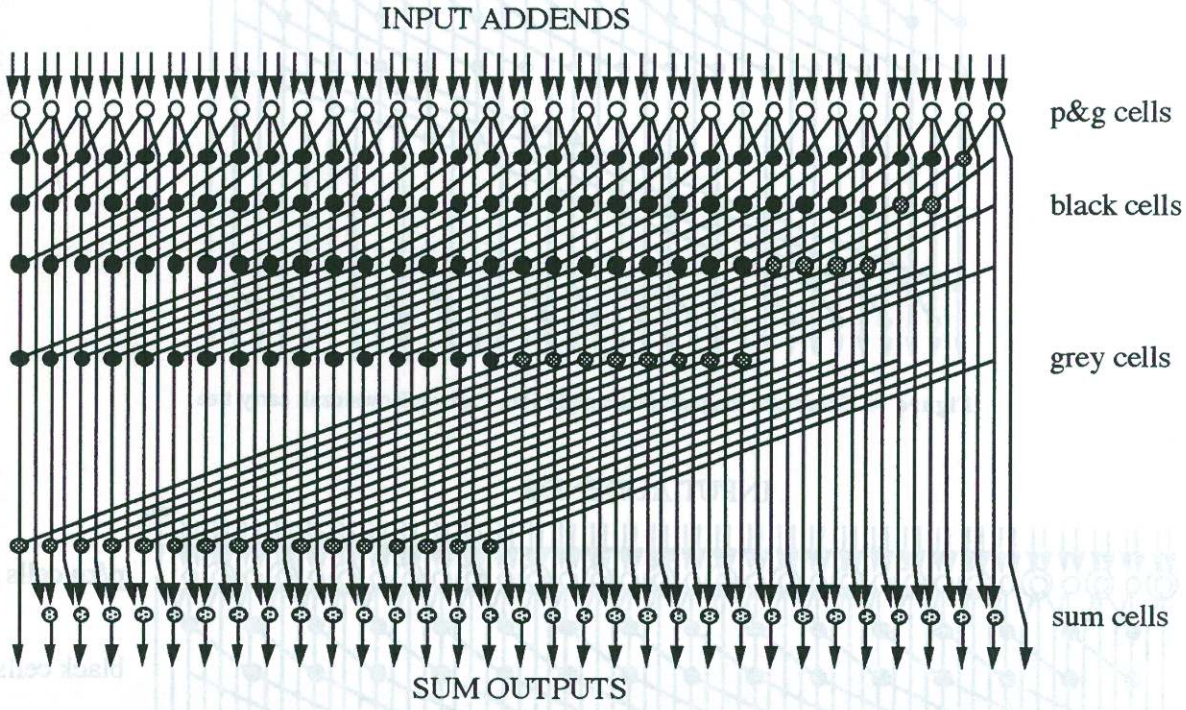

Figure 1 Schematic diagram of the 32-bit Kogge-Stone adder

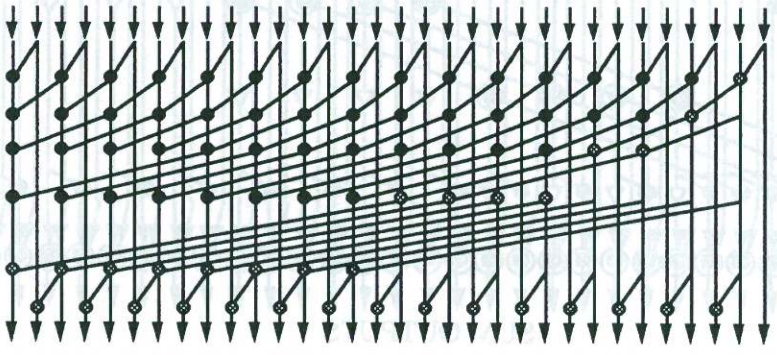

Figure 2 Schematic diagram of the Han-Carlson carry tree

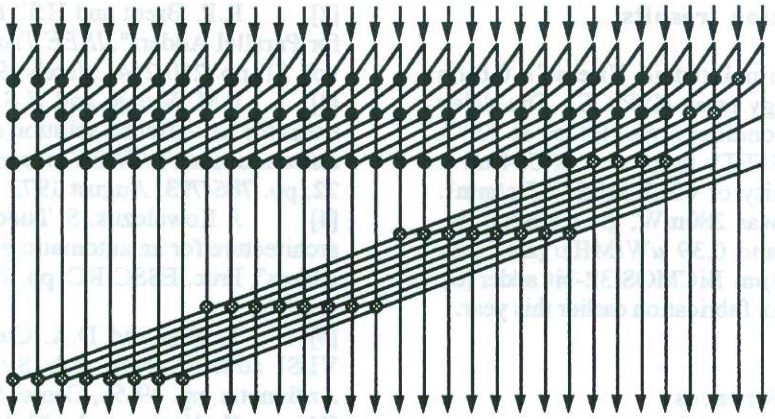

Figure 3 Schematic diagram of a Kowalczuk carry tree

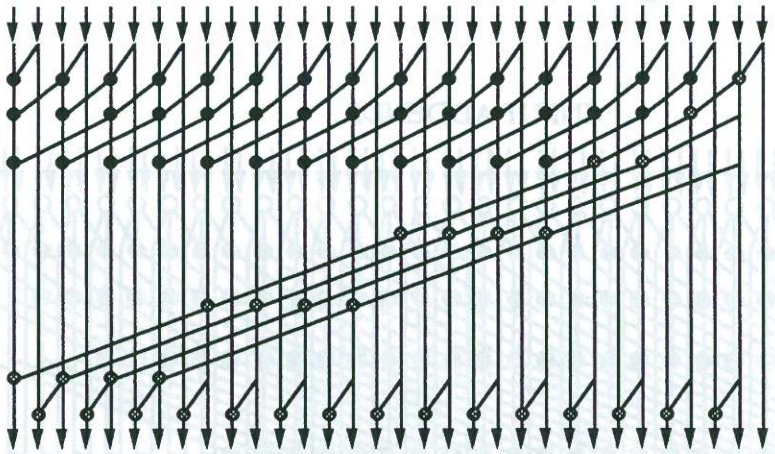

Figure 4 Schematic diagram of a simple Han-Carlson/Kowalczuk carry tree

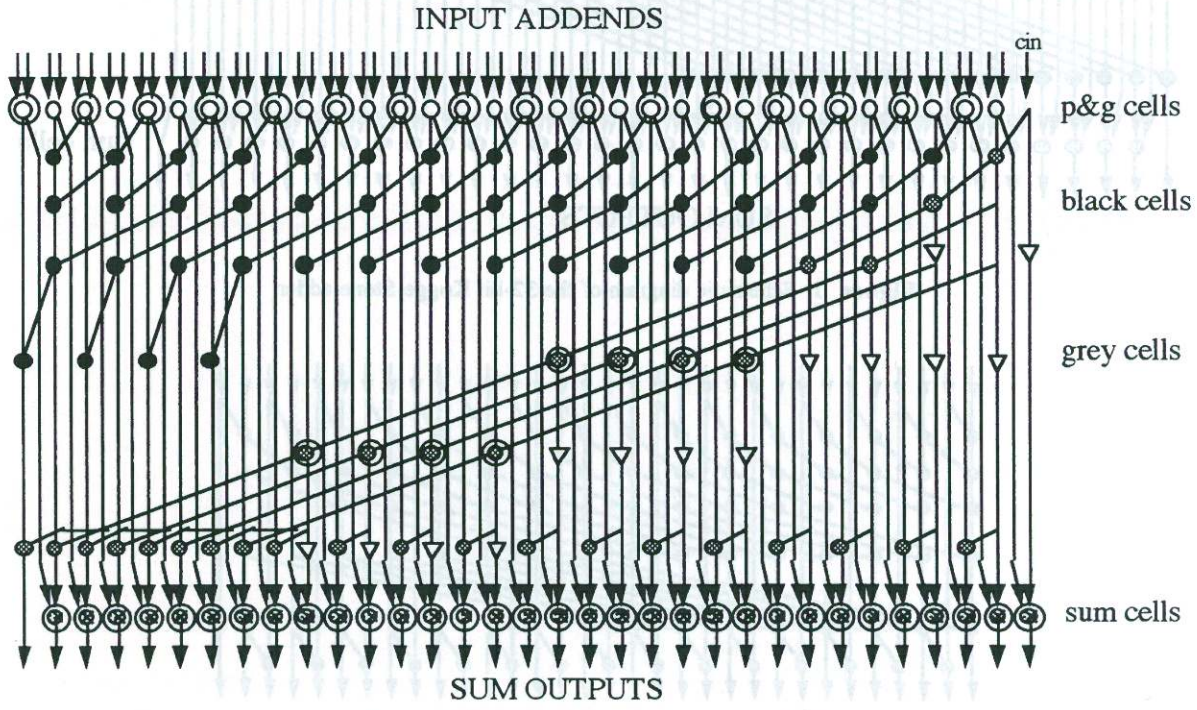

Figure 5 Schematic diagram of proposed adder

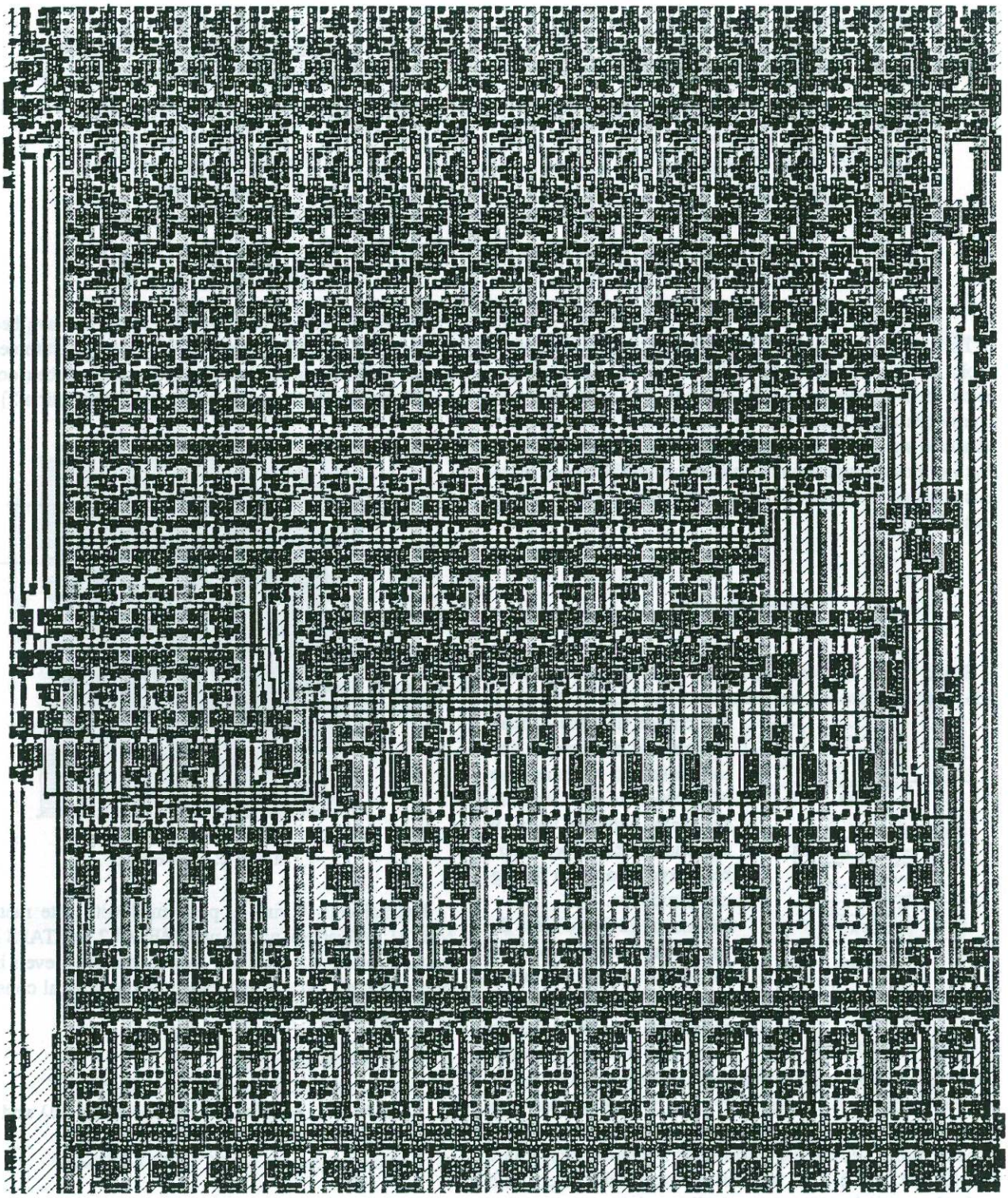

Figure 6 Layout of proposed adder