# A 2ns/660mW GaAs 5Kbit ROM using Low Leakage Current FET Circuit (L2FC)

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*Abstract*— **In this paper, a 5Kbit ROM is presented using a primitive-cell architecture based on a compensation technique, named *Low Leakage Current FET Circuit (L2FC)*, whose main advantage relies on the fact that it has an extremely low noise margin sensitivity with fan-in compared with *Direct Coupled FET Logic (DCFL)*. This characteristic is found to be the key factor when implementing GaAs ROMs because of its degradation as the number of word lines is increased. The performance obtained using this structure demonstrates the effectivenes of this technique and its significant improvement on noise margin increase.**

## I. Introduction

Today's DSP and communication circuits manufacturers are demanding memories of ever decreasing cycle times, combined with the flexibility afforded by input and output latches and internal write–pulse generation. To meet stringent requirements in a competitive industry, GaAs offers an alternative to Silicon (Si). However, placing embedded GaAs memories on chip is crucial in many applications in order to avoid the restrictions imposed by chip-to-chip delays occuring when the memory is in a separate package. Up to now, most of the papers that have been published refering to GaAs ROMs show very high speed circuit performance, but they are based on new processes developed specifically for memory design [1], [2], [3]. These processes impose separate chips for the memory thus introducing off-chip delays in the systems, limiting the operating bandwidth. The implementation of GaAs memories using conventional process technologies would allow to overcome these disadvantages. However, a conventional GaAs process presents some problems, mainly due to its leaky characteristics, and the small output logic swing, in the order of 0.6V. In this paper, a 5Kbit ROM using a conventional H-GaAs II process from Vitesse Semiconductor Corp. is presented. The memory contains 30.000 transistors in an area of 1.5mm by 3.5mm, thus resulting in a density of 5700 $ttor/mm^2$. The results obtained from simulations give an access time in the order of 2ns and a power consumption of 660mW at 25°$C$. The circuit was packaged in a 132 Pin Ceramic LDCC, and is being tested currently.

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## II. Direct Coupled FET Logic (DCFL)

Direct Coupled FET Logic (DCFL), the most compact logic family in GaAs, is highly suited for high performance VLSI systems. This type of logic family resembles nMOS logic in Silicon, using a D–MESFET transistor as an active load and E–MESFETs to implement the logic functions [4], [5], [6]. DCFL is a ratio logic family, which means the introduction of a dimensioning factor, $\beta$, defined as

$$\beta = \frac{(W/L)_{pull-down}}{(W/L)_{pull-up}} \quad (1)$$

in order to obtain satisfactory logic levels and noise margin at different process spread. For the case of H–GaAs II technology, it is convenient to use $\beta$ equal to 10 for commercial temperatures and 14 for military temperatures [7].

### A. Temperature effects

The design of ROMs using GaAs MESFET DCFL is a challenging task due to the deterioration of logic voltage swing. As the temperature increases, the characteristics of the GaAs MESFET also change as it is shown in Figure 1 for the case of an inverter.

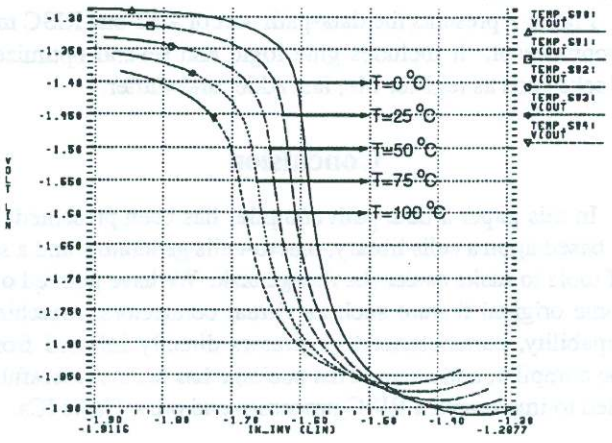


FIG. 1: Effect of temperature in logic swing

As the temperature rises, the high level of the output signal falls, the low level rises, and the transient region from *high* level to *low* level stretches. Therefore, the signal voltage swing becomes small and the transient slope from *high* level to *low* level smooth. The smaller signal voltage swing and the gentler transient slope lead to the decrease of the noise margin. The degradation of the inverter characteristics by the increase of the temperature is a physical phenomenon and there is no means to prevent the degradation. This is one of the most important problems in using E/D–DCFL for memory circuit at high temperature.

### *B. Leakage current*

The sub–threshold leakage current of the GaAs MESFET is five to six orders of magnitude larger than that of the Si MOSFET. Therefore, the sub–threshold leakage current easily dominates circuit operation. As an example, the graphical representation of drain–to–source current, $I_{DS}$, versus gate–to–source voltage, $V_{GS}$, for different values of drain-to-source voltage, $V_{GS}$, is shown in Figure 2 for the case of an E–MESFET with $10\mu m$ width and $1.2\mu m$ legth.

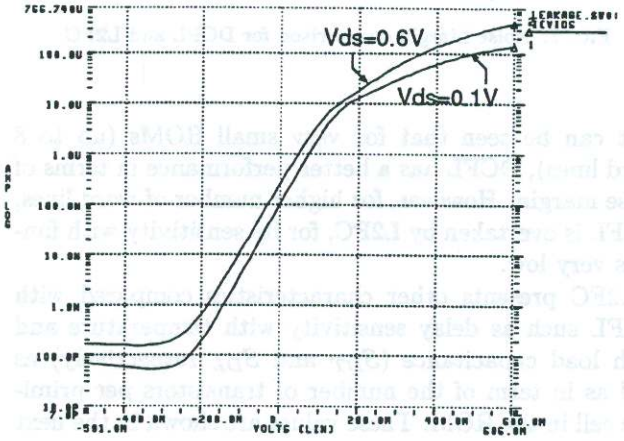


FIG. 2: $I_D - V_{GS}$ characteristics for an E–MESFET at $25°C$

Basically a ROM matrix consists of NOR gates with high fan–in, that corresponds to the number of word lines. In such a structure only one transistor is in conduction at any one time while the remaining MESFETs at the input are cut–off. Thus the influence of the sub–threshold currents for this type of architectures is apparent as the number of word lines is increased. This is shown in Figure 3, where $N$ represents the number of transistors contributing to the total leakage current, thus $N+1$ representing the number of word lines in the core.

It can be seen that it is possible to implement DCFL NOR gates with up to 8 inputs. However, when we increase the number of inputs to 16 no switching is produced, because the total leakage current is so huge that the high logic level is degraded, reducing significantly the noise margin.

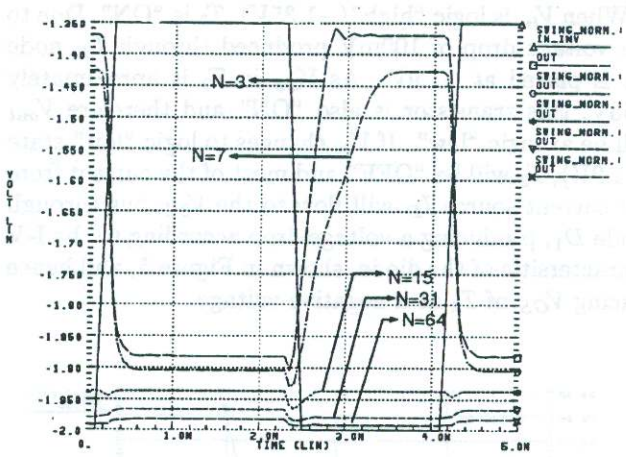


FIG. 3: Logic swing variations versus fan–in $(N+1)$ for NOR gates

## III. LOW LEAKAGE CURRENT FET CIRCUIT (L2FC)

Low Leakage Current FET Circuit (L2FC) presents, as its main advantage, a low Noise Margin sensitivity with fan–in [8]. It is based on placing the input transistors with such a low $V_{GS}$ when they are in cut–off region, that leakage currents are almost negligible. As it was shown in Figure 2, for the gate–to–source voltage, $V_{GS}$, below the threshold voltage, $V_T$ (210mV for E–MESFET in H–GaAs II process), a current in the order of a few $\mu A$ continues to flow. If the MESFET is operated with negative values for $V_{GS}$ instead of positive values, it becomes possible to significantly reduce the leakage currents. The structure to produce such situation is shown in Figure 4.

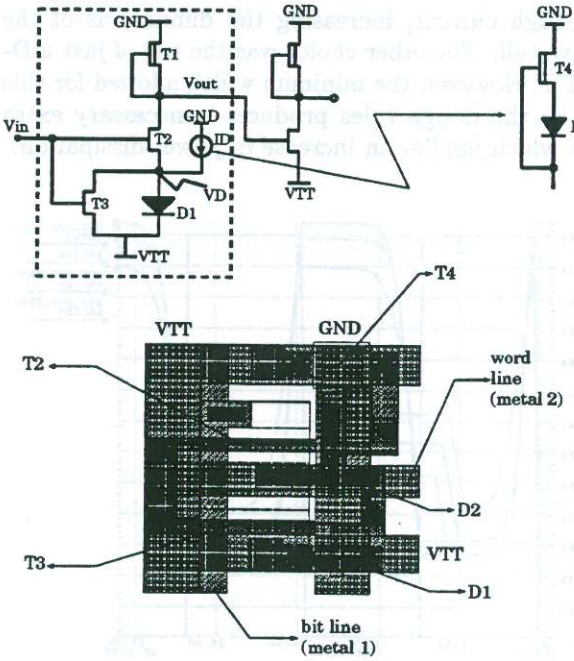


FIG. 4: L2FC inverter and layout

When $V_{in}$ is logic "high" ($-1.35V$), $T_3$ is "ON". Due to the voltage drop of 100mV produced through $T_3$, node $V_D$ is placed at $-1.9V$. As $V_{GS}$ in $T_2$ is aproximately 0.55V, this transistor is also "ON" and therefore $V_{out}$ will be at logic "low". If $V_{in}$ changes to logic "low" state ($-1.9V$), $T_3$ will be "OFF" and most of the current from the current source $I_D$ will flow to the $V_{TT}$ bus through diode $D_1$, producing a voltage drop according to the I-V charactersitic of the diode, shown in Figure 5, and hence placing $V_{GS}$ of $T_2$ at a negative voltage.

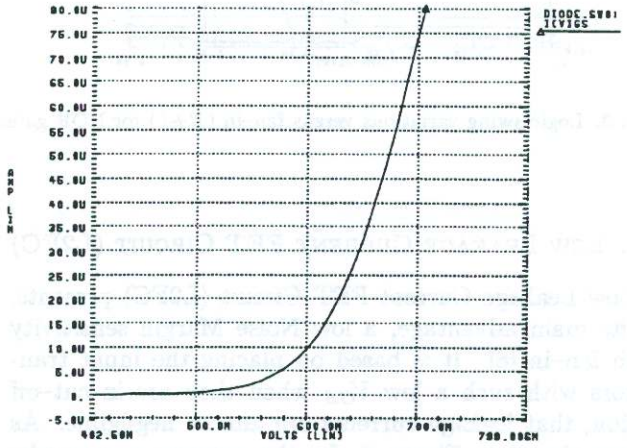

FIG. 5: I-V characteristic for diode $D_1$

As it was shown in Figure 4, a structure implemented by a D-MESFET, $T_4$, and a diode, $D_2$, has been used for the current source in order to produce the voltage drop in diode $D_1$ with a good area-power tradeoff. If an E-MESFET were used, its width should be large to give enough current, increasing the dimensions of the primitive cell. The other choice was the use of just a D-MESFET. However, the minimun width allowed for this device by the design rules produces unnecessary extra current which implies an increase in power dissipation.

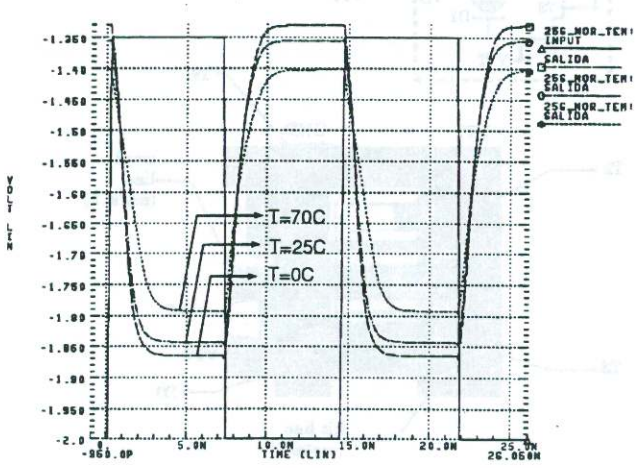


FIG. 6: 256 inputs L2FC NOR gate

With all these considerations, ROMs with up to 256 word lines can be implemented with good logic levels in a range of temperature from $0°C$ to $70°C$ as shown in Figure 6.

## IV. Comparison and Results

A comparison in terms of noise margin sensitivity with fan-in is shown in Figure 7 for the case of DCFL and L2FC.

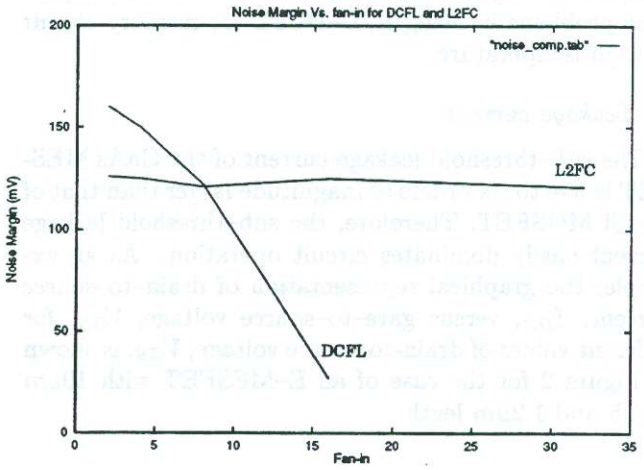


FIG. 7: Noise Margin comparison for DCFL and L2FC

It can be seen that for very small ROMs (up to 8 word lines), DCFL has a better performance in terms of noise margin. However, for higher number of word lines, DCFL is overtaken by L2FC, for its sensitivity with fan-in is very low.

L2FC presents other characteristics compared with DCFL such as delay sensitivity with temperature and with load capacitance ($S_{DT}$ and $S_{DL}$ respectively) as well as in term of the number of transistors per primitive cell in the ROM. These values are shown in the next table.

| Performance | DCFL | L2FC | Units |
|---|---|---|---|
| $S_{DT}$ | $-0.8$ | $-0.4$ | ps/$°C$ |
| $S_{DL}$ | 0.7 | 1.7 | ps/fF |
| Trans. per cell | 1 | 5 | transistors |

Clearly, the drawbacks of L2FC are its high delay sensitivity with load capacitance (which is directly related with the length of the bit line and hence with the storage capacity of the memory) and the number of transistors used to implement the primitive cell. In order to overcome both problems, much care was put on optimising the layout of the primitive cell, giving as result an area of $25 \times 23\mu m^2$.

Taking into account all these considerations, a 5Kbit ROM was implemented using L2FC and H-GaAs II process ($0.8\mu m$) for its inclusion as part of a CORDIC processor designed by our group [9]. The ROM was divided

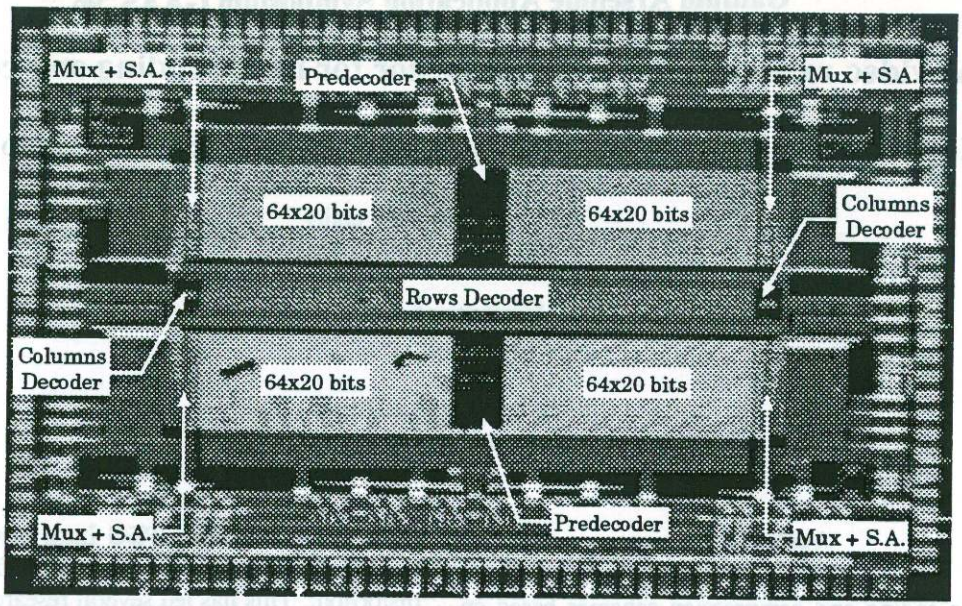


FIG. 8: Microphotograph of the 5Kbit ROM

in four $64 \times 20$ blocks extracting 5 bits from each one using multiplexing blocks at the outputs. Thus, the global organization of this ROM is $256 \times 20$ bits. Figure 8 shows a microphotograph of this memory.

HSPICE results obtained for this 5Kbit memory are shown in the table below.

| Temp. ($^\circ C$) | Delay (ns) | Power (mW) | $\frac{mW}{bit}$ | No. ttors. | $\frac{ttors}{mm^2}$ | $\frac{bits}{mm^2}$ |
|---|---|---|---|---|---|---|
| 0 | 2.2 | 560 | 110 | | | |
| 25 | 2.1 | 660 | 130 | 30K | 5700 | 1000 |
| 70 | 2.0 | 920 | 180 | | | |

## V. CONCLUSIONS

The performance of a high speed processor depends greatly on how fast data are sent and obtained from memory. Although GaAs technology is found to be a good choice in order to get the bandwidth requirements needed by current and future processors, it is evident the need of implementing embedded memories to overcome the off-chip interconnect delay penalty. However, because of the high leakage current produced in these devices and its temperature dependance, much care has to be taken in order to get good performance. The solution presented in this paper is based on biasing gate-to-source voltage in the E-MESFETs so that its value is placed in a negative range when the transistor is OFF, thus decreasing sub-threshold leakage current. With this technique, a $0^\circ C$ to $70^\circ C$ fully operative 5Kbit ROM has been implemented. Simulation results show access time in the order of 2ns with power consumption below 1W. These results demonstrate how using a conventional GaAs process technology, the implementation of embedded memories is possible.

## ACKNOWLEDGMENTS

The contributions provided by R. Esper-Chain, F. Tobajas and L. Hernández of the *Centre for Applied Microelectronics* are very much appreciated. This work has been partially funded by *GARDEN: Gallium Arsenide Reliable Design Environment* (CT93–0385) from the European Community.

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