A Low-Power Differential Cross-Coupled FET Logic for GaAs Asynchronous Design

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Abstract

This paper describes a new GaAs MESFET structure, named Differential Cross-Coupled FET Logic - DC²FL, which is compatible with DCFL, DPTL and DCVS circuits. It can be efficiently used in delay-insensitive asynchronous circuits and self-timed rings, as well as in synchronous ones. When combined with the mentioned differential structures it offers attractive power savings without performance degradation. As an example, a fully functional 8-bit ripple carry adder has been designed and fabricated, verifying the expected very low power dissipation during the standby state.

Introduction

Gallium Arsenide (GaAs) has been for a long time presented as the future state-of-the-art IC technology for very high-speed VLSI systems. However, GaAs have some drawbacks for synchronous digital circuits. Large static power dissipation, clock skew and signal synchronization are the main problems to be solved when both the operation speed and the design complexity are increased. Since asynchronous circuits do not require any clock to control state changes, they have no skew and signal synchronization problem [1]. Self-timed differential structures has been proposed as a way to avoid the discussed troubles [2,3].

Moreover, the use of handshake protocol in asynchronous design makes it run as fast as possible, giving automatic adaptation to physical variations, average-case instead of the worst-case performance, and easier design migration thanks to a simpler timing [4]. Besides, MESFET differential structures [5,6,7,8] allows to design gates with a larger number of inputs thus dissipating less power per logic function.

In this paper, a novel DC²FL low-power differential MESFET logic structure is proposed. This configuration mixes several features of previously known techniques, achieving a power-delay product lower than DCFL gates and comparable to the DCVS ones. Additionally, it can be also used to reduce the static power consumption of asynchronous circuits during the standby state, showing further significant advantages when applied to built self-timed rings [9].

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A fully functional 8-bit ripple carry adder was designed with the Vitesse GaAs III technology [10] and a 2V power-supply voltage. The structure is totally compatible with DCFL, DPTL and DCVS topologies.

Basic Structure

Unlike most of the previously published precharged differential structures [6,7,8], DC²FL is based on predischarging internal nodes. The basic structure is illustrated in Fig. 1. A tree of EFET transistors and its dual tree are connected to two internal nodes *a* and *b* which are required for delay-insensitive asynchronous applications. When *fi* goes high (*fin* is low) the predischarge phase starts and both internal nodes are discharged through the M2 and M3 transistors, while M1 isolates the logic tree from the supply voltage, so no significant currents flow into the EFET logic trees.

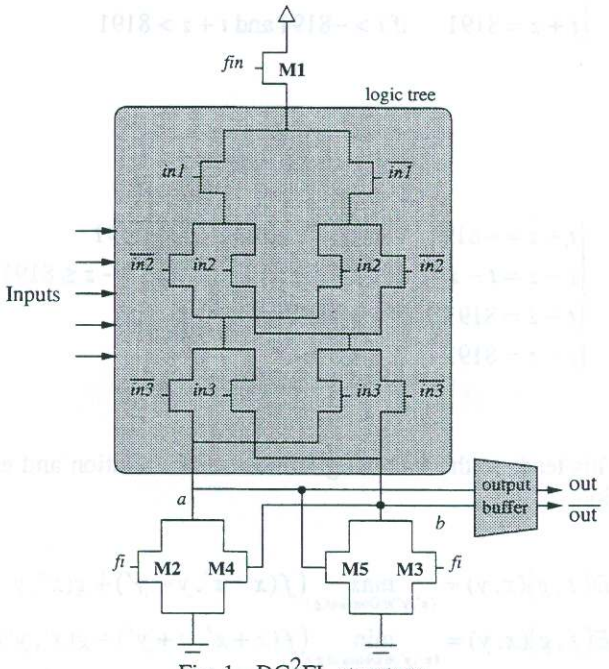

Fig. 1 - DC²FL structure.

Then, during the evaluation phase (*fi* is low, *fin* goes high), either the node *a* or the node *b* is charged up to 0.6V according to the tree connection and the input values. The cross-coupled transistors M4 and M5 connected to the internal nodes provide a positive feedback draining charge leakage on the uncharged internal node to the ground during the evaluation phase and switching rapidly as soon as a small voltage

difference is sensed. The internal nodes voltage levels are then buffered by the output stage (Fig. 1), offering a suitable fanout capacity.

The two predischarge transistors M2 and M3, as well as the cross-coupled ones M4 and M5 can be made as small as possible since their size do not affect the global performance. The M1 transistor size is similar to the logic trees transistors because the number of EFET devices involved in the logic part define the current used to charge the respective internal node. So, as can be seen in Fig. 2, the logic tree transistors size (W) is a compromise between the charging delay (td) responsible for the speed performance, and the current flow through the tree (I), that contributes to the power dissipation. The analysis was done on an inverter and a disjunction (Fig. 1), but it can be extended to more complex gates.

A constraint of this approach, like for DPTL and DCVS techniques, is that the high input voltages must be restricted (Vin < 0.7V) to prevent the forward biasing of the MESFET Schottky barrier in the DC^{2}FL tree transistors. This constraints about the output stage are discussed in the next section.

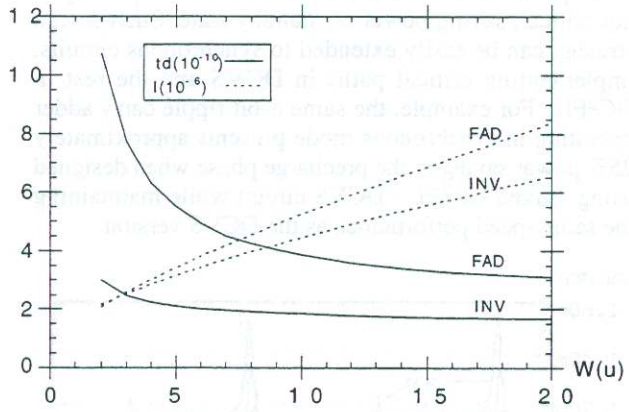

Fig. 2 - Variation of charging delay (td) and current consumption (I) vs. tree transistor width.

Output Stage

The output stage consists of a buffer that regenerates the internal voltage levels, providing a good fanout and noise margin. Moreover, it must be a no inverting circuit, because these outputs can be connected to either a similar next stage or a DCVS one [8] and they have to be low during the predischarge phase for the proper operation of these circuits. Furthermore, this output stage must limit the output high voltage to 0.7V in order to comply with the input voltage requirements of the next stage. The evident solution of merely cascading two DCFL inverters for each output is unsuitable due to the significant power dissipation of this approach.

A new and ad-hoc output circuit to achieve low consumption during the standby state is proposed. The circuit is shown in Fig. 3 and consists of a pullup NOR gate configuration, a SBFL inverter and a NOR SR latch implemented with Power Rail technique [11]. The NOR gate detects when either *a* or *b* node is charged to more than approximately 0.2V, and generates a signal which buffered through the SBFL inverter supplies the power to the SR latch. The latch senses small voltage differences in the nodes *a* and *b*, like a DPTL buffer [5], switching rapidly and providing the appropriated voltage levels 0.1V and 0.7V.

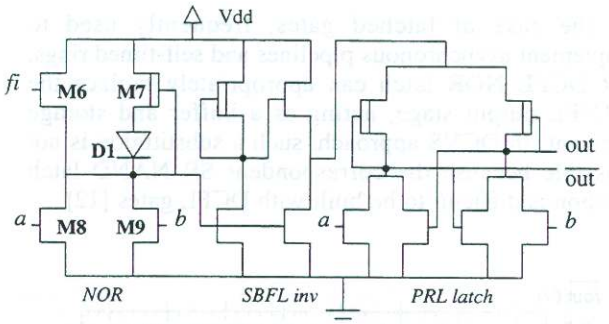

Fig. 3 - Output stage schematic.

The pullup NOR output is raised up at 0.6V by *fi* signal during the predischarge phase. The logic tree input variables may not be ready or even *a* or *b* nodes not be properly charged when the evaluation phase is started. This would discharge the output NOR leading to a malfunctioning of the circuit. So a weak pullup current source (M7 and D1) is used to compensate the subthreshold currents through M8 and M9 transistors. Such a configuration keeps the NOR output voltage at approximately 0.6V.

This weak current source must provide a current equivalent to the M8 and M9 subthreshold currents (I_{sub}) plus the SBFL inverter gate currents (I_{Sh}). Both currents depend on the transistor sizes and their biasing voltages. So, $I_{M7\text{-}D1} \geq 2.I_{sub} + 2.I_{Sh}$ condition must be satisfied. However, with the NOR output at 0.6V, I_{Sh} is much lower than I_{sub} and can be neglected. Furthermore, the M7 transistor is always operating in saturation region, then [12]:

$$\beta_7(V_{gs}-V_T)^2 tanh(\alpha V_{ds}) \geq C1.W_8.no(1- e^{-U_{ds}})/L_8 \quad (1)$$

where

no = equilibrium minority carrier concentration;

$C1 = 2.L_B.q.Dn$

L_B is the extrinsic Debye length and

Dn is the diffusion constant.

Considering $W_8=2\mu$ and $L_8=1\mu$, the size for M7 $W_7=4\mu$ and $L_7=2\mu$ is obtained. The dimensions $W_1=2\mu$ and $L_1=2\mu$ of the D1 transistor were found by using the expression [13]:

$$I_{Sh} = W_1.L_1(C2.e^{-Uds}) e^{U} \quad (2)$$

where

$C2 = q.N_D.V$

N_D is the dopant concentration and

V depends on both drift and diffusion velocities.

The voltages variables $\{U, U_{ds}\}$ are normalized by thermal voltage.

Design considerations of the SBFL and Power Rail latch can be found in [14] and [11], respectively. In Fig. 4 the dc transfer curve of a DC^{2}FL inverter using such output stage is shown.

In the case of latched gates, frequently used to implement asynchronous pipelines and self-timed rings, SR DCFL NOR latch can appropriately replace the DC^{2}FL output stage, acting as a buffer and storage element. In DCVS approach, such a substitution is not possible because the correspondent SR NAND latch version is difficult to be built with DCFL gates [12].

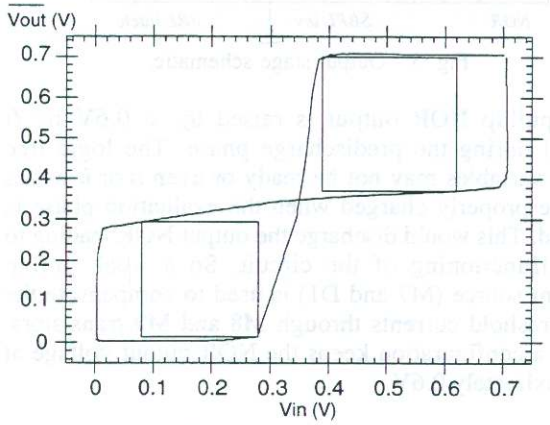

Fig. 4 - DC^{2}FL inverter dc transfer curve.

Simulation Results

A. *Full adder*

Full adder circuits were used to evaluate and compare this structure with the DCFL, DPTL and DCVS ones. The DC^{2}FL sum circuit is presented in Fig. 1. HSPICE simulation results are summarized in Table I. The power-delay products (Pot×td) were obtained considering average values. Power dissipation of DPTL, DCVS and DC^{2}FL full adder versions during standby state and evaluation phase are also plotted in Fig. 5.

TABLE I - Full adder simulation results.

	td (ps) fi-out/in-out	Pot (mW) prech./eval.	Pot×td (fJ)	# transistor
DCFL	137.5*	3.76*	517.0	42
DPTL	44.3 / - **	1.16 / 1.02	48.3	36
DCVS	210.4 / 238.8	1.15 / 1.02	243.7	56
DC^{2}FL	449.4 / 358.5	0.47 / 1.05	307.0	58

* In DCFL, there are not *fi* signal and precharge phase.
** In DPTL, the inputs must be available in the evaluation.

TABLE II - Latched full adder simulation results.

	td (ps) fi-out/in-out	Pot (mW) prech./eval.	Pot×td (fJ)	# transistor
DPTL	181.6 / ---	1.96 / 1.83	344.1	50
DCVS	317.3 / 344.0	2.16 / 2.13	709.2	70
DC^{2}FL	622.1 / 584.3	1.01 / 1.02	363.5	42

Nevertheless latched gates were also considered in order to evaluate the differential structure performances, as shown in Table II. For latched DPTL and DCVS gates, it was necessary to add the SR DCFL NOR latches to the outputs for memorization. A significant power reduction as well as the expected lower power-delay product were verified for the DC^{2}FL

B. *8-bit ripple carry adder*

A 8-bit ripple carry adder circuit was used to demonstrate the DC^{2}FL advantages. A test chip containing DC^{2}FL as well as DCVS versions was designed and fabricated through the CMP services in the Vitesse GaAs III technology. The chip layout is shown in Fig. 6. Table III presents the HSPICE simulation results.

TABLE III - 8-bit ripple carry adder simulation results.

	td (ns)	Pot (mW)	Pot×td (pJ)	# transistor
DCVS	0.903	8.93	8.06	448
DC^{2}FL	1.641	6.08	9.98	464

The most appealing feature of DC^{2}FL is its compatibility with DCVS which allows to replace some portions of functional blocks where the delay is not critical, saving power on standby state. Such design strategy can be easily extended to synchronous circuits, implementing critical paths in DCVS and the rest in DC^{2}FL . For example, the same 8-bit ripple carry adder operating in synchronous mode presents approximately 25% power saving in the precharge phase when designed using mixed DC^{2}FL - DCVS circuit while maintaining the same speed performance as the DCVS version.

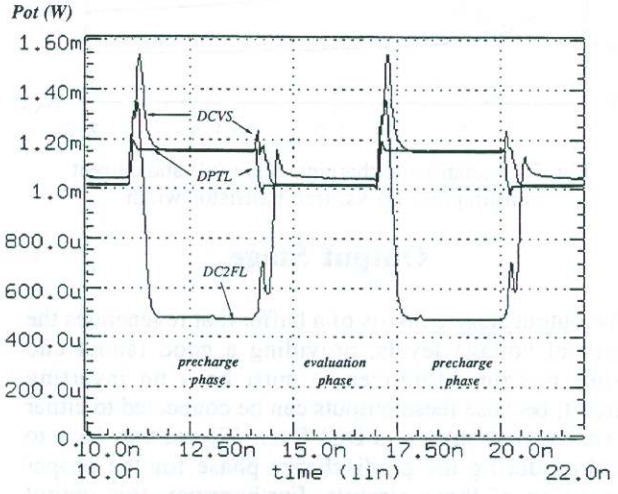

Fig. 5 - Power dissipation graph.

Conclusions

A new GaAs MESFET differential structure for self-timed circuits has been presented. The structure requires only one 2V power supply and uses a predischarge technique. The most important feature of the DC^{2}FL structure is its compatibility with the DCFL, DPTL and DCVS families. Levels of power-delay product

lower than DCFL and as low as DCVS are recorded. A 8-bit ripple carry adder chip test has demonstrated that DC^{2}FL is an appropriate structure to implement delay-insensitive asynchronous circuits. For the design of synchronous circuits a significant power reduction is obtained when circuits are implemented using mixed DC^{2}FL and DCVS approaches.

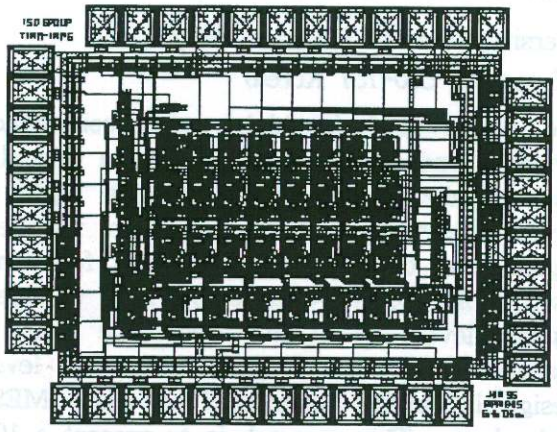

Fig. 6 - Test chip layout.

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